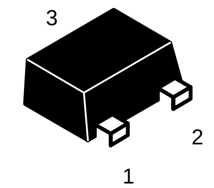
Small Signal MOSFET
115 mAmps, 60 Volts
N–Channel SOT–723

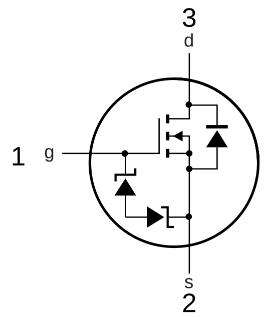
L2N7002EM3T5G
S-L2N7002EM3T5G



SOT-723

- Pb−Free Package is Available.
- ESD Protected:2000V
- S- Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

N - Channel



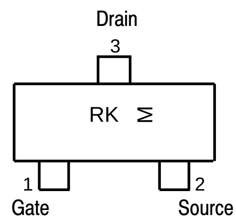
ORDERING INFORMATION

Device	Marking	Shipping
L2N7002EM3T5G S-L2N7002EM3T5G	RK	8000 Tape & Reel

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	60	Vdc
Drain Current – Continuous T_C = 25°C (Note 1.) – Pulse t < 10us	I_D I_{DM}	±115 ±800	mAdc
Gate–Source Voltage – Continuous	V_{GS}	±20	Vdc

MARKING DIAGRAM & PIN ASSIGNMENT



RK = Device Code
M = Month Code

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR–5 Board (Note 2.) T_A = 25°C Derate above 25°C	P_D	150 1.2	mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	833	°C/W
Junction and Storage Temperature	T_J, T_{stg}	–55 to +150	°C

1. The Power Dissipation of the package may result in a lower continuous drain current.
2. FR–5 = 1.0 x 0.75 x 0.062 in.
3. Alumina = 0.4 x 0.3 x 0.025 in 99.5% alumina.

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●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Gate-source leakage current	I_{GSS}	–	–	±10	μA	V_{GS}=±20V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	–	–	V	I_D=10μA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	–	–	1	μA	V_{DS}=60V, V_{GS}=0V
Gate threshold voltage	$V_{GS(th)}$	1	1.85	2.5	V	V_{DS}=V_{GS} , I_D=250uA
Drain-source on-state resistance	$R_{DS(on)}$*	–	–	7.5	Ω	I_D=0.5A, V_{GS}=10V
		–	–	7.5		I_D=0.05A, V_{GS}=5V
Forward transfer admittance	$\lvert Y_{fs}\rvert$*	80	–	–	mS	V_{DS}=10V, I_D=0.2A
Input capacitance	C_{iss}	–	25	50	pF	V_{DS}=25V V_{GS}=0V f=1MHz
Output capacitance	C_{oss}	–	10	25	pF	
Reverse transfer capacitance	C_{rss}	–	3.0	5.0	pF	
Turn-on delay time	$t_{d(on)}$*	–	12	20	ns	I_D=200mA, V_{DD}≒30V V_{GS}=10V, R_L=150Ω ,R_{GS}=10Ω
Turn-off delay time	$t_{d(off)}$*	–	20	30	ns	

* Pw≤300μs, Duty cycle≤1%

●Electrical characteristic curves

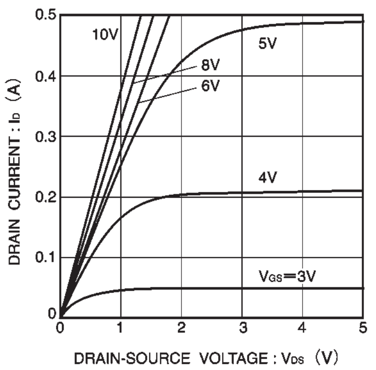

Fig.1 Typical output characteristics

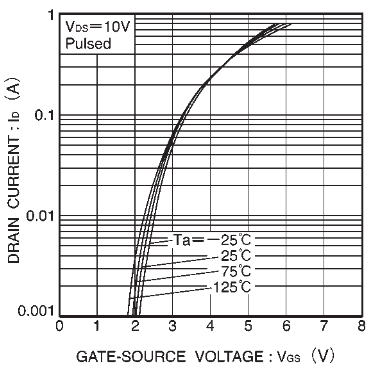

Fig.2 Typical transfer characteristics

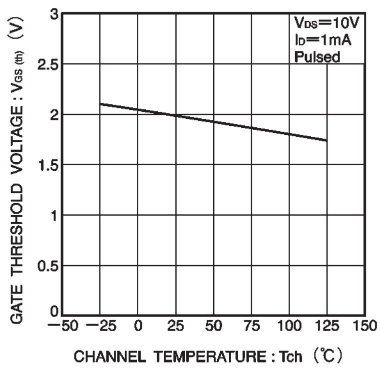

Fig.3 Gate threshold voltage vs. channel temperature

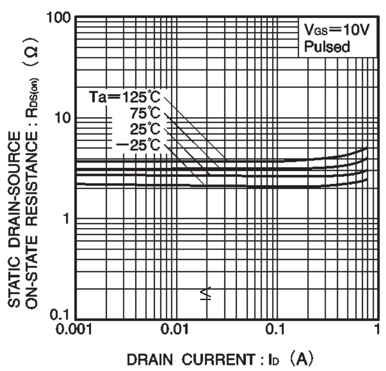

Fig.4 Static drain-source on-state resistance vs. drain current (I)

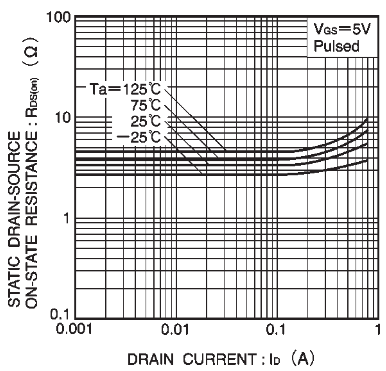

Fig.5 Static drain-source on-state resistance vs. drain current (Ⅱ)

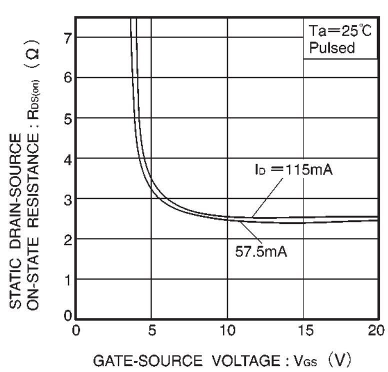

Fig.6 Static drain-source on-state resistance vs. gate-source voltage

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●Electrical characteristic curves (continues)

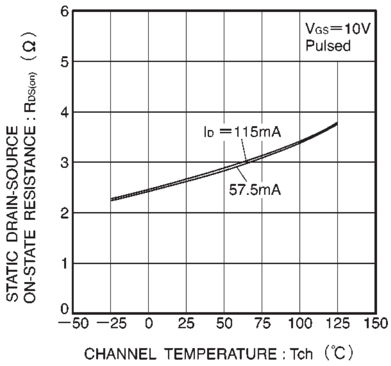


Fig.7 Static drain-source on-state resistance vs. channel temperature

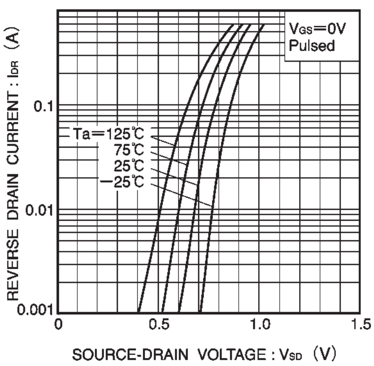


Fig.8 Reverse drain current vs. source-drain voltage (Ⅰ)

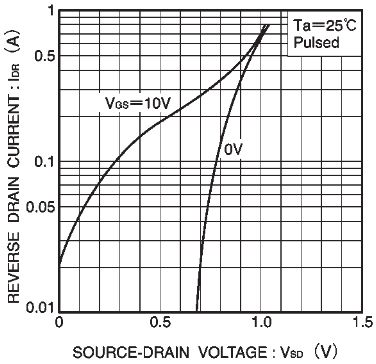


Fig.9 Reverse drain current vs. source-drain voltage (Ⅱ)

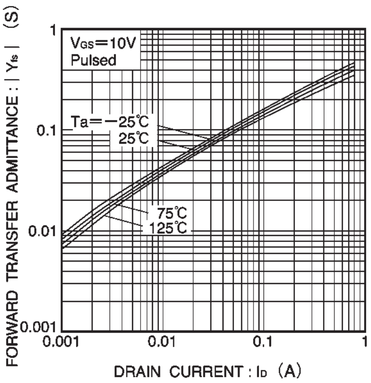


Fig.10 Forward transfer admittance vs. drain current

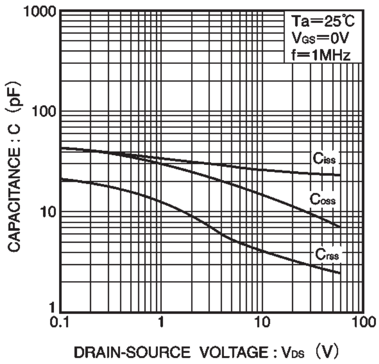


Fig.11 Typical capacitance vs. drain-source voltage

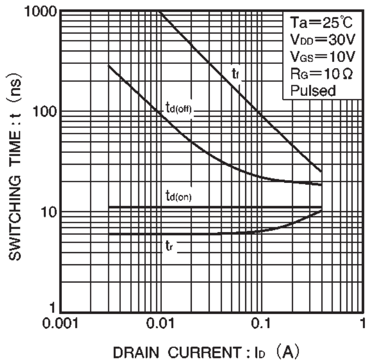


Fig.12 Switching characteristics (See Figures 13 and 14 for the measurement circuit and resultant waveforms)

●Switching characteristics measurement circuit

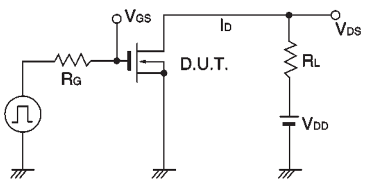


Fig.13 Switching time measurement circuit

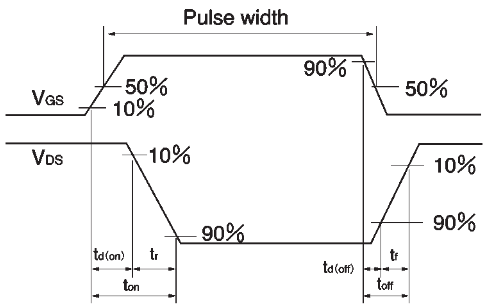
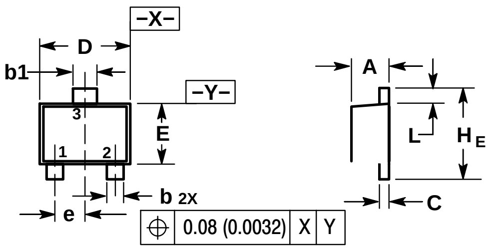


Fig.14 Switching time waveforms

SOT−723



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.45	0.50	0.55	0.018	0.020	0.022
b	0.15	0.20	0.27	0.0059	0.0079	0.0106
b1	0.25	0.3	0.35	0.010	0.012	0.014
C	0.07	0.12	0.17	0.0028	0.0047	0.0067
D	1.15	1.20	1.25	0.045	0.047	0.049
E	0.75	0.80	0.85	0.03	0.032	0.034
e	0.40 BSC			0.016 BSC		
H_E	1.15	1.20	1.25	0.045	0.047	0.049
L	0.15	0.20	0.25	0.0059	0.0079	0.0098

SOLDERING FOOTPRINT