

Small Signal MOSFET 115 mAmps, 60 Volts N-Channel SOT-23

- Pb-Free Package is Available.

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MAXIMUM RATINGS

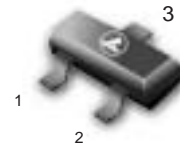
Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	V _{dc}
Drain-Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$)	V_{DGR}	60	V _{dc}
Drain Current - Continuous $T_C = 25^\circ\text{C}$ (Note 1.) $T_C = 100^\circ\text{C}$ (Note 1.) - Pulsed (Note 2.)	I_D I_D I_{DM}	± 115 ± 75 ± 800	mA _{dc}
Gate-Source Voltage - Continuous - Non-repetitive ($t_p \leq 50 \mu\text{s}$)	V_{GS} V_{GSM}	± 20 ± 40	V _{dc} V _{pk}

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board (Note 3.) $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	225 1.8	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	556	$^\circ\text{C}/\text{W}$
Total Device Dissipation Alumina Substrate, (Note 4.) $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	300 2.4	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	417	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

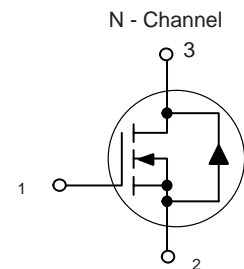
- The Power Dissipation of the package may result in a lower continuous drain current.
- Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.
- FR-5 = $1.0 \times 0.75 \times 0.062$ in.
- Alumina = $0.4 \times 0.3 \times 0.025$ in 99.5% alumina.

L2N7002LT1

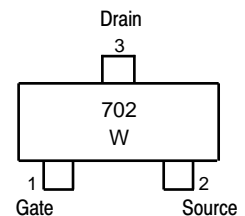


CASE 318, STYLE 21
SOT-23 (TO-236AB)

115 mAmps
60 Volts
 $R_{DS(on)} = 7.5 \Omega$



MARKING DIAGRAM & PIN ASSIGNMENT



702 = Device Code
W = Work Week

ORDERING INFORMATION

Device	Marking	Shipping
L2N7002LT1	702	3000 Tape & Reel
L2N7002LT1G	702(Pb-Free)	3000 Tape & Reel

L2N7002LT1

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage ($V_{GS} = 0, I_D = 10 \mu\text{A}$)	$V_{(BR)DSS}$	60	–	–	Vdc
Zero Gate Voltage Drain Current ($V_{GS} = 0, V_{DS} = 60 \text{ Vdc}$)	I_{DSS}	– –	– –	1.0 500	μA
Gate–Body Leakage Current, Forward ($V_{GS} = 20 \text{ Vdc}$)	I_{GSSF}	–	–	100	nA
Gate–Body Leakage Current, Reverse ($V_{GS} = -20 \text{ Vdc}$)	I_{GSSR}	–	–	-100	nA

ON CHARACTERISTICS (Note 2.)

Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$)	$V_{GS(th)}$	1.0	1.6	2.5	Vdc
On–State Drain Current ($V_{DS} \geq 2.0 V_{DS(on)}, V_{GS} = 10 \text{ Vdc}$)	$I_{D(on)}$	500	–	–	mA
Static Drain–Source On–State Voltage ($V_{GS} = 10 \text{ Vdc}, I_D = 500 \text{ mA}$) ($V_{GS} = 5.0 \text{ Vdc}, I_D = 50 \text{ mA}$)	$V_{DS(on)}$	– –	– –	3.75 0.375	Vdc
Static Drain–Source On–State Resistance ($V_{GS} = 10 \text{ V}, I_D = 500 \text{ mA}$) $T_C = 25^\circ\text{C}$ $T_C = 125^\circ\text{C}$ ($V_{GS} = 5.0 \text{ Vdc}, I_D = 50 \text{ mA}$) $T_C = 25^\circ\text{C}$ $T_C = 125^\circ\text{C}$	$r_{DS(on)}$	– – – –	1.4 – 1.8 –	7.5 13.5 7.5 13.5	Ohms
Forward Transconductance ($V_{DS} \geq 2.0 V_{DS(on)}, I_D = 200 \text{ mA}$)	g_{FS}	80	–	–	mmhos

DYNAMIC CHARACTERISTICS

Input Capacitance ($V_{DS} = 25 \text{ Vdc}, V_{GS} = 0, f = 1.0 \text{ MHz}$)	C_{iss}	–	17	50	pF
Output Capacitance ($V_{DS} = 25 \text{ Vdc}, V_{GS} = 0, f = 1.0 \text{ MHz}$)	C_{oss}	–	10	25	pF
Reverse Transfer Capacitance ($V_{DS} = 25 \text{ Vdc}, V_{GS} = 0, f = 1.0 \text{ MHz}$)	C_{rss}	–	2.5	5.0	pF

SWITCHING CHARACTERISTICS (Note 2.)

Turn–On Delay Time	$(V_{DD} = 25 \text{ Vdc}, I_D \cong 500 \text{ mA}, R_G = 25 \Omega, R_L = 50 \Omega, V_{gen} = 10 \text{ V})$	$t_{d(on)}$	–	7	20	ns
Turn–Off Delay Time		$t_{d(off)}$	–	11	40	ns

BODY–DRAIN DIODE RATINGS

Diode Forward On–Voltage ($I_S = 11.5 \text{ mA}, V_{GS} = 0 \text{ V}$)	V_{SD}	–	–	-1.5	Vdc
Source Current Continuous (Body Diode)	I_S	–	–	-115	mA
Source Current Pulsed	I_{SM}	–	–	-800	mA

2. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

TYPICAL ELECTRICAL CHARACTERISTICS

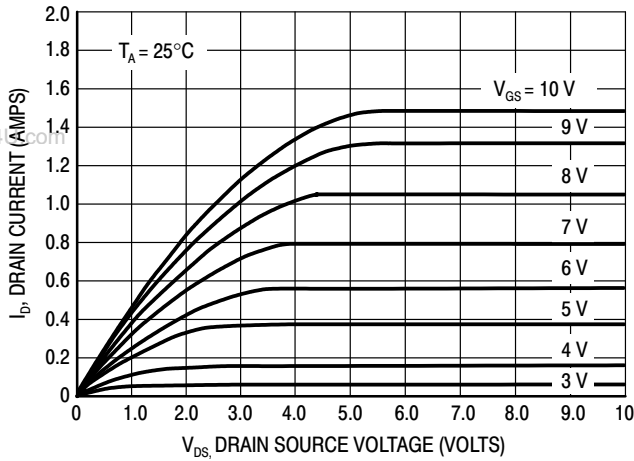


Figure 1. Ohmic Region

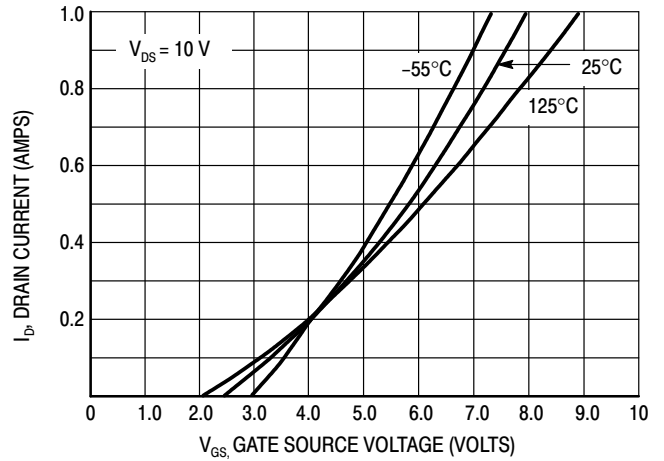


Figure 2. Transfer Characteristics

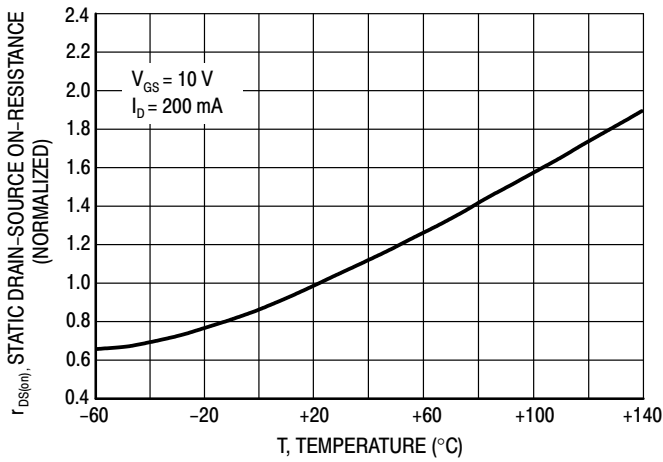


Figure 3. Temperature versus Static Drain-Source On-Resistance

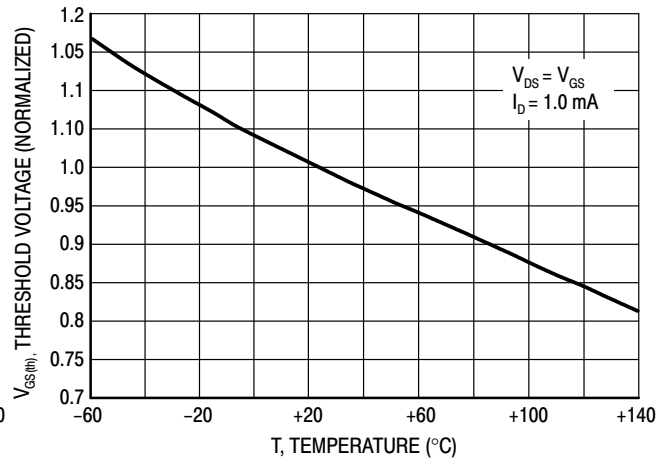


Figure 4. Temperature versus Gate Threshold Voltage