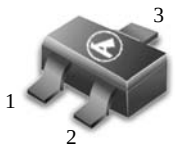
Small Signal MOSFET
115 mAmps, 60 Volts N–Channel SOT–323

L2N7002WT1G
S-L2N7002WT1G

●FEATURES

1)We declare that the material of product compliant with RoHS requirements and Halogen Free.
2)ESD Protected:1000V
3)S- Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

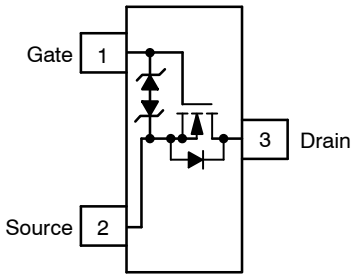


SOT– 323 (SC-70)

●ORDERING INFORMATION

Device	Marking	Shipping
L2N7002WT1G	6C	3000/Tape&Reel
L2N7002WT3G	6C	10000/Tape&Reel

Simplified Schematic



(Top View)

●MAXIMUM RATINGS(Ta = 25℃)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	60	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Drain Current – Continuous T_C = 25°C (Note 1.) T_C = 100°C (Note 1.) – Pulsed (Note 2.)	 I_D I_D I_{DM}	 ±115 ±75 ±800	mAdc
Gate–Source Voltage – Continuous – Non–repetitive (tp ≤ 50 μs)	 V_{GS} V_{GSM}	 ±20 ±40	 Vdc Vpk

●THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR–5 Board (Note 3.) TA = 25°C Derate above 25°C	P_D	 225 1.8	 mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate,(Note 4.) T_A = 25°C Derate above 25°C	P_D	 300 2.4	 mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature	T_J, T_{stg}	-55 to +150	°C

1. The Power Dissipation of the package may result in a lower continuous drain current.
2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
3. FR–5 = 1.0 x 0.75 x 0.062 in.
4. Alumina = 0.4 x 0.3 x 0.025 in 99.5% alumina.

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●ELECTRICAL CHARACTERISTICS (Ta= 25℃)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μAdc)	$V_{(BR)DSS}$	60	–	–	Vdc
Zero Gate Voltage Drain Current (T_J = 25℃)	I_{DSS}	–	–	1.0	μAdc
(V_{GS} = 0, V_{DS} = 60 Vdc) (T_J = 125℃)		–	–	500	
Gate–Body Leakage Current, Forward (V_{GS} = 20 Vdc)	I_{GSSF}	–	–	1	μAdc
Gate–Body Leakage Current, Reverse (V_{GS} = – 20 Vdc)	I_{GSSR}	–	–	-1	μAdc
ON CHARACTERISTICS (Note 2.)					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250uAdc)	$V_{GS(th)}$	1.0	1.6	2.5	Vdc
On–State Drain Current (V_{DS} ≥ 2.0 $V_{DS(on)}$, V_{GS} = 10 Vdc)	$I_{D(on)}$	500	–	–	mA
Static Drain–Source On–State Voltage	$V_{DS(on)}$				Vdc
(VGS = 10 Vdc, ID = 500 mAdc)		–	–	3.75	
(V_{GS} = 5.0 Vdc, I_D = 50 mAdc)		–	–	0.375	
Static Drain–Source On–State Resistance	$r_{DS(on)}$				Ohms
(V_{GS} = 10 V, I_D = 500 mAdc) (T_C = 25℃)		–	1.4	7.5	
(T_C = 125℃)		–	–	13.5	
(V_{GS} = 5.0 Vdc, I_D = 50 mAdc) (T_C = 25℃)		–	1.8	7.5	
(T_C = 125℃)		–	–	13.5	
Forward Transconductance (V_{DS} ≥ 2.0 $V_{DS(on)}$, I_D = 200 mAdc)	g_{FS}	80	–	–	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 25 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	–	17	50	pF
Output Capacitance (V_{DS} = 25 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	–	10	25	pF
Reverse Transfer Capacitance (V_{DS} = 25 Vdc, VGS = 0, f = 1.0 MHz)	C_{rss}	–	2.5	5.0	pF
SWITCHING CHARACTERISTICS (Note 2.)					
Turn–On Delay Time (V_{DD} = 25 Vdc , I_D =500 mAdc, R_G = 25 Ω, , R_L = 50 Ω, , V_{gen} = 10 V)	td(on)	–	7	20	ns
Turn–Off Delay Time	td(off)	–	11	40	ns
BODY–DRAIN DIODE RATINGS					
Diode Forward On–Voltage (I_S = 115 mAdc, V_{GS} = 0 V)	V_{SD}	–	–	–1.5	Vdc
Source Current Continuous (Body Diode)	I_S	–	–	–115	mAdc
Source Current Pulsed	I_{SM}	–	–	–800	mAdc

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

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ELECTRICAL CHARACTERISTIC CURVES

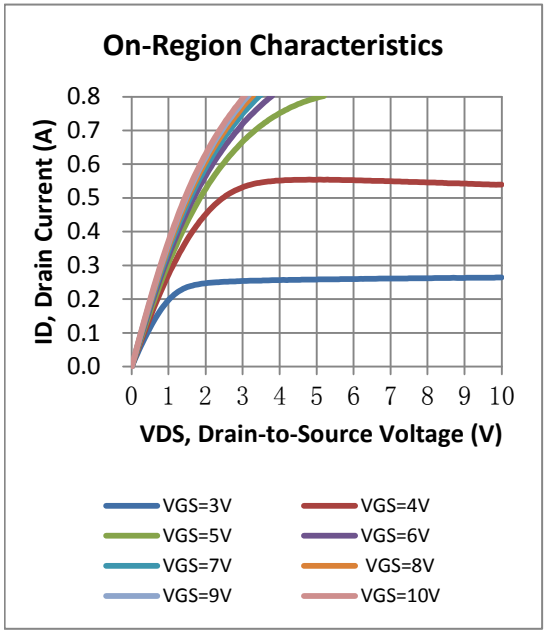


FIG1

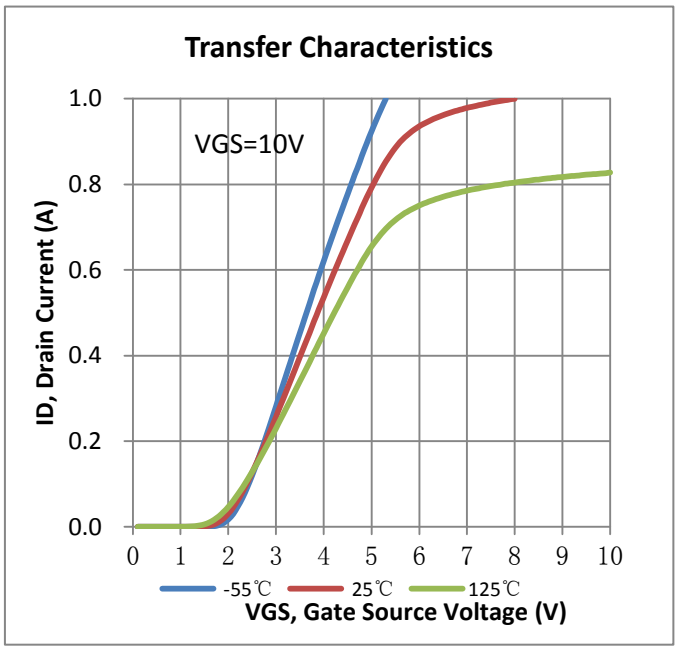


FIG2

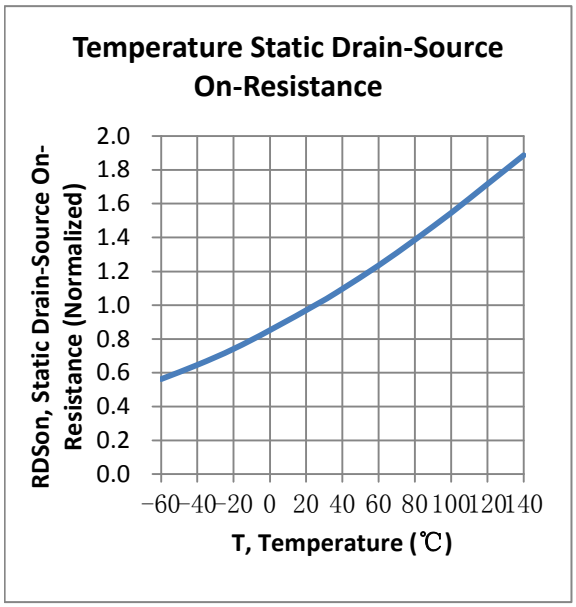


FIG3

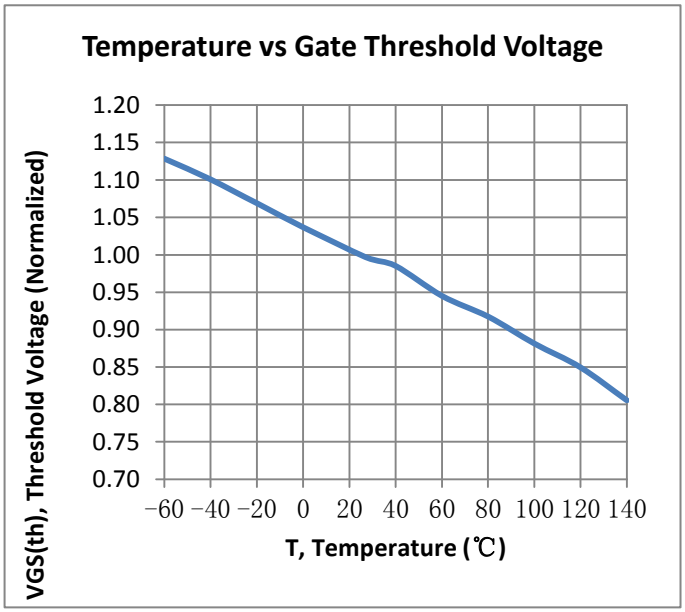
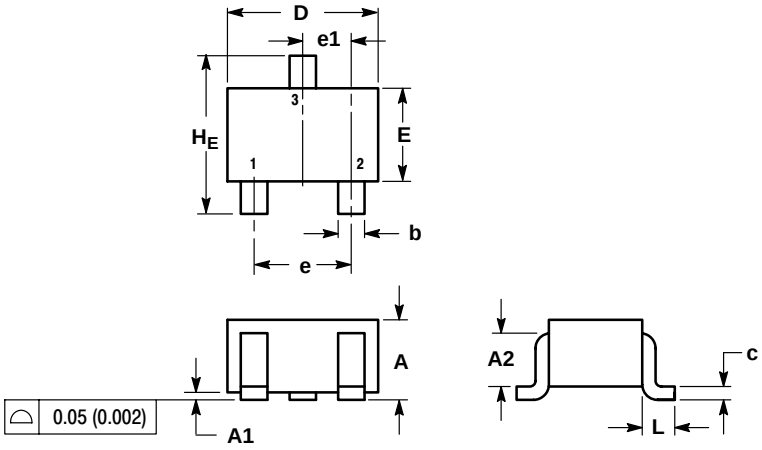


FIG4

L2N7002WT1G,S-L2N7002WT1G

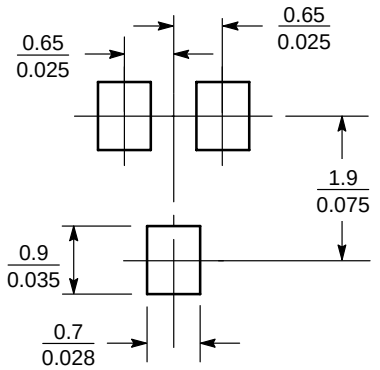
SC−70 (SOT−323)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

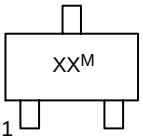
	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2		0.7 REF			0.028 REF	
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.10	2.20	0.071	0.083	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1		0.65 BSC			0.026 BSC	
L		0.425 REF			0.017 REF	
H_E	2.00	2.10	2.40	0.079	0.083	0.095

SOLDERING FOOTPRINT*



SCALE 10:1 $\left(\frac{mm}{inches}\right)$

GENERIC MARKING DIAGRAM



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.