L3654

LINEAR INTEGRATED CIRCUIT

PRELIMINARY DATA

PRINTER SOLENOID DRIVER

The L3654 is a printer solenoid driver containing ten open-collector driver outputs and a ten-bit serial-in, parallel-out shift register.
Data is clocked into the shift register serially and transferred to the open-collector outputs by an enable input. Serial input data is loaded by the rising edge of the clock. A serial output from the tenth bit is provided which changes at the falling edge of the clock. This output is not controlled by the enable input and remains active at all time.
Output stages are inhibited when the logic supply voltage falls below 6V.
Each output is rated at 250 mA (sink) and is clamped to ground internally at 50V to dissipate stored energy in inductive loads.
The L3654 is supplied in a 16 lead dual in-line plastic package, and its main fields of application comprise thermal printers, cash registers and printing pocket calculators.

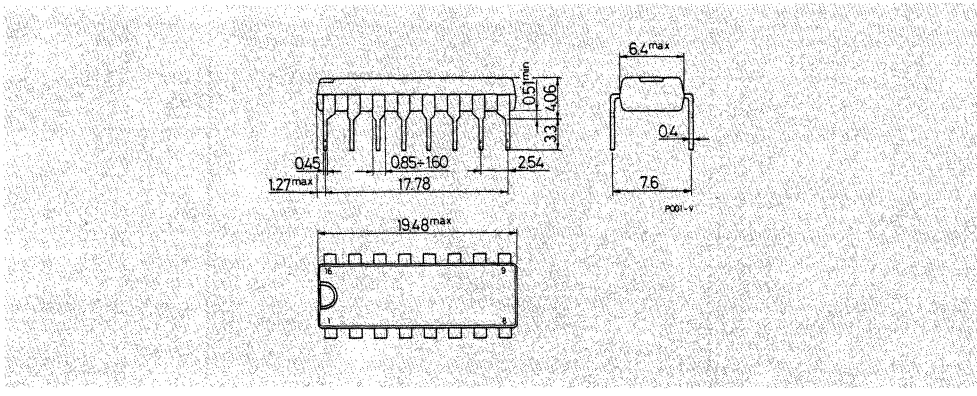
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	9.5	V
V_i	Input voltage	9.5	V
V_E	External supply voltage	45	V
I_o	Output current (single output)	0.4	A
I_g	Ground current	4.0	A
P_{tot}	Total power dissipation (T_{amb} = 70°C)	1	W
T_{stg}, T_j	Storage and junction temperature	-65 to 150	°C

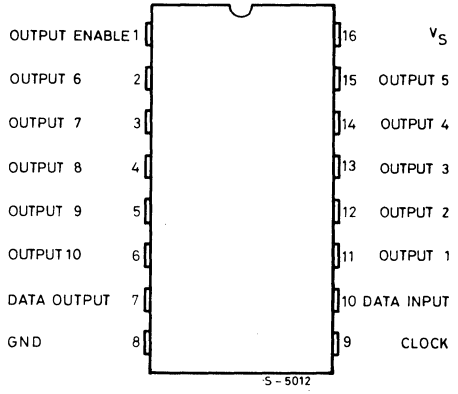
ORDERING NUMBER: L3654 B

MECHANICAL DATA

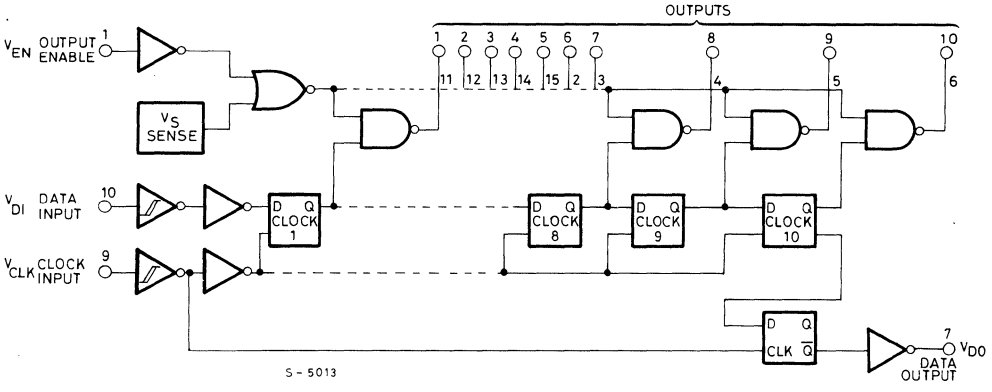
Dimensions in mm



CONNECTION DIAGRAM
(top view)



LOGIC DIAGRAM



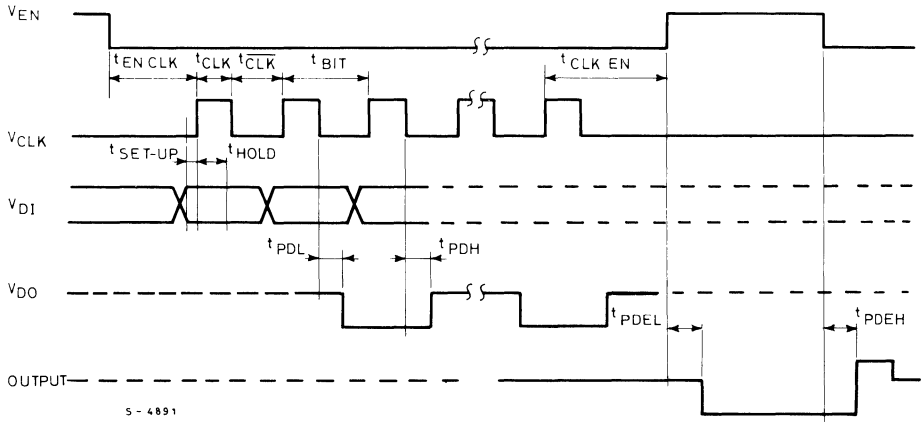
THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (V_s= 8.5V, V_{ss}= 30V, T_{amb}= 0° to 70°C, unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			7.5		9.5	V
I_S	Supply current	T_{amb}= 25°C V_s = 9.5V	V_{EN}= 0V; V_{DO}= 0V		27	40	mA
			V_{EN}= 2.6V I_o = 250 mA (each bit)		55	70	mA
V_E	External operating supply voltage					40	V
I_{leak}	Output leakage current (each output)	V_{ss}= 40V	V_{EN}= 0V			1	mA
V_Z	Internal clamp voltage	I_Z = 0.3A	V_{EN}= 0V	45	50	65	V
$V_{CE\ sat}$	Output saturation voltage	I_o = 250 mA	V_{EN}= 2.6V			1.6	V
V_{DI} V_{CLK} V_{EN}	Input logic levels (pins 1, 9, 10)	Low State (L)				0.8	V
		High state (H)		2.6			
I_{DI}	Data input current	V_{DI}= 2.6V	T_{amb}= 70°C	0.3	0.57		mA
			T_{amb}= 0°C		0.57	0.75	
		V_{DI}= 1V	T_{amb}= 70°C		220		μA
I_{CLK}	Clock input current	V_{CLK}= 2.6V	T_{amb}= 70°C	0.2	0.33		mA
			T_{amb}= 0°C		0.33	0.5	
		V_{CLK}= 1V	T_{amb}= 70°C		125		μA
I_{EN}	Enable input current	V_{EN}= 2.6V	T_{amb}= 70°C	0.2	0.33		mA
			T_{amb}= 0°C		0.33	0.5	
		V_{EN}= 1V	T_{amb}= 70°C		125		μA
R_{IN}	Input pull-down resistance Clock input	T_{amb}= 25°C	$V_{CLK} < V_s$		8		KΩ
	Enable input	T_{amb}= 25°C	$V_{EN} < V_s$		8		
	Data input	T_{amb}= 25°C	$V_{DI} < V_s$		4.5		
V_{DO}	Output logic levels (pin 7)	Low state (L) V_{DI}= 0V	I_{DO}(pin 7)= 0		0.01	0.5	V
		High state (H) V_{DI}= 2.6V I_{DO} (pin 7) = -0.75 mA		2.6	3.4		V
R_{DO}	Output pull-down resistance (pin 7)	V_{DI}= 0V	V_{DO}= 1V		14		KΩ

Fig. 1 - Timing diagram



ELECTRICAL CHARACTERISTICS (see fig. 1 and the section "definition of terms")

Parameter		Test conditions	Min.	Typ.	Max.	Unit
Clock, data and enable input	t_{CLK}		4			µs
	$\overline{t_{CLK}}$		5.5			
	t_{SET-UP}		1			
	t_{HOLD}		3			
Clock to enable delay	$t_{CLK\ EN}$		2 t_{BIT}			
Enable to clock delay	$t_{EN\ CLK}$		t_{BIT}			
Data output delay	t_{PDH}, t_{PDL}	R_L= 5KΩ, $C_L \leqslant$ 10 pF		0.8	2.5	µs
Output delay	t_{PDEL}			3		µs
	t_{PDEH}			3.5		
Output rise time		R_L= 100 Ω, $C_L <$ 100 pF		1.2		µs
Output fall time		R_L= 100 Ω, $C_L <$ 100 pF		1.2		µs
V_{DO} rise time				0.4		µs
V_{DO} fall time				0.4		µs

DEFINITION OF TERMS

V_{ss} : External power supply voltage. The return for open-collector relay driver outputs.

V_{DI}, V_{CLK}, V_{EN} : The voltages at the data, clock and enable inputs respectively.

V_{DO} : The voltage at data output.

t_{BIT} : Period of the incoming clock.

t_{CLK} : The portion of t_{BIT} when $V_{CLK} \geqslant 2.6V$.

$\overline{t_{CLK}}$: The portion of t_{BIT} when $V_{CLK} \leqslant 0.8V$.

t_{HOLD} : The time following the start of t_{CLK} required to transfer data within the shift register.

$t_{SET\text{-}UP}$: The time prior to the end of $\overline{t_{CLK}}$ required to insure valid data at the shift register input for subsequent clock transitions.