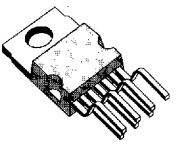
DUAL MULTIFUNCTION VOLTAGE REGULATOR

ADVANCE DATA

- STANDBY OUTPUT VOLTAGE PRECISION 5V ± 2%
- OUTPUT 2 TRACKED TO THE STANDBY OUTPUT
- OUTPUT 2 DISABLE FUNCTION FOR STANDBY MODE
- VERY LOW QUIESCENT CURRENT, LESS THAN 250µA, IN STANDBY MODE
- OUTPUT CURRENTS : I_{O1} = 50mA, I_{O2} = 500mA
- VERY LOW DROPOUT (max 0.4V/0.6V)
- OPERATING TRANSIENT SUPPLY VOLTAGE UP TO 40V
- POWER-ON RESET CIRCUIT SENSING THE STANDBY OUTPUT VOLTAGE
- POWER-ON RESET DELAY PULSE DEFINED BY THE EXTERNAL CAPACITOR
- THERMAL SHUTDOWN AND SHORT CIRCUIT PROTECTIONS



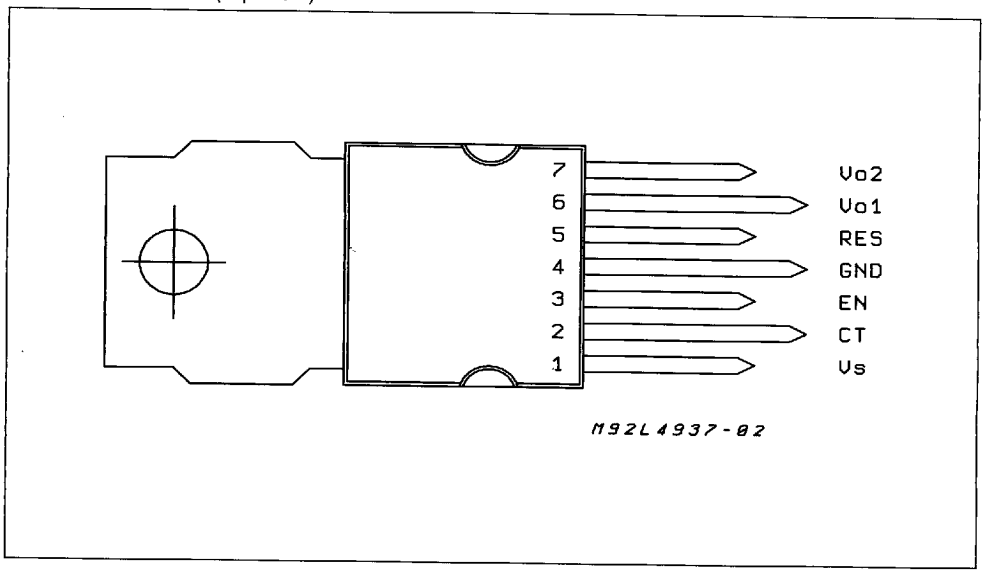
Heptawatt

ORDERING NUMBERS : L4937

DESCRIPTION

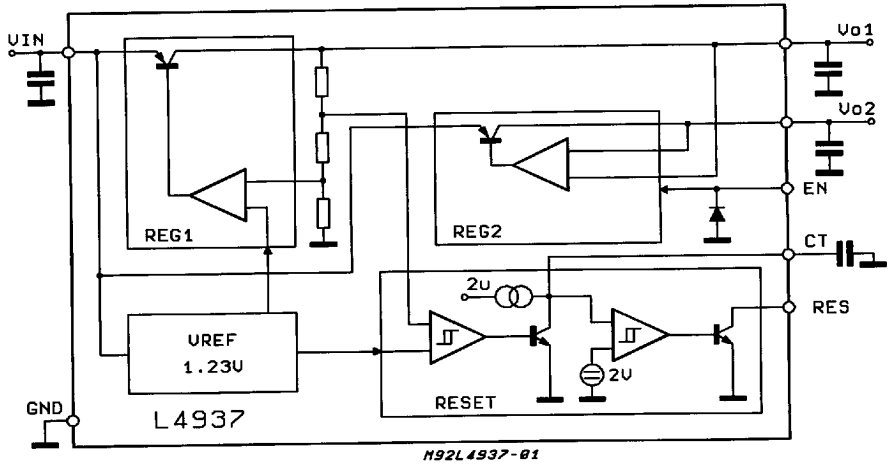
The L4937 is a monolithic integrated dual voltage regulators with two very low dropout outputs and additional functions such as power-on reset and input voltage sense. It is designed for supplying microcomputer controlled systems specially in automotive applications.

PIN CONNECTION (top view)



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



THERMAL DATA

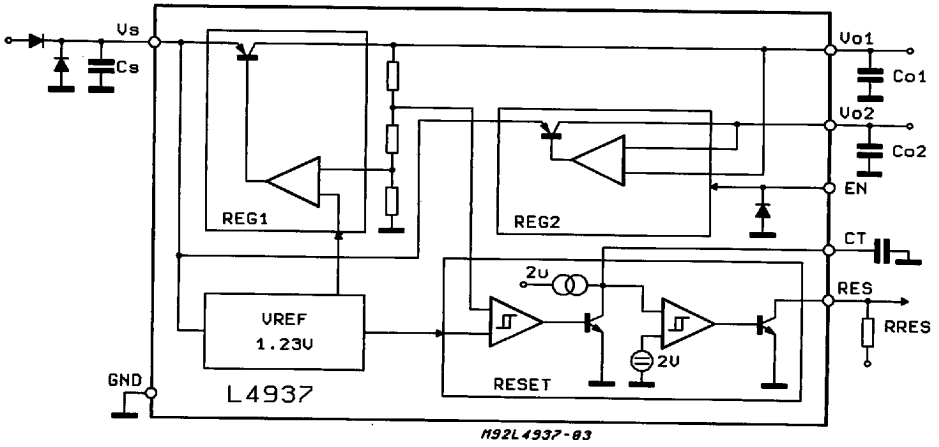
$R_{th\ j\text{-}c}$	Thermal Resistance Junction-case	Max	3	°C/W

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	D.C. Supply Voltage Transient Supply Voltage (T < 1s)	28 40	V V
T_j, T_{stg}	Junction and Storage Temperature Range	– 55 to 150	°C
I_{EN}	Enable Input Current (V_{EN} < – 0.3V)	– 1	mA
V_{EN}	Enable Input Voltage	V_s	V
V_{RES}	Reset Output Voltage	20	V
I_{RES}	Reset Output Current	5	mA
P_D	Power Dissipation (T_A = 80°C, $R_{th\ heatsink}$ = 9°C/W)	5	W

Note : The circuit is ESD protected according to MIL–STD–883C.

APPLICATION CIRCUIT



Cs ≥ 1µF ; C_{o1} ≥ 6µF ; C_{o2} ≥ 10µF, ESR < 10Ω at 10KHz

ELECTRICAL CHARACTERISTICS (V_S = 14V ; $-40°C \le T_j \le 125°C$ unless otherwise specified).

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage				25	V
V_{O1}	Standby Output Voltage	T_j = 25°C ; I_{O1} = 1mA	4.95	5.00	5.05	V
V_{O1}	Standby Output Voltage	$6V \le V_S \le 25V$ $1mA \le I_{O1} \le 50mA$	4.90	5.00	5.10	V
V_{O2}-V_{O1}	Output Voltage 2 Tracking Error (note1)	$6V \le V_S \le 25V$ $5mA \le I_{O2} \le 500mA$ Enable = LOW	− 25		+ 25	mV
V_{DP1}	Dropout Voltage 1	I_{O1} = 10mA I_{O1} = 50mA		0.1 0.2	0.25 0.4	V V
V_{IO1}	Input to output Voltage Difference in Undervoltage Condition	V_S = 4V, I_{O1} = 35mA			0.4	V
V_{DP2}	Dropout Voltage 2	I_{O2} = 100mA I_{O2} = 500mA		0.2 0.3	0.3 0.6	V V
V_{IO2}	Input to output Voltage Difference in Undervoltage Condition	V_S = 4.6V, I_{O2} = 350mA			0.6	V
$V_{OL1.2}$	Line Regulation	$6V \le V_S \le 25V$ I_{O1} = 1mA, I_{O2} = 5mA			20	mV
V_{OLIO1}	Load Regulation 1	$1mA \le I_{O1} \le 50mA$			25	mV
V_{OLO2}	Load Regulation 2	$5mA \le I_{O2} \le 500mA$			50	mV
I_{LIM1}	Current Limit 1	V_{O1} = 4.5V V_{O1} = 0V (note2)	55 25	100	200 100	mA mA
I_{LIM2}	Current Limit 2	V_{O2} = 0V	550	1000	1500	mA
I_{QSB}	Quiescent Current Standby Mode (output 2 disabled)	I_{O1} = 0.3mA ; T_j < 100°C $V_{EN} \ge 2.4V$ Vs = 14V Vs = 3.5V		 150 300	 250 800	 µA µA
I_Q	Quiescent Current	I_{O1} = 50mA I_{O2} = 500mA			30	mA

ENABLE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ENL}	Enable Input LOW Voltage (output 2 active)		− 0.3		1.5	V
V_{ENH}	Enable Input HIGH Voltage		2.4		7	V
V_{ENhyst}	Enable Hysteresis		30	75	200	mV
I_{EN}	Enable Input Current	$0V < V_{EN} < 1.2V$ $2.5V < V_{EN} < 7V$	− 10 − 1	− 1.5 0	− + 1	µA µA

RESET

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{Rt}	Reset Low Threshold Voltage	Vs = 14V	V_{o1}-0.4	4.7	V_{o1}-0.1	V
V_{Rth}	Reset Threshold Hysteresis		50	100	200	mV
t_{RD}	Reset Pulse Delay	C_T = 100nF ; t_R > 100µs	55	100	180	ms
t_{RR}	Reset Reaction Time	C_T = 100nF	1	10	50	µs
V_{RL}	Reset Output LOW Voltage	R_{RES} = 10KΩ to V_{O1} $V_S \geq 3V$			0.4	V
I_{LRES}	Reset Output HIGH Leakage	V_{RES} = 5V			1	µA
V_{CTth}	Delay Comparator Threshold			2.0		V
$V_{CTth, hyst}$	Delay Comparator Threshold Hysteresis			100		mV

Note : 1 : V_{O2} connected to ADJ.V_{O2} can be set to higher values by inserting an external resistor divider.
2 : Foldback characteristic

FUNCTIONAL DESCRIPTION

The L4937 is based on the SGS-THOMSON Microelectronics modular voltage regulator approach. Several out-standing features and auxiliary functions are provided to meet the requirements of supplying the microprocessor systems used in automotive applications.

Furthermore the device is suitable also in other applications requiring two stabilized voltages.

The modular approach allows other features and functions to be realized easily when required.

STANDBY REGULATOR

The standby regulator uses an Isolated Collector Vertical PNP transistor as the regulating element. This structure allows a very low dropout voltage at currents up to 50mA. The dropout operation of the standby regulator is maintained down to 2V input supply voltage. The output voltage is regulated up to the transient input supply voltage of 40V. This feature avoids functional interruptions which could be generated by overvoltage pulses.

The typical curve of the standby output voltage as a function of the input supply voltage is shown in fig. 1.

The current consumption of the device (quiescent current) is less than 250µA when output 2 is disabled (standby mode). The dropout voltage is controlled to reduce the quiescent current peak in the undervoltage region and to improve the transient response in this region.

The quiescent current is shown in fig. 2 as a function of the supply input voltage 2.

OUTPUT 2 VOLTAGE

The output 2 regulator uses the same output structure as the standby regulator, but rated for an output current of 500mA.

The output 2 regulator works in tracking mode with the standby output voltage as a reference voltage.

The output 2 regulator can be switched off via the Enable input.

Figure 1 : Output Voltage vs. Input Voltage.

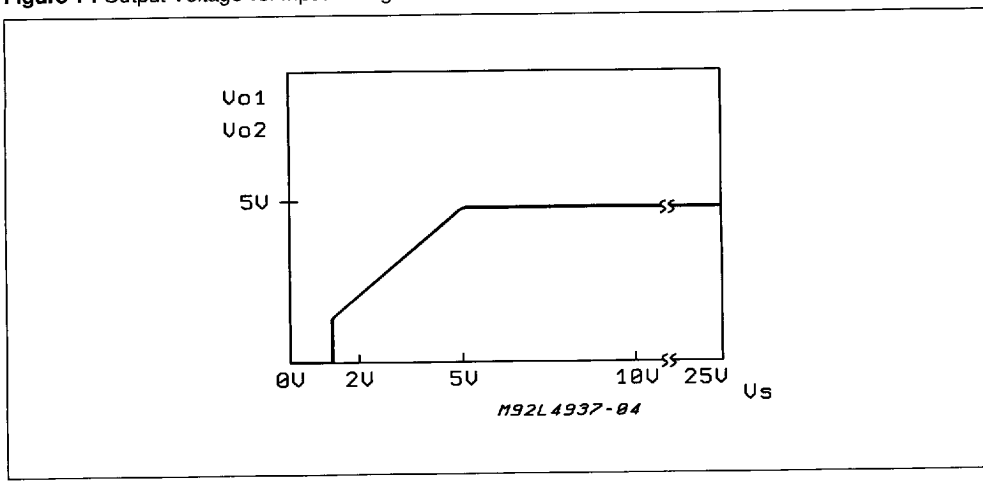
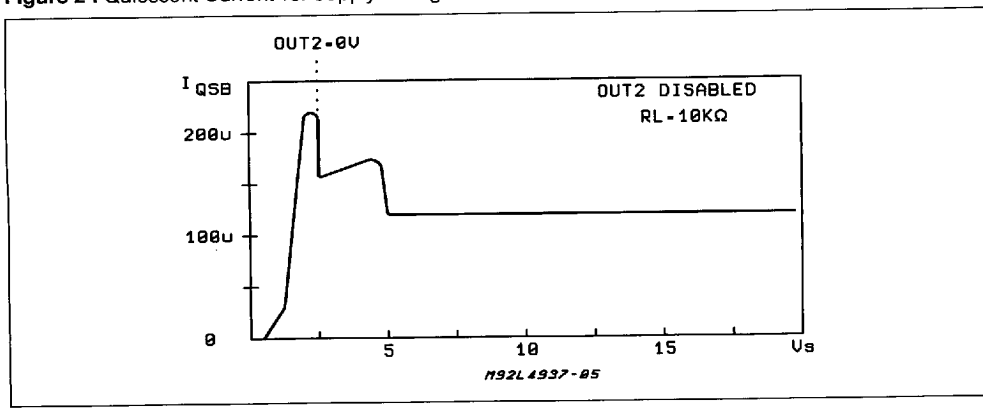


Figure 2 : Quiescent Current vs. Supply Voltage.



RESET CIRCUIT

The block circuit diagram of the reset circuit is shown in fig. 3. The reset circuit supervises the standby output voltage. The reset threshold of 4.7V is defined by the internal reference voltage and the standby output divider.

The reset pulse delay time t_{RD}, is defined by the charge time of an external capacitor C_T :

$$t_{RD} = \frac{C_T \times 2V}{2\mu A}$$

The reaction time of the reset circuit depends on the discharge time limitation of the reset capacitor C_T and is proportional to the value of C_T.

The reaction time of the reset circuit increases the noise immunity. In fact, if the standby output voltage drops below the reset threshold for a time shorter than the reaction time t_{RR}, no reset output variation occurs. The nominal reset delay is generated for standby output voltage drops longer than the time necessary for the complete discharging of the capacitor C_T. This time is typically equal to 50µs if C_T = 100nF. The typical reset output waveforms are shown in fig.

Figure 3 : Block Diagram of the Reset Circuit.

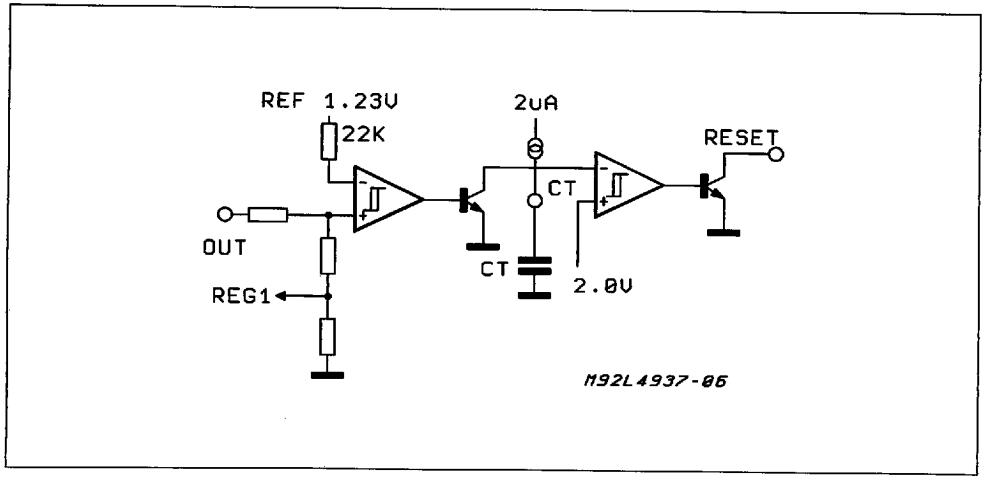


Figure 4 : Typical Reset Output Waveforms.