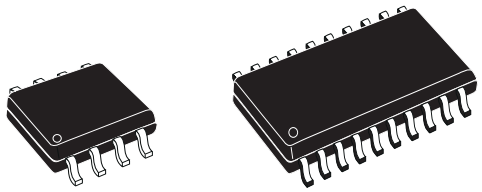
# L4989

## Low power voltage regulator

### Features

- Operating DC supply voltage range 5.6V to 31V
- Very low quiescent current with watchdog disabled
- Precision output voltage (3%)
- Low drop voltage (180mV typ ai $I_o$=150mA)
- Reset circuit sensing the output voltage down to 1V
- Programmable reset delay with external capacitor
- Watchdog disable input
- Programmable watchdog timer with external capacitor
- Thermal shutdown and short circuit protection
- Wide temperature range ($T_j$ = -40°C to 150°C)



SO-8 SO-20



**Table 1. Device summary**

| Package | Order codes | |
|---|---|---|
| | Tube | Tape & reel |
| SO-8 | L4989D | L4989D013TR |
| SO-20 | L4989MD | L4989MD013TR |

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# 1 Block diagram and pin configuration

**Figure 1. Block diagram**

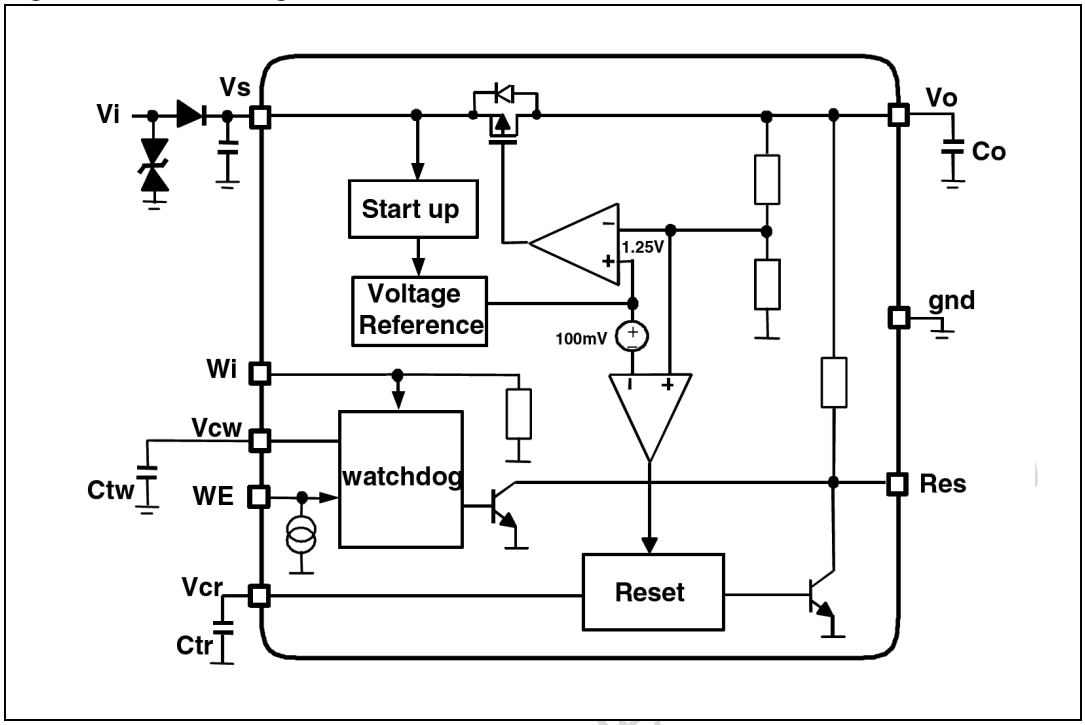
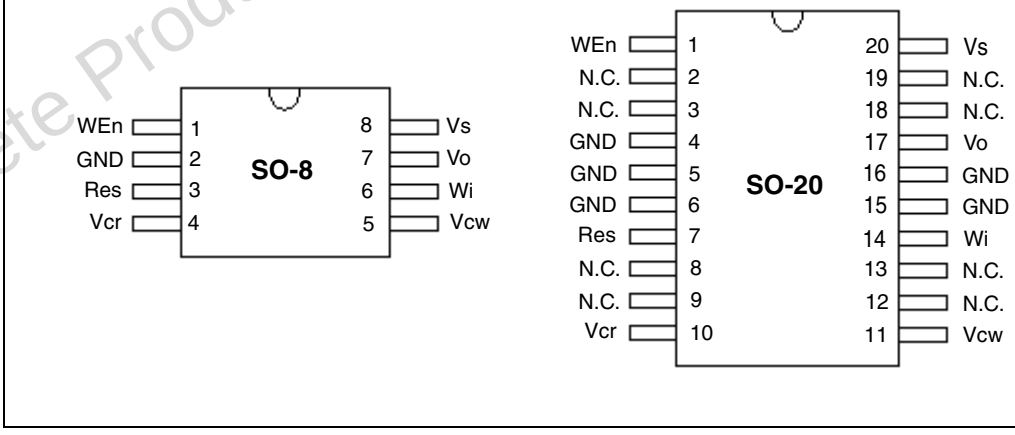


**Table 2. Pins description**

| Pin name | SO-8(D) | S0-20(MD) | Function |
|---|---|---|---|
| WEn | 1 | 1 | Watchdog Enable input<br>If high watchdog functionality is active |
| Gnd | 2 | 4 | Ground reference |
| Gnd | | 5, 6, 15, 16 | Ground.<br>Connected these pins to a heat spreader ground |
| Res | 3 | 7 | Reset output.<br>It is pulled down when output voltage goes below Vo_th or frequency at Wi is too low. |
| Vcr | 4 | 10 | Reset timing adjust.<br>A capacitor between Vcr pin and gnd, sets the reset delay time (trd) |
| Vcw | 5 | 11 | Watchdog timer adjust<br>A capacitor between Vcw pin and gnd, sets the time response of the watchdog monitor. |
| Wi | 6 | 14 | Watchdog input.<br>If the frequency at this input pin is too low, the Reset output is activated. |
| Vo | 7 | 17 | Voltage regulator output<br>Block to ground with a capacitor >100nF (needed for regulator stability) |
| Vs | 8 | 20 | Supply voltage<br>Block to ground directly at IC pin with a capacitor |
| N.C. | | 2, 3, 8, 9, 12, 13, 18, 19 | Not connected |

**Figure 2. Pins configuration**



# 2 Electrical specifications

## 2.1 Absolute maximum ratings

**Table 3. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{Vsdc}$ | DC supply voltage | -0.3 to 40 | V |
| $I_{Vsdc}$ | Input current | Internally limited | |
| $V_{Vo}$ | DC output voltage | -0.3 to 6 | V |
| $I_{Vo}$ | DC output current | Internally limited | |
| $V_{Wi}$ | Watchdog input voltage | -0.3 to $V_{Vo}$ + 0.3 | V |
| $V_{od}$ | Open Drain output voltage | -0.3 to $V_{Vo}$ + 0.3 | V |
| $I_{od}$ | Open Drain output current | Internally limited | |
| $V_{cr}$ | Reset delay voltage | -0.3 to $V_{Vo}$ + 0.3 | V |
| $V_{cw}$ | Watchdog delay voltage | -0.3 to $V_{Vo}$ + 0.3 | V |
| $V_{WEn}$ | Watchdog Enable input voltage | -0.3 to 40 | V |
| $T_j$ | Junction temperature | -40 to 150 | “C |
| $V_{ESD}$ | ESD voltage level (HBM-MIL STD 883C) | ±2 | kV |

*Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.*

## 2.2 Thermal data

**Table 4. Thermal data**

| Symbol | Parameter | S0-8 | S0-12+4+4 | Unit |
|---|---|---|---|---|
| $R_{th\text{-}jamb}$ | Thermal resistance junction to ambient | 130 to 180 | 50(1) | °C/W |

1. With 6 sq. cm on board heat sink.

## 2.3 Electrical characteristics

$V_s$ =5.6V to 31V, $T_j$= -40°C to +150°C unless otherwise specified.

**Table 5. General**

| Pin | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Vo | $V_{o\_ref}$ | Output voltage | Vs = 5.6 to 31V<br>Io = 1 to 150 mA | 4.85 | 5.0 | 5.15 | V |
| Vo | $I_{short\_13}$ | Short circuit current | Vs = 13.5V(1) | 160 | 210 | 250 | mA |
| Vo | $I_{lim}$ | Output current limitation | Vs = 13.5V(1) | 170 | 250 | 290 | mA |
| Vs, Vo | $V_{line}$ | Line regulation voltage | Vs = 5.6 to 31V<br>Io = 1 to 150mA | | | 25 | mV |
| Vo | $V_{load}$ | Load regulation voltage | Io = 1 to 150mA | | | 25 | mV |
| Vs, Vo | $V_{dp}$ | Drop voltage | Io = 150mA | | 180 | 400 | mV |
| Vs, Vo | SVR | Ripple rejection | fr = 100 Hz | 55 | | | dB |
| Vs, Vo | $I_{qs\_1}$ | Current consumption with watchdog not active<br>$I_{qs\_1}= I_{VS}-I_O$ | Vs=13.5V, Io<1mA,<br>WEn = low | | 69 | 115 | µA |
| Vs, Vo | $I_{qs\_10}$ | Current consumption with watchdog not active<br>$I_{qs\_10}= I_{VS}-I_O$ | Vs=13.5V,<br>Io= 10mA,<br>WEn = low | | 127 | 300 | µA |
| Vs, Vo | $I_{qs\_50}$ | Current consumption with watchdog not active<br>$I_{qs\_50}= I_{VS}-I_O$ | Vs=13.5V,<br>Io= 50mA,<br>WEn = low | | 498 | 900 | µA |
| Vs, Vo | $I_{qs\_150}$ | Current consumption with watchdog not active<br>$I_{qs\_150}= I_{VS}-I_O$ | Vs=13.5V,<br>Io= 150mA,<br>WEn = low | | 1.40 | 2 | mA |
| Vs, Vo | $I_{qn\_1}$ | Current consumption with watchdog active<br>$I_{qn\_1}= I_{VS}-I_O$ | Vs=13.5V, Io<1mA,<br>WEn = high | | 110 | 170 | µA |
| Vs, Vo | $I_{qn\_10}$ | Current consumption with watchdog active<br>$I_{qn\_10}= I_{VS}-I_O$ | Vs=13.5V,<br>Io= 10mA,<br>WEn = high | | 168 | 350 | µA |
| Vs, Vo | $I_{qn\_50}$ | Current consumption with watchdog active<br>$I_{qn\_50}= I_{VS}-I_O$ | Vs=13.5V,<br>Io= 50mA,<br>WEn = high | | 538 | 1000 | µA |
| Vs, Vo | $I_{qn\_150}$ | Current consumption with watchdog active<br>$I_{qn\_150}= I_{VS}-I_O$ | Vs=13.5V,<br>Io= 150mA,<br>WEn = high | | 1.45 | 2 | mA |
| | Tw | Thermal protection temperature | | 150 | | 190 | °C |
| | Tw_hy | Thermal protection temperature hysteresis | | | 10 | | °C |

1. See *Figure 3*.

**Table 6. Reset**

| Pin | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Res | Vres_l | Reset output low voltage | $R_{ext}$ = 5kΩ to Vo, Vo > 1V | | | 0.4 | V |
| Res | $I_{Res\_lkg}$ | Reset output high leakage current | $V_{Res}$ = 5V | | | 1 | µA |
| Res | $R_{Res}$ | Pull up internal resistance | Versus Vo | 10 | 20 | 40 | kΩ |
| Res | Vo_th | Reset threshold voltage | Vs = 5.6 to 31V, Io = 1 to 150mA | 6% | 8% | 10% | Below $V_{o\_ref}$ |
| Vcr | Vrlth | Reset timing low threshold | Vs = 13.5V | 10% | 13% | 16% | $V_{o\_ref}$ |
| Vcr | Vrhth | Reset timing high threshold | Vs =13.5V | 44% | 47% | 50% | $V_{o\_ref}$ |
| Vcr | Icr | Charge current | Vs = 13.5V | 8 | 15 | 30 | µA |
| Vcr | Idr | Discharge current | Vs = 13.5V | 8 | 15 | 30 | µA |
| Res | Trr_2 | Reset reaction time(1) | Vo = $V_{o\_th}$ -100mV | 100 | 250 | 700 | µs |
| Res | Trd | Reset delay time | Vs = 13.5V, Ctr = 1nF | 65 | 115 | 165 | ms |

1. When Vo becomes lower than 4V, the reset reaction time decreases down to 2µs assuring a faster reset condition in this particular case.

**Table 7. Watchdog**

| Pin | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Wi | Vih | Input high voltage | Vs = 13.5V | 3.5 | | | V |
| Wi | Vil | Input low voltage | Vs = 13.5V | | | 1.5 | V |
| Wi | Vih | Input hysteresis | Vs = 13.5V | | 500 | | mV |
| Wi | Rwi | Pull down resistor | Vs = 13.5V | 30 | 100 | 250 | KΩ |
| Vcw | Vwhth | High threshold | Vs = 13.5V | 44% | 47% | 50% | $V_{o\_ref}$ |
| Vcw | Vwlth | Low threshold | Vs = 13.5V | 10% | 13% | 16% | $V_{o\_ref}$ |
| Vcw | Icwc | Charge current | Vs = 13.5V, Vcw = 0.1V | 5 | 10 | 20 | µA |
| Vcw | Icwd | Discharge current | Vs = 13.5V, Vcw = 2.5V | 1.25 | 2.5 | 5 | µA |
| Vcw | Twop | Watchdog period | Vs = 13.5V, Ctw = 47nF | 20 | 40 | 80 | ms |
| Res | twol | Watchdog output low time | Vs = 13.5V, Ctw = 47nF | 4 | 8 | 16 | ms |

**Table 8. Watchdog Enable**

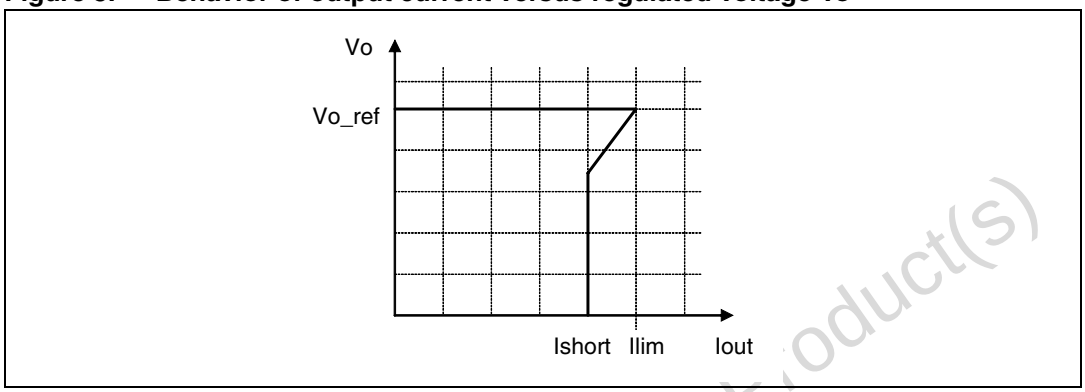
| Pin | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| WEn | $V_{WEn\_l}$ | Enable input low voltage | | | | 1 | V |
| WEn | $V_{WEn\_h}$ | Enable input high voltage | | 3 | | | V |
| WEn | $V_{WEn\_hy}$ | Enable input hysteresis | | 600 | 920 | 1300 | mV |
| WEn | I_leak | Pull down current | Vs = 13.5V | 1 | 2.5 | 5 | µA |

# 3 Application information

## 3.1 Voltage regulator

The voltage regulator uses a p-channel MOS transistor as a regulating element. With this structure a very low dropout voltage at current up to 150mA is obtained. The output voltage is regulated up to transient input supply voltage of 40V. No functional interruption due to over-voltage pulses is generated.The voltage Regulator is always active and not depending on the state of WEn input pin. A short circuit protection to GND is provided.

**Figure 3. Behavior of output current versus regulated voltage Vo**




## 3.2 Reset

The reset circuit supervises the output voltage Vo. The Vo_th reset threshold is defined with the in-ternal reference voltage and a resistor output divider. If the output voltage becomes lower than Vo_th then Res goes low with a reaction time trr. The reset low signal is guaranteed for an output voltage Vo greater than 1V.

When the output voltage becomes higher than Vo_th then Res goes high with a delay trd. This delay is obtained by an internal oscillator.

The oscillator period is given by:

$$Tosc = [(Vrhth-Vrlth) \times Ctr] / Icr + [(Vrhth-Vrlth) \times Ctr] / Idr$$

where:

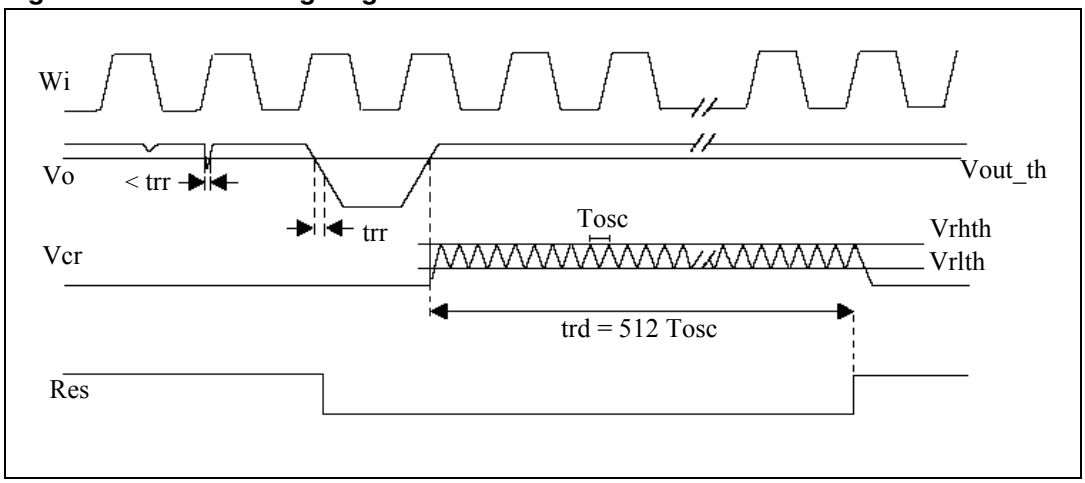
- Icr: is an internally generated charge current
- Idr: is an internally generated discharge current
- Vrhth, Vrlth: are two voltages defined with the output voltage and a resistor output divider
- Ctr: is an external capacitance.

trd is given by:

$$trd = 512 \times Tosc$$

The Reset is always active and not depending on the state of WEn input pin.

**Figure 4. Reset timing diagram**



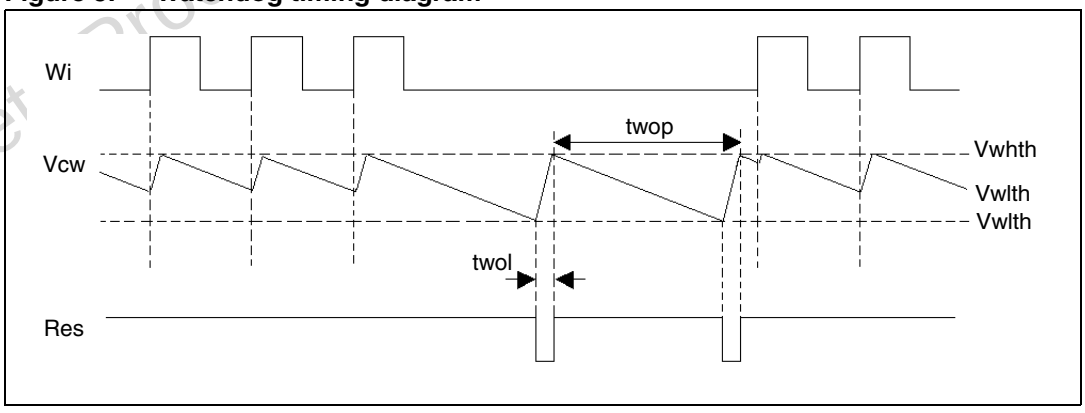

## 3.3 Watchdog

A connected microcontroller is monitored by the watchdog input Wi. If pulses are missing, the Reset output pin is set to low. The pulse sequence time can be set within a wide range with the external capacitor, Ctw. The watchdog circuit discharges the capacitor Ctw, with the constant current Icwd. If the lower threshold Vwlth is reached, a watchdog reset is generated. To prevent this the microcontroller must generate a positive edge during the discharge of the capacitor before the voltage has reached the threshold Vwlth. In order to calculate the minimum time t, during which the micro-controller must output the positive edge, the following equation can be used:

$$(Vwhth\text{-}Vwlth) \times Ctw = Icwd \times t$$

Every Wi positive edge switches the current source from discharging to charging. The same happens when the lower threshold is reached. When the voltage reaches the upper threshold, Vwhth, the current switches from charging to discharging. The result is a saw-tooth voltage at the watchdog timer capacitor Ctw.

**Figure 5. Watchdog timing diagram**



# 4 Package and packing information

## 4.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

## 4.2 SO-8 package information

**Figure 6. SO-8 package dimensions**

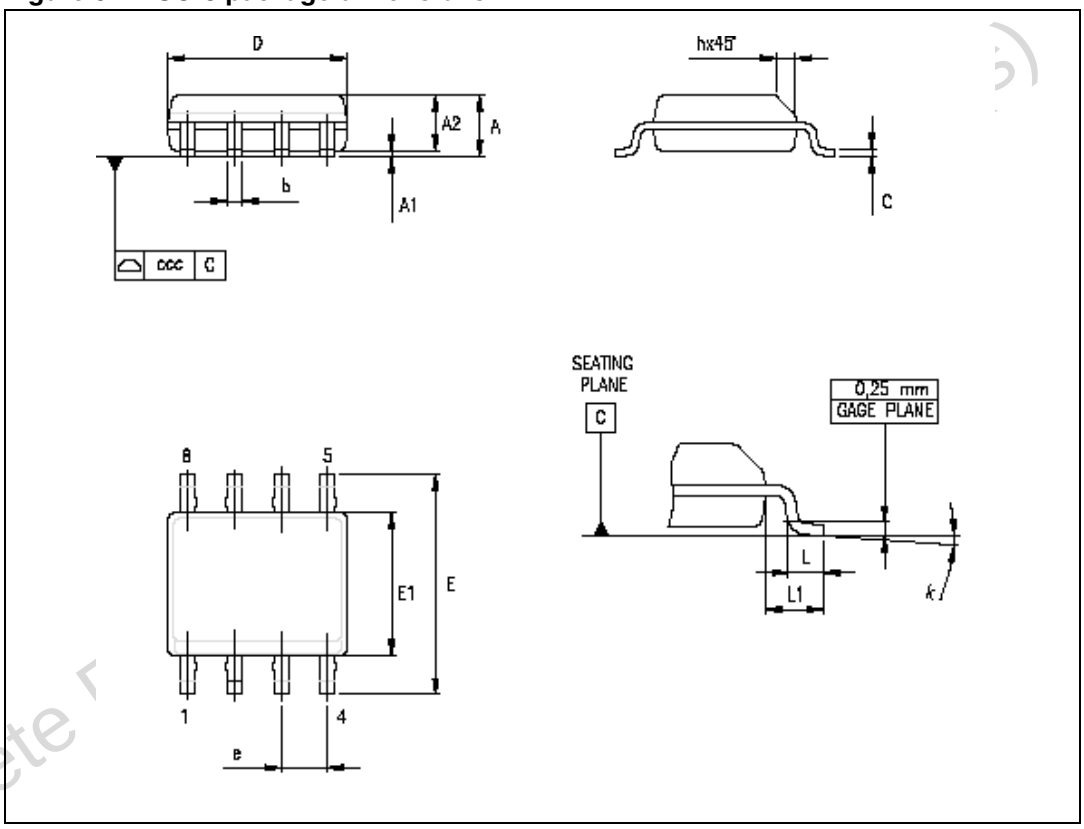


**Table 9. SO-8 mechanical data**

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | | | 1.75 |
| A1 | 0.10 | | 0.25 |
| A2 | 1.25 | | |
| b | 0.28 | | 0.48 |
| c | 0.17 | | 0.23 |
| D(1) | 4.80 | 4.90 | 5.00 |
| E | 5.80 | 6.00 | 6.20 |
| E1(2) | 3.80 | 3.90 | 4.00 |
| e | | 1.27 | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| L1 | | 1.04 | |
| k | 0° | | 8° |
| ccc | | | 0.10 |

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, potrusions or gate burrs shall not exceed 0.15mm in total (both side).
2. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

## 4.3 SO-20 package information

**Figure 7. SO-20 package dimensions**

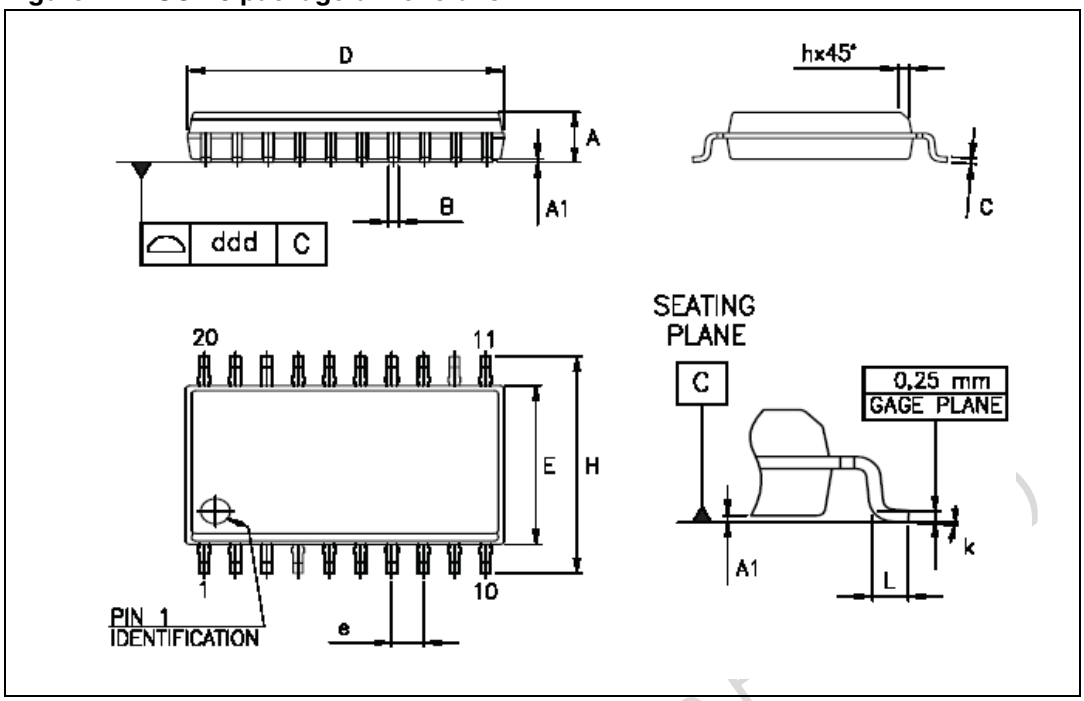


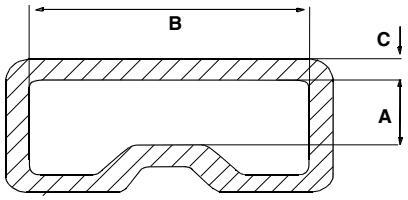

**Table 10. SO-20 mechanical data**

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 2.35 | | 2.65 |
| A1 | 0.10 | | 0.30 |
| B | 0.33 | | 0.51 |
| C | 0.23 | | 0.32 |
| D(1) | 12.60 | | 13.00 |
| E | 7.40 | | 7.60 |
| e | | 1.27 | |
| H | 10.0 | | 10.65 |
| h | 0.25 | | 0.75 |
| L | 0.40 | | 1.27 |
| k | 0° | | 8° |
| ddd | | | 0.10 |

1. “D” dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

## 4.4 SO-8 packing information

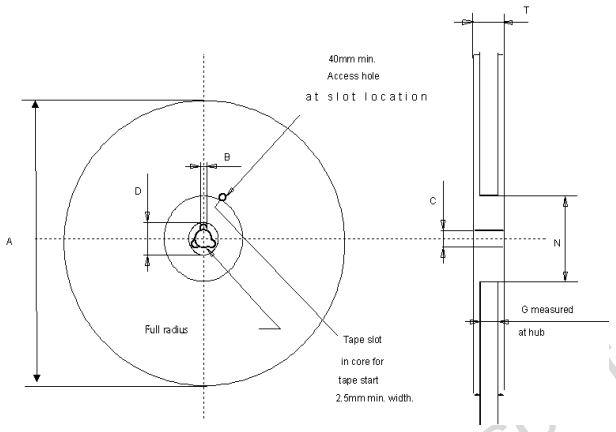
**Figure 8. SO-8 tube shipment (no suffix)**




| | |
|---|---|
| **Base Q.ty** | 100 |
| **Bulk Q.ty** | 2000 |
| **Tube length (± 0.5)** | 532 |
| **A** | 3.2 |
| **B** | 6 |
| **C (± 0.1)** | 0.6 |

All dimensions are in mm.

**Figure 9. SO-8 tape and reel shipment (suffix "TR")**




**Reel dimensions**

| | |
|---|---|
| **Base Q.ty** | 2500 |
| **Bulk Q.ty** | 2500 |
| **A (max)** | 330 |
| **B (min)** | 1.5 |
| **C (± 0.2)** | 13 |
| **F** | 20.2 |
| **G (+ 2 / -0)** | 12.4 |
| **N (min)** | 60 |
| **T (max)** | 18.4 |

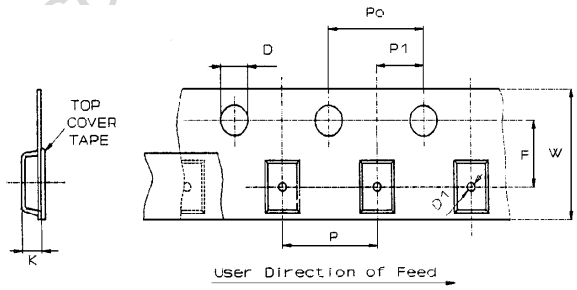
All dimensions are in mm.

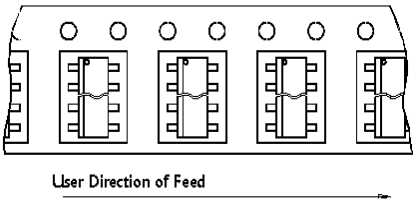
**Tape dimensions**

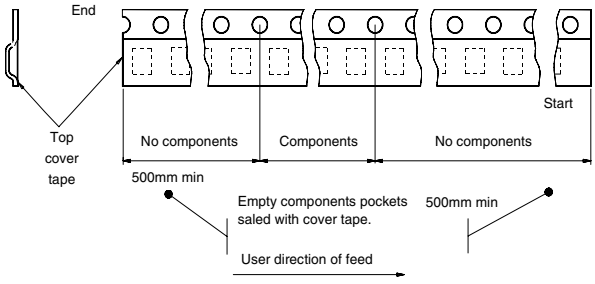
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

| | | |
|---|---|---|
| **Tape width** | **W** | 12 |
| **Tape Hole Spacing** | **P0 (± 0.1)** | 4 |
| **Component Spacing** | **P** | 8 |
| **Hole Diameter** | **D (+0.1/-0)** | 1.5 |
| **Hole Diameter** | **D1 (min)** | 1.5 |
| **Hole Position** | **F (± 0.05)** | 5.5 |
| **Compartment Depth** | **K (max)** | 4.5 |
| **Hole Spacing** | **P1 (± 0.1)** | 2 |

All dimensions are in mm.

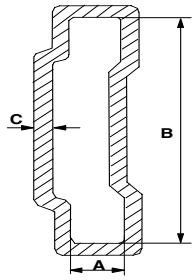


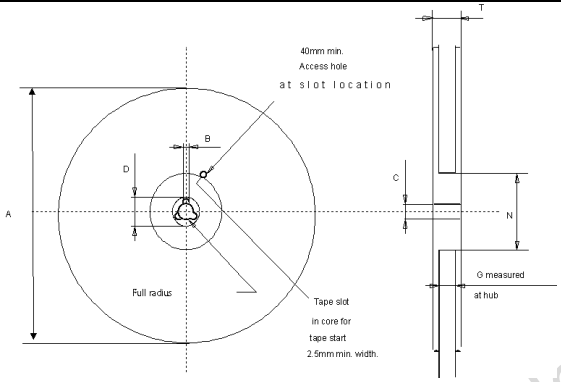
## 4.5 SO-20 packing information

**Figure 10. SO-20 tube shipment (no suffix)**




| | |
|---|---|
| **Base Q.ty** | 40 |
| **Bulk Q.ty** | 800 |
| **Tube length (± 0.5)** | 532 |
| **A** | 3.5 |
| **B** | 13.8 |
| **C (± 0.1)** | 0.6 |

**Figure 11. SO-20 tape and reel shipment (suffix "TR")**




**Reel dimensions**

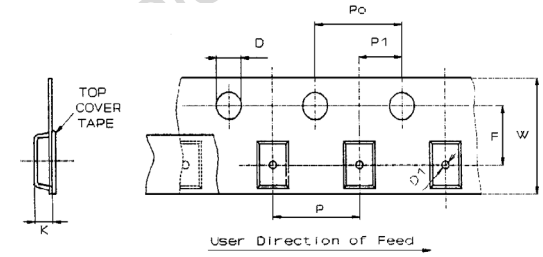
| | |
|---|---|
| **Base Q.ty** | 1000 |
| **Bulk Q.ty** | 1000 |
| **A (max)** | 330 |
| **B (min)** | 1.5 |
| **C (± 0.2)** | 13 |
| **D** | 20.2 |
| **G (+ 2 / -0)** | 24.4 |
| **N (min)** | 60 |
| **T (max)** | 30.4 |

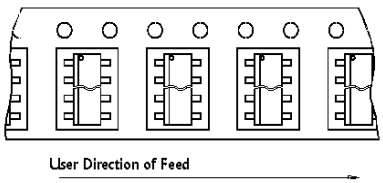
**Tape dimensions**

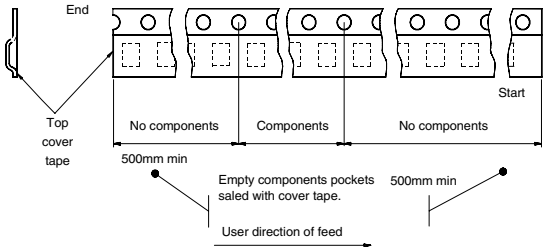
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

| | | |
|---|---|---|
| **Tape width** | **W** | 24 |
| **Tape Hole Spacing** | **P0 (± 0.1)** | 4 |
| **Component Spacing** | **P** | 12 |
| **Hole Diameter** | **D (+0.1/-0)** | 1.5 |
| **Hole Diameter** | **D1 (min)** | 1.5 |
| **Hole Position** | **F (± 0.05)** | 11.5 |
| **Compartment Depth** | **K (max)** | 6.5 |
| **Hole Spacing** | **P1 (± 0.1)** | 2 |

All dimensions are in mm.



# 5 Revision history

Table 11. Document revision history

| Date | Revision | Changes |
|---|---|---|
| Mar-2004 | 1 | Initial release |
| 13-Feb-2007 | 2 | Changed document maturity status.<br>Added *SO-8 packing information* and *SO-20 packing information*. |
| 18-Nov-2008 | 3 | Document reformatted and restructured.<br>Added *Table 1: Device summary*.<br>Added list of contents, tables and figures.<br>Added *ECOPACK® packages* information. |

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