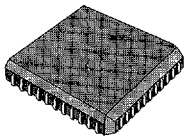
SPINDLE DRIVER

ADVANCE DATA

- 2.5A MAXIMUM PEAK CURRENT
- CONTROLLED SLEW RATE
- CENTRAL CHARGE PUMP
- PWM AND LINEAR MODES
- CUTOFF TIME USER CONFIGURABLE
- FAST, FREE-WHEELING DIODES ON CHIP
- OVER-TEMPERATURE PROTECTION
- BRAKE FUNCTION INPUT

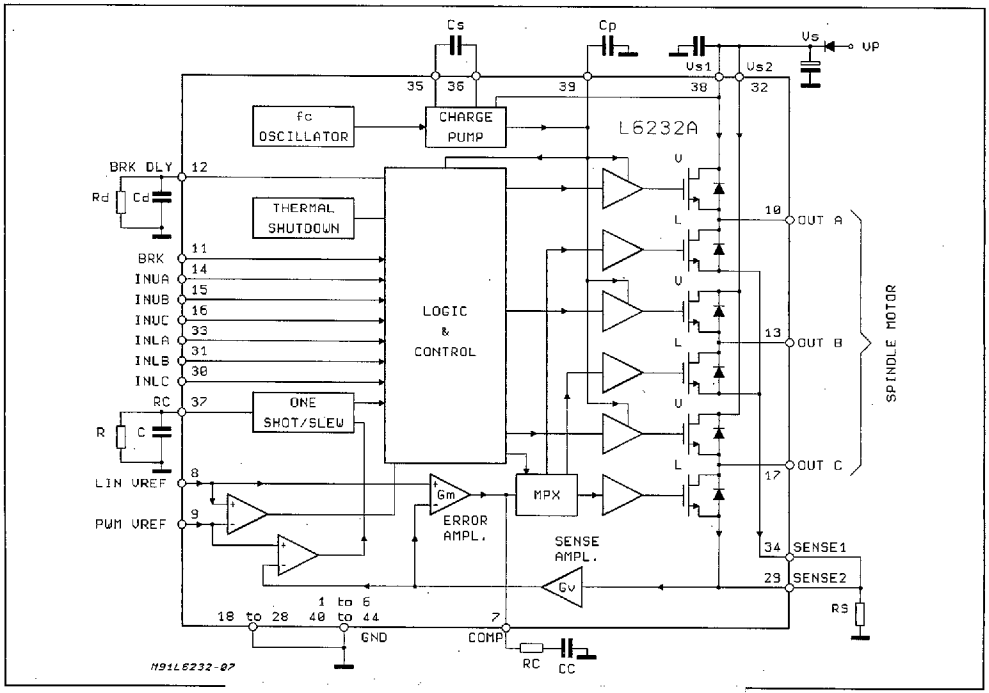


PLCC44
ORDERING NUMBER: L6232A

DESCRIPTION

The L6232A is a triple half bridge driver intended for use in brushless DC motor applications. This part can be used to form the power stage of a three-phase, brushless DC motor control loop, and is especially useful for disk drive applications. Power drivers are Integrated DMOS transistors and feature fast recirculating diodes as an integral part of their structure. The logic inputs are TTL-level compatible, with internal pull-up, allowing interfacing to open collector outputs. All necessary circuitry to perform PWM and linear motor speed control is included. A central charge pump is utilized to drive the upper DMOS transistors, and also to power the braking function. The L6232A is packaged in PLCC44.

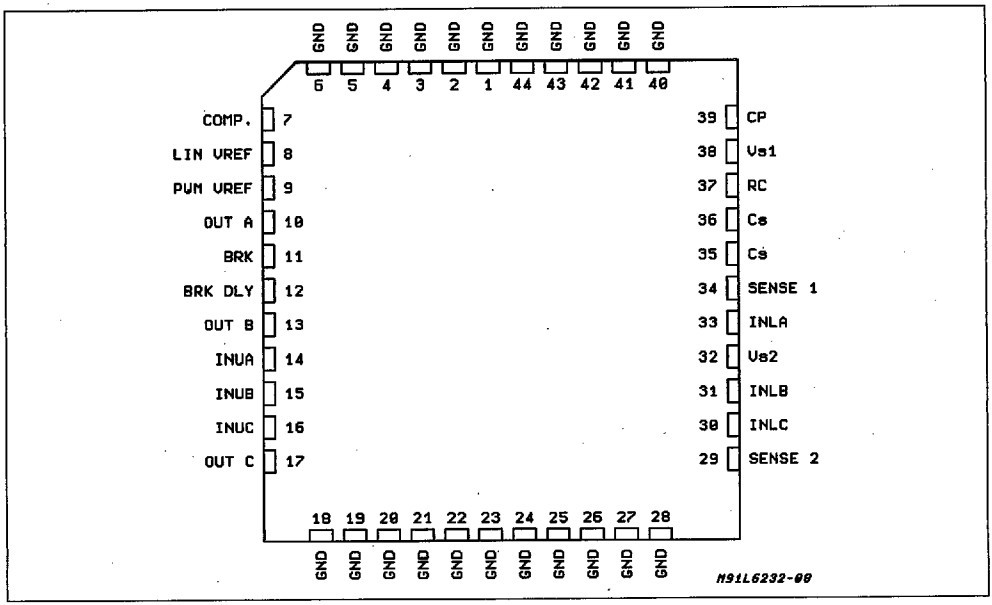
BLOCK DIAGRAM



PIN DESCRIPTION

Pin	Name	Function
1 to 6	GND	Common Ground. Also provides heat-sink to PCB.
7	COMP	External compensation for error amplifier.
8	LIN Vref	Input for Reference Control voltage in LIN mode.
9	PWM Vref	Input for Reference Control in PWM mode.
10	OUTA	DMOS Half-bridge A Out.
13	OUTB	DMOS Half-bridge B Out.
17	OUTC	DMOS Half-bridge C Out.
11	BRK	Active LOW logic input that triggers the delayed brake.
12	BRK DLY	External RC network for the brake delay.
14	INUA	Logic Inputs to turn on the upper drivers (Active Low).
15	INUB	
16	INUC	
18 to 28	GND	Common Ground. Also provides heat-sink to PCB.
29, 34	SENSE	Output for current sense resistors.
30	INLC	Logic inputs to turn on the lower drivers (Active High).
31	INLB	
33	INLA	
32, 38	V_S	Supply Voltage.
35, 36	C_S	External Charge Pump Capacitor.
37	RC	Cutoff Time RC Network in PWM mode. The Resistor value is also used to define the slew-rate in linear mode (LIN).
39	C_P	External Main Charge Pump capacitor.
40 to 44	GND	Common Ground. Also provides heat-sink to PCB.

PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{DS\ sus}$	Peak Output Sustaining Voltage	18	V
V_S	Supply Voltage	15	V
$V_{O\ peak}$	Output Peak Voltage (t_{pK} = 5 µsec; 10% d.c.)	18	V
V_{Cp}	Charge Pump Input Voltage	30	V
V_i	Logic Input Voltage	-0.3 to 7	V
V_{REF}	PWM VREF--LIN VREF Input Voltage	-0.3 to 7	V
V_{is}	Sense Input Voltage	-1 to 7	V
I_p	Sink-Source Peak Output Current(*)	3.5	A
I_O	Sink-Source DC Output Current	2.5	A
P_{tot}	Total Power Dissipation (T_{amb} = 60°C)	1.8	W
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}pin}$	Thermal Resistance Junction-pins	Max.	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient (**)	Max.	50	°C/W

Notes
(*) Pulse width limited only by junction temperature and by the transient thermal resistance
(**) Mounted on board with minimized dissipating copper area

ELECTRICAL CHARACTERISTICS (See the block diagram, V_S =12V, R = 100KΩ; C = 180pF; T_j = 25°C, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		10.5	12	13.5	V
I_S	Quiescent Supply Current	BRK = L; INUA = INUB = INUC = L; INLA = INLB = INLC = H; Table 1		0.3	0.5	mA
		BRK = H; INUA = INUB = INUC = H; INLA = INLB = INLC = L; Table 1		4	6	mA
I_{OL}	Output Leakage Current	V_O = V_S = 13.5V			1	mA
R_{DSon}	Sink Out ON Resistance	T_j = 25°C (see Fig.4)		0.42	0.47	Ω
		T_j = 125°C		0.7		Ω
R_{DSon}	Source Out ON Resistance	T_j = 25°C (see Fig.4)		0.42	0.47	Ω
		T_j = 125°C		0.7		Ω
V_F	Body Diode Forward Drop (sink and source)	I_{DS} = 1A (see Fig. 6)		1	1.5	V
$t_{d(BRK)}$	Brake Delay Time	See Fig. 1, 3; note1		210		ms
T_{BRK}	Braking Time		10			s
$I_{B(LIN)}$	LIN Vref Input Bias Current	LIN V_{ref} = 0.4 to 5.5V		400	800	nA
$I_{B(PWM)}$	PWM Vref Input Bias Current	PWM V_{ref} = 0.4 to 5.5V		400	800	nA
LIN V_{ref}	Reference Voltage Input	Note 2; R_S = 0.5Ω I_{motor} (PWM) = 1A I_{motor} (LIN) = 200mA		2		V
PWM V_{ref}				0.4		V
G_v	Sense Amplifier Voltage Gain	PWM V_{ref} = 2.5V, LIN V_{ref} = 0.4V, R_S = 0.5Ω; Note 2	3.8	4	4.2	V/V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_m	LIN Error Amplifier Transconductance			0.8		mA/V
Zout	Error Amplifier Output Impedance			2		MΩ
V_{INH}	Logic Input Voltage BRK; INUA; INUB; INUC; INLA; INLB; INLC		2			V
V_{INL}					0.8	V
$I_{INH(leak)}$	Logic Input Current BRK; INUA; INUB; INUC; INLA; INLB; INLC	V_i = 2.7V			-1	mA
I_{INL}		V_i = 0.4V			-0.1	mA
t_{donU}	Upper/Lower Turn-on Delay	Table 1 see Fig. 3		0.7		µs
t_{donL}				0.15		µs
t_{doffU}	Upper/Lower Turn-off Delay			15		µs
t_{doffL}				0.5		µs
dV/dt	Source DMOS Slew-Rate (PWM)	see Fig. 3	10			V/µs
dV/dt	Source DMOS Slew-Rate (LIN)	see Fig. 3			1	V/µs
dV/dt	Sink DMOS Output Turn-off Slew-Rate	Note 3; R = 100KΩ		0.1		V/µs
F_C	Internal Clock Frequency			380		KHz
T_{off}	PWM Cutoff Time	R=100KΩ; C=180pF, Note 4; see Fig. 2		12		µs
T_{sd}	Shutdown Temperature			160		°C
T_{sdr}	Recovery Temperature			120		°C

Notes:

1) The Head Park time must be shorter than the Brake Delay time $t_{d(BRK)} = R_d C_d$
2) Both in PWM and in LIN mode the Ref. Voltage must agree to $V_{ref}=G_V R_S I_{motor}$
3) The resistance of the RC network defines the dv/dt value.
4) $t_{off} = 1.8RC + 6 \cdot 10^{-8}$

Table 1

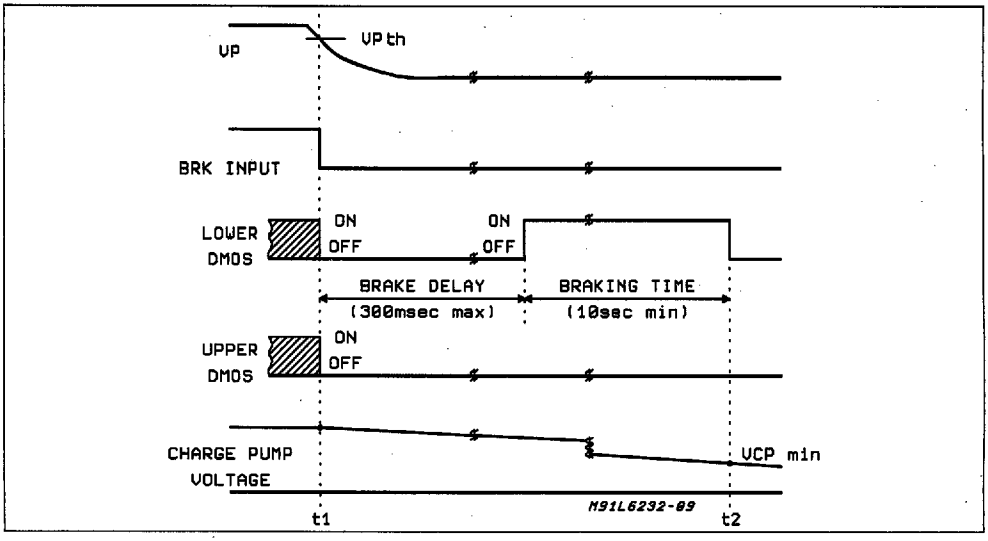
INPUT STATE						OUTPUT STATE		
INUA	INUB	INUC	INLA	INLB	INLC	A	B	C
L	L	L	H	H	H	*	*	*
L	L	L	L	L	L	H	H	H
H	H	H	L	L	L	*	*	*
H	H	H	H	H	H	L	L	L

H = The Upper DMOS is ON

L = The Lower DMOS is ON

* = Tristate condition

Figure 1: Brake Delay and Braking timing of the L6232A. At the time t1 a VP Powerdown threshold detector drives low the BRK input; at time t2 the Charge Pump voltage becomes inadequate to maintain ON the lower DMOS.



FUNCTIONAL DESCRIPTION (Refer to the Block Diagram)

The commutation sequence is provided by the user via six inputs. INUA,INUB,INUC turn on the three upper DMOS drivers when held at logic LOW, and inputs INLA,INLB,INLC turn on the three lower DMOS drivers when held at logic HIGH.

The BRK and BRK DLY inputs offer flexibility to the system designer in the implementation of the braking function. The BRK logic input, when pulled low will turn-off all upper and lower Dmos drivers. The low transition at BRK will produce a delayed negative transition at the BRK DLY input, configurable by connection of a capacitor Cd and a resistor Rd from the BRK DLY pin to ground. The negative transition at BRK DLY will initiate the braking of the motor by turning on all lower Dmos, while keeping all upper DMOS turned-off. This feature provides a time interval where the motor BEMF can be used to power the head parking function before the braking procedure is iniziated. External detection of the supply(VP) drop-off is necessary to provide the appropriate logic signal to the BRK input. (see Fig. 1)

The brake function utilizes the energy stored in the central charge pump capacitor (Cp) to turn-on or turn-off the DMOS drivers. This allows for completion of the braking procedure after the VP supply has powered down.

The L6232A is capable of driving the motor in either pulse width modulation (PWM) or linear (LIN) mode. The driving mode is determined by the smaller of two analog voltages inputs, LIN Vref and PWM Vref. The motor current is controlled by LIN Vref and PWM Vref and the current sense resistor Rs connected to the SENSE output. The SENSE output provides for connection of a resistor in series with the source of all lower DMOS drivers. The voltage at this pin provides the error signal wich is utilized internally to regulate the motor current Im. The current in both PWM and linear mode is determined by the expression :

$$I_m = \frac{V_{ref}}{G_V \cdot R_S}$$

in wich Gv is the voltage gain of the sense amplifier. In linear mode, the current is regulated by a linear control loop wich drives the lower DMOS. Compensation of the linear control loop is achieved by connection of a series network (Rc,Cc) from the transconductance amplifier output (Gm) and ground. Control is passed to each lower DMOS in succession during the commutation sequence(MPX).

The rate at which the upper and lower drivers turns-off during linear mode operation is configurable externally by the value of the resistor R used at the RC pin. This defines a current which is utilized internally to limit the voltage slew-rate at the outputs during transitions. The output slew-rate is internally adjusted for fast slewing during PWM operation to reduce losses, and a relatively slower rate during linear mode operation to mi-

nimize noise effects(EMI). LIN Vref and PWM Vref are connected to a comparator whose output is fed to the logic . The upper and lower DMOS driver slew-rates are controlled by the internal logic.

In PWM mode, the upper driver is turned-off when the motor current reaches the intended value. An internal One-Shot pulse determines the lenght of time the upper driver stays off before turning on again. The pulse width, and thus the cutoff time (toff), is configurable by means of the external RC network connected to the RC pin. (see Fig. 2). The resistor at the RC pin, therefore determines both the driver output slew-rate during linear mode and the off-time constant during PWM. The lower driver is always on during PWM mode of operation; an on-chip 2µs mask can prevent the beginning of a new cutoff time because of transient current spikes caused by the upper drivers turn-on.

The driving mode is determined by the smaller of the two controlling input voltages. In a typical application the motor start-up would occur in PWM mode to limit power dissipation, with on-speed control then performed in linear mode.

Thermal protection circuitry will shut-off all drivers when the chip junction temperature exceeds the threshold temperature. A small amount of hysteresis is included to prevent rapid on/off cycling of the power stages.

Additional protection is provided against driver input combinations where the upper and lower drivers of a half bridge are turned on simultaneusly, resulting in a short from supply to ground. The chip logic will cause both the upper and lower drivers involved to turn-off. (see Table 1)

APPLICATION INFORMATION

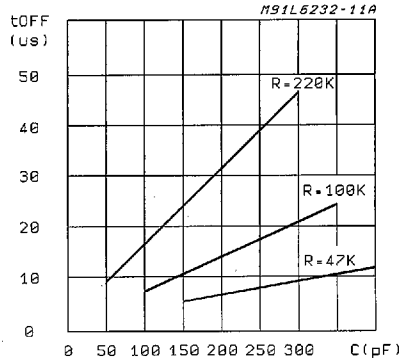
A typical application configuration of the L6232A driving a three-phase brushless DC motor is shown in Fig.3. The spindle motor is a 4 ohm-2mH per phase, star connected. This load requires a suitable compensation of the linear control loop that can be achieved by Rc= 10 Kohm and Cc= 10nF (R3;C8). Changing the motor characteristics, the RcCc network would be modified for the best performances of the system. At the start-up the spindle is driven in PWM mode fixed toff time.

The off-time is calculated by the formula :

$$toff = 0.69\ R2\ C7$$

See fig.2 for a quick choice of the needed capacitor, after the resistor has been fixed. The value of the resistor defines the rate at which the upper and lower drivers turn-off during linear mode operation to avoid EMI effects. During turn-off, the slew rate is constant for the sink stage, while it has a varying slope for the source stage because of the non linear change of the gate to source impedance of the DMOS transistor. Practically, the

Figure 2: Typical t_{off} vs. Capacity of C



slowest slew rate is obtained at the sink transistor switch-off time (see fig. 5), then it increases during the first period of the source transistor switch-off (source,1st) and it becomes the fastest during the final portion of the turn-off duration (source, 2nd). The PWM to linear mode of operation is switched by decreasing the LIN Vref level under the PWM Vref value that could be fixed and calculated by:

$$PWM\ Vref = 4\ Rs\ Ip$$

where Ip is the peak chopping current in the motor windings. Of course, when the required RPM is reached, it become of no need a strong torque and the LIN Vref starting from a value higher than the calculated PWM Vref, decreases to the value :

$$LIN\ Vref = 4\ Rs\ Im$$

where Im, smaller than Ip, is the needed motor current to keep constant spin. This last reference voltage is generally a PLL output driven by speed transducers coupled to the spindle (like Hall effect sensors or BEMF processors). To drive the upper DMOS and during the brake function a voltage higher than the supply Vs is needed. The charge pump integrated in the L6232A keeps C3 at the correct voltage. To guarantee efficient braking of the motor , C3 must be chosen of adeguate quality (very high equivalent parallel resistance). C4 can be a ceramic disk capacitor . The typical application od the L6232A is in HDD systems on which there is the need to park the Read-Write Heads before the motor braking. This behavior is possible with the circuit of Fig.3. At Power Supply switch-off (see Fig. 1), VP falls down and drives down the BRK input (Active Low). D1 insulates the L6232A from the power suppy output while the power output stage is switched in a high impedance state. The spindle motor acting as a three-phase alternator supplies the Heads voice coil motor driven through integrated diodes that rectifie the EMF. After a delay longer than the parking time, the lower output DMOS are switched-on and the spindle motor is braked. The brake delay time is tipically

150 msec and it is defined by :

$$td(BRK) = 1.4\ R1\ C6$$

The sensing resistor value is generally lower than 1ohm, but a wire wounded type must be avoided. In Fig.3 the 0.33 ohm sensing resistor is shown as three parallel 1ohm metal film resistors. Care must be taken in the PC Board design particularly about ground loops and ground copper area. The typical Thermal Resistance junction to ambient versus PC Board copper area (Fig.7) is shown in Fig 8. For Transient Thermal Resistance see Fig. 9.

Figure 3: Typical Application Circuit

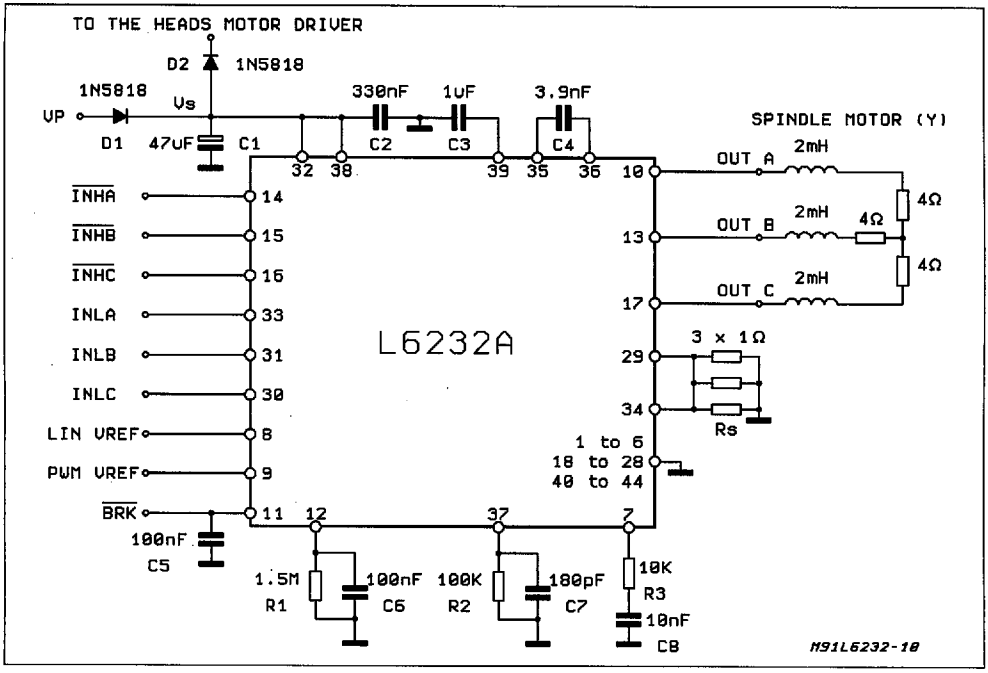


Figure 4: Typical Normalized $R_{DS\,(on)}$ vs. Junction Temperature

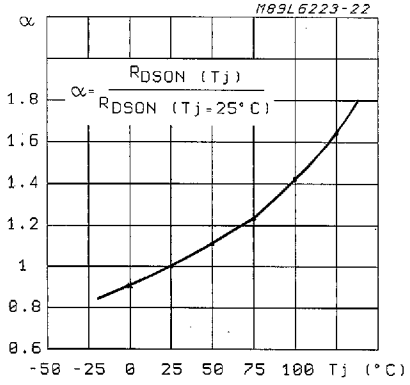


Figure 5: Output Voltage Slew Rate Control vs. $1/R_2$ Value

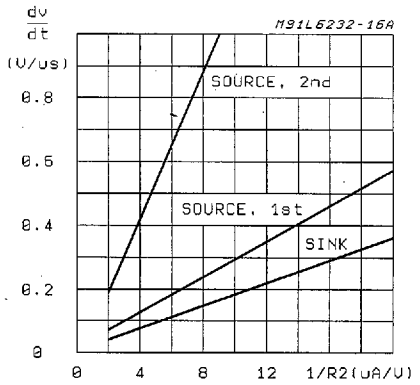


Figure 6: Typical Body Diode Forward Drop vs. Drain to Source Current.

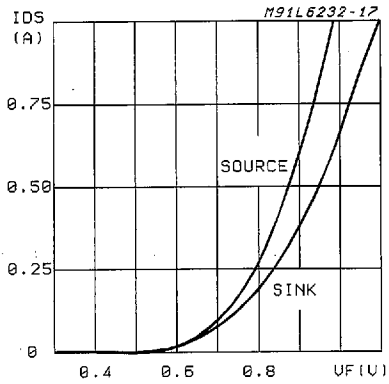


Figure 7: On Board Dissipation Copper Area Size

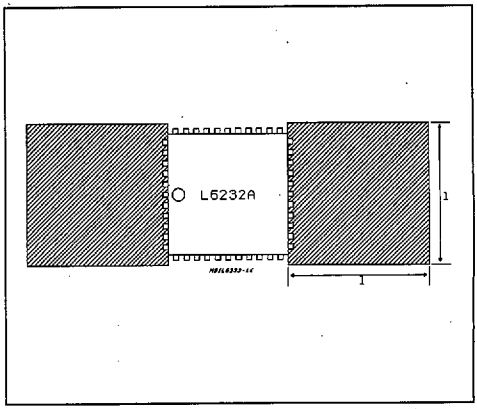


Figure 8: Typical $R_{th\ j\text{-}amb}$ vs. On-Board Heatsink Side l.

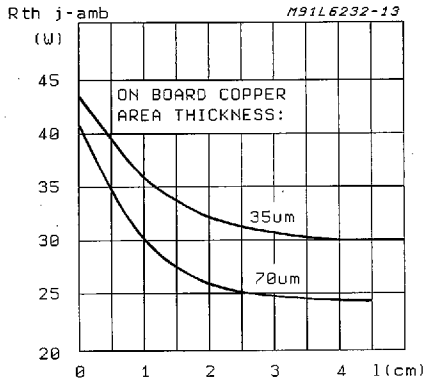


Figure 9: Typical Transient R_{th} in Single Pulse Condition.