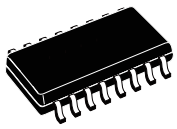
L6390

High voltage high/low-side driver

Datasheet - production data



SO-16

Features

- High voltage rail up to 600 V
- dV/dt immunity ± 50 V/nsec in full temperature range
- Driver current capability: 290 mA source, 430 mA sink
- Switching times 75/35 nsec rise/fall with 1 nF load
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Integrated bootstrap diode
- Operational amplifier for advanced current sensing
- Comparator for fast fault protection
- Smart shutdown function
- Adjustable deadtime
- Interlocking function
- Compact and simplified layout
- Bill of material reduction

Applications

- Home appliances
- Motor drivers
  - DC, AC, PMDC and PMAC motors
  - FOC and sensorless BEMF detection systems
- Industrial applications and drives
- Induction heating
- HVAC
- Factory automation
- Power supply systems

Description

The L6390 is a full featured high voltage device manufactured with the BCD ™ "offline" technology. It is a single-chip half-bridge gate driver for N-channel power MOSFETs or IGBTs. The high-side (floating) section is able to work with voltage rail up to 600 V.

Both device outputs can sink and source 430 mA and 290 mA respectively. Prevention from cross conduction is ensured by interlocking and programmable deadtime functions.

The device has dedicated input pins for each output and a shutdown pin. The logic inputs are CMOS/TTL compatible down to 3.3 V for easy interfacing with control devices. Matched delays between low-side and high-side sections guarantee no cycle distortion and allow high frequency operation.

The L6390 embeds an operational amplifier suitable for advanced current sensing in applications such as field oriented motor control or for sensorless BEMF detection. A comparator featuring advanced smartSD function is also integrated in the device, ensuring fast and effective protection against fault events like overcurrent, overtemperature, etc.

The L6390 device features also UVLO protection on both the lower and upper driving sections, preventing the power switches from operating in low efficiency or dangerous conditions.

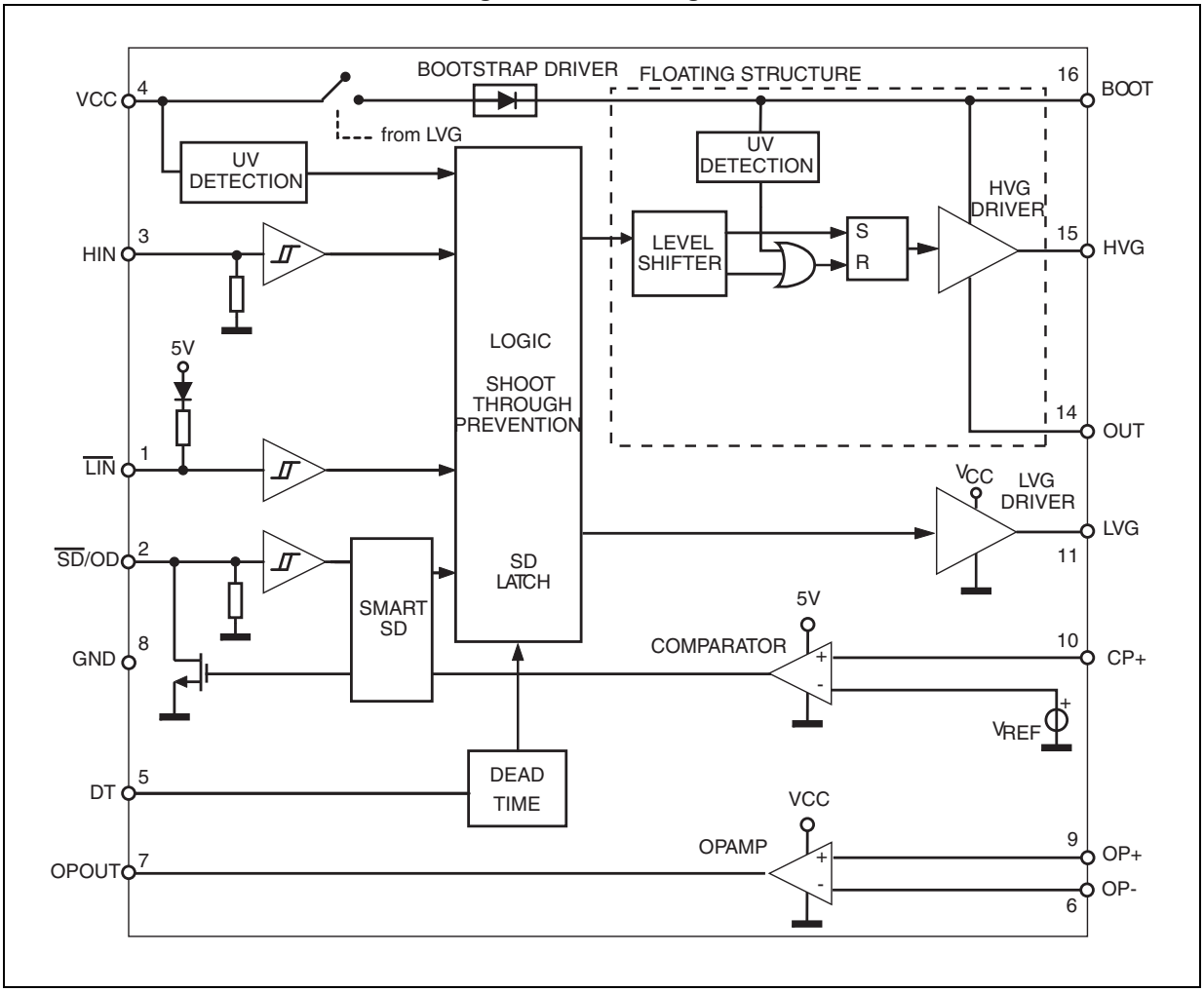
The integrated bootstrap diode as well as all of the integrated features of this IC make the application PCB design easier, more compact and simple thus reducing the overall bill of material.

The device is available in an SO-16 tube and tape and reel packaging options.

Contents

1 Block diagram

Figure 1. Block diagram



2 Pin connection

Figure 2. Pin connection (top view)

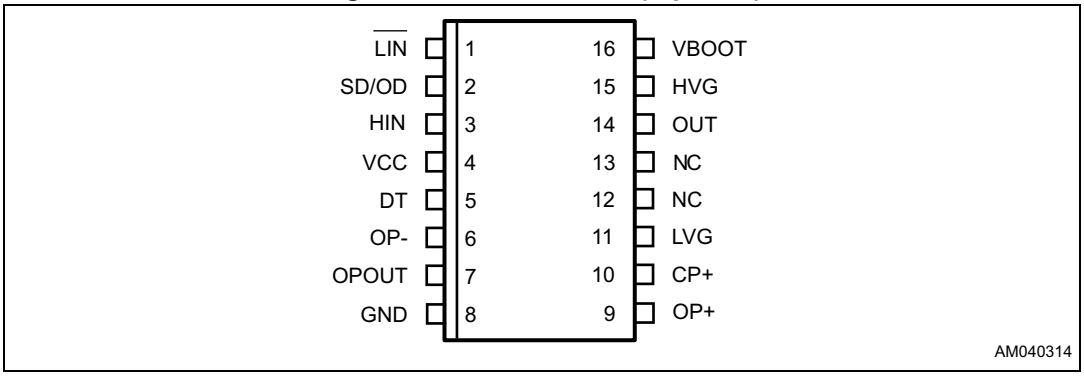


Table 1. Pin description

Pin no.	Pin name	Type	Function
1	$\overline{\text{LIN}}$	I	Low-side driver logic input (active low)
2	$\overline{\text{SD}}$/OD (1)	I/O	Shutdown logic input (active low)/open drain (comparator output)
3	HIN	I	High-side driver logic input (active high)
4	VCC	P	Lower section supply voltage
5	DT	I	Deadtime setting
6	OP-	I	Op amp inverting input
7	OPOUT	O	Op amp output
8	GND	P	Ground
9	OP+	I	Op amp non-inverting input
10	CP+	I	Comparator input
11	LVG (1)	O	Low-side driver output
12, 13	NC		Not connected
14	OUT	P	High-side (floating) common voltage
15	HVG (1)	O	High-side driver output
16	BOOT	P	Bootstrap supply voltage

1. The circuit provides less than 1 V on the LVG and HVG pins (at I_{sink} = 10 mA), with V_{CC} > 3 V. This allows the omission of the “bleeder” resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low; the gate driver assures low impedance also in SD condition.

3 Electrical data

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min.	Max.	
V_{CC}	Supply voltage	- 0.3	21	V
V_{OUT}	Output voltage	V_{BOOT} - 21	V_{BOOT} + 0.3	V
V_{BOOT}	Bootstrap voltage	- 0.3	620	V
V_{hvg}	High-side gate output voltage	V_{OUT} - 0.3	V_{BOOT} + 0.3	V
V_{lvg}	Low-side gate output voltage	- 0.3	V_{CC} + 0.3	V
V_{OP+}	Op amp non-inverting input	- 0.3	V_{CC} + 0.3	V
V_{OP-}	Op amp inverting input	- 0.3	V_{CC} + 0.3	V
V_{CP+}	Comparator input voltage	- 0.3	V_{CC} + 0.3	V
V_i	Logic input voltage	- 0.3	15	V
V_{od}	Open drain voltage	- 0.3	15	V
dV_{OUT}/dt	Allowed output slew rate	-	50	V/ns
P_{tot}	Total power dissipation (T_A = 25 °C)	-	800	mW
T_J	Junction temperature	-	150	°C
T_{stg}	Storage temperature	-50	150	°C
ESD	Human body model	2		kV

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	SO-16	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient	120	°C/W

3.3 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Pin	Parameter	Test condition	Min.	Max.	Unit
V_{CC}	4	Supply voltage	-	12.5	20	V
V_{BO}(1)	16 - 14	Floating supply voltage	-	12.4	20	V
V_{OUT}	14	DC output voltage	-	- 9(2)	580	V
f_{sw}	-	Switching frequency	HVG, LVG load C_L = 1 nF	-	800	kHz
T_J	-	Junction temperature	-	-40	125	°C

1. $V_{BO} = V_{BOOT} - V_{OUT}$.
2. LVG off. V_{CC} = 12.5 V. Logic is operational if V_{BOOT} > 5 V. Refer to the AN2738 for more details.

4 Electrical characteristics

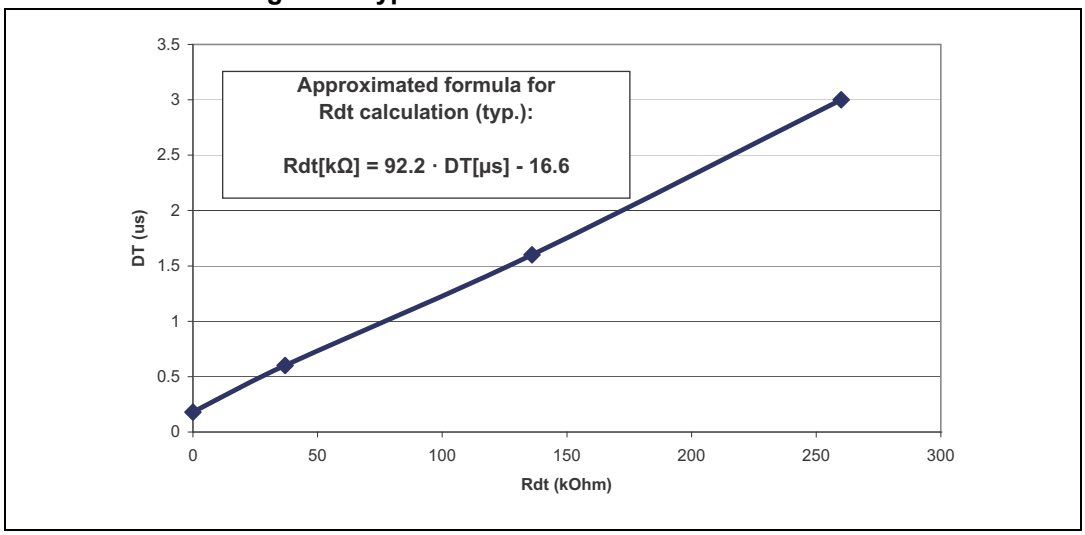
4.1 AC operation

Table 5. AC operation electrical characteristics (V_{CC} = 15 V; T_J = +25 °C)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{on}	1 vs. 11 3 vs. 15	High/low-side driver turn-on propagation delay	V_{OUT} = 0 V V_{BOOT} = V_{CC} C_L = 1 nF V_i = 0 to 3.3 V See *Figure 4 on page 12*	50	125	200	ns
t_{off}		High/low-side driver turn-off propagation delay		50	125	200	ns
t_{sd}	2 vs. 11, 15	Shutdown to high/low-side driver propagation delay		50	125	200	ns
t_{isd}	-	Comparator triggering to high/low-side driver turn-off propagation delay	Measured applying a voltage step from 0 V to 3.3 V to pin CP+.	50	200	250	ns
MT	-	Delay matching, HS and LS turn-on/off	-	-	-	30	ns
DT	5	Deadtime setting range(1)	R_{DT} = 0, C_L = 1 nF	0.1	0.18	0.25	µs
			R_{DT} = 37 kΩ, C_L = 1 nF, C_{DT} = 100 nF	0.48	0.6	0.72	µs
			R_{DT} = 136 kΩ, C_L = 1 nF, C_{DT} = 100 nF	1.35	1.6	1.85	µs
			R_{DT} = 260 kΩ, C_L = 1 nF, C_{DT} = 100 nF	2.6	3.0	3.4	µs
MDT	-	Matching deadtime(2)	R_{DT} = 0, C_L = 1 nF	-	-	80	ns
			R_{DT} = 37 kΩ, C_L = 1 nF, C_{DT} = 100 nF	-	-	120	ns
			R_{DT} = 136 kΩ, C_L = 1 nF, C_{DT} = 100 nF	-	-	250	ns
			R_{DT} = 260 kΩ, C_L = 1 nF, C_{DT} = 100 nF	-	-	400	ns
t_r	11, 15	Rise time	C_L = 1 nF	-	75	120	ns
t_f		Fall time	C_L = 1 nF	-	35	70	ns

1. See *Figure 3*.
2. MDT = | DT_{LH} - DT_{HL} | see *Figure 6 on page 13*.

Figure 3. Typical deadtime vs. DT resistor value



4.2 DC operation

Table 6. DC operation electrical characteristics (V_{CC} = 15 V; T_J = + 25 °C)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Low supply voltage section							
V_{CC_hys}	4	V_{CC} UV hysteresis	-	1200	1500	1800	mV
V_{CC_thON}		V_{CC} UV turn-ON threshold	-	11.5	12	12.5	V
V_{CC_thOFF}		V_{CC} UV turn-OFF threshold	-	10	10.5	11	V
I_{QCCU}		Undervoltage quiescent supply current	V_{CC} = 10 V $\overline{SD}$ = 5 V; $\overline{LIN}$ = 5 V; HIN = GND; R_{DT} = 0 Ω; CP+ = OP+ = GND; OP- = 5 V	90	120	150	µA
I_{QCC}		Quiescent current	V_{CC} = 15 V $\overline{SD}$ = 5 V; $\overline{LIN}$ = 5 V; HIN = GND; R_{DT} = 0 Ω; CP+ = OP+ = GND; OP- = 5 V	300	720	1000	µA
V_{ref}	-	Internal reference voltage	-	500	540	580	mV
Bootstrapped supply voltage section(1)							
V_{BO_hys}	16	V_{BO} UV hysteresis	-	1200	1500	1800	mV
V_{BO_thON}		V_{BO} UV turn-ON threshold	-	11.1	11.5	12.1	V
V_{BO_thOFF}		V_{BO} UV turn-OFF threshold	-	9.8	10	10.6	V
I_{QBOU}		Undervoltage V_{BO} quiescent current	V_{BO} = 9 V $\overline{SD}$ = 5 V; $\overline{LIN}$ and HIN = 5 V; R_{DT} = 0 Ω; CP+ = OP+ = GND; OP- = 5 V	30	70	110	µA
I_{QBO}		V_{BO} quiescent current	V_{BO} = 15 V $\overline{SD}$ = 5 V; $\overline{LIN}$ and HIN = 5 V; R_{DT} = 0 Ω; CP+ = OP+ = GND; OP- = 5 V	30	150	240	µA
I_{LK}	-	High voltage leakage current	V_{hvg} = V_{OUT} = V_{BOOT} = 600 V	-	-	10	µA
$R_{DS(on)}$	-	Bootstrap driver on-resistance(2)	LVG ON	-	120	-	Ω

Table 6. DC operation electrical characteristics (V_{CC} = 15 V; T_J = + 25 °C) (continued)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Driving buffers section							
I_{so}	11, 15	High/low-side source short-circuit current	$V_{IN} = V_{ih}$ (t_p < 10 µs)	200	290	-	mA
I_{si}		High/low-side sink short-circuit current	$V_{IN} = V_{il}$ (t_p < 10 µs)	250	430	-	mA
Logic inputs							
V_{il}	1, 2, 3	Low level logic threshold voltage	-	0.8	-	1.1	V
V_{ih}		High level logic threshold voltage	-	1.9	-	2.25	V
V_{il_S}	1, 3	Single input voltage	$\overline{LIN}$ and HIN connected together and floating	-	-	0.8	V
I_{HINh}	3	HIN logic “1” input bias current	HIN = 15 V	110	175	260	µA
I_{HINl}		HIN logic “0” input bias current	HIN = 0 V	-	-	1	µA
I_{LINl}	1	$\overline{LIN}$ logic “0” input bias current	$\overline{LIN}$ = 0 V	3	6	20	µA
I_{LINh}		$\overline{LIN}$ logic “1” input bias current	$\overline{LIN}$ = 15 V	-	-	1	µA
I_{SDh}	2	$\overline{SD}$ logic “1” input bias current	$\overline{SD}$ = 15 V	10	40	100	µA
I_{SDl}		$\overline{SD}$ logic “0” input bias current	$\overline{SD}$ = 0 V	-	-	1	µA
R_{PD_SD}	2	$\overline{SD}$ input pull-down resistor	$\overline{SD}$ = 15 V	150	375	1500	kΩ

1. $V_{BO} = V_{BOOT} - V_{OUT}$.
2. R_{DSON} is tested in the following way: $R_{DSON} = [(V_{CC} - V_{BOOT1}) - (V_{CC} - V_{BOOT2})] / [I_1(V_{CC},V_{BOOT1}) - I_2(V_{CC},V_{BOOT2})]$ where I_1 is the pin 16 current when $V_{BOOT} = V_{BOOT1}$, I_2 when $V_{BOOT} = V_{BOOT2}$.

Table 7. Op amp characteristics[1] (V_{CC} = 15 V, T_J = +25 °C)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{io}	6, 9	Input offset voltage	V_{ic} = 0 V, V_o = 7.5 V	-	-	6	mV
I_{io}		Input offset current	V_{ic} = 0 V, V_o = 7.5 V	-	4	40	nA
I_{ib}		Input bias current[2]		-	100	200	nA
V_{icm}		Input common mode voltage range	-	0	-	V_{CC}-4	V
V_{OPOUT}	7	Output voltage swing	OPOUT = OP-; no load	0.07	-	V_{CC}-4	V
I_o		Output short-circuit current	Source, V_{id} = +1; V_o = 0 V	16	30	-	mA
			Sink,V_{id} = -1; V_o = V_{CC}	50	80	-	mA
SR	-	Slew rate	V_i = 1 ÷ 4 V; C_L = 100 pF; unity gain	2.5	3.8	-	V/µs
GBWP	-	Gain bandwidth product	V_o = 7.5 V	8	12	-	MHz
A_{vd}	-	Large signal voltage gain	R_L = 2 kΩ	70	85	-	dB
SVR	-	Supply voltage rejection ratio	vs. V_{CC}	60	75	-	dB
CMRR	-	Common mode rejection ratio	-	55	70	-	dB

1. The operational amplifier is disabled when V_{CC} is in UVLO condition.
2. Input bias current flows out the IC leads.

Table 8. Sense comparator characteristics[1] (V_{CC} = 15 V, T_J = +25 °C)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{ib}	10	Input bias current	V_{CP+} = 1 V	-	-	1	µA
V_{OL}	2	Open drain low level output voltage	I_{OD} = - 3 mA	-	-	0.5	V
R_{ON_OD}	2	Open drain ON resistor	-	-	125	167	Ω
t_{d_comp}	-	Comparator delay	$\overline{SD}$/OD pulled to 5 V through 100 kΩ resistor	-	90	130	ns
SR	2	Slew rate	C_L = 180 pF; R_{pu} = 5 kΩ	-	60	-	V/µs

1. The comparator is disabled when V_{CC} is in UVLO condition.

5 Timing and waveforms definitions

Figure 4. Propagation delay timing definition

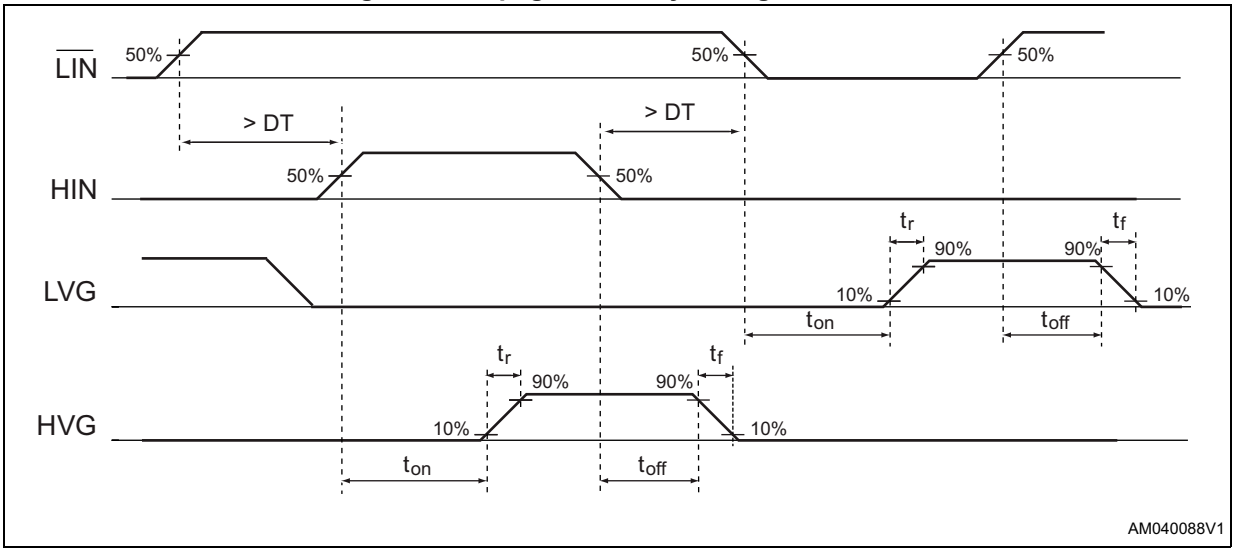


Figure 5. Dead time and interlocking timing definitions

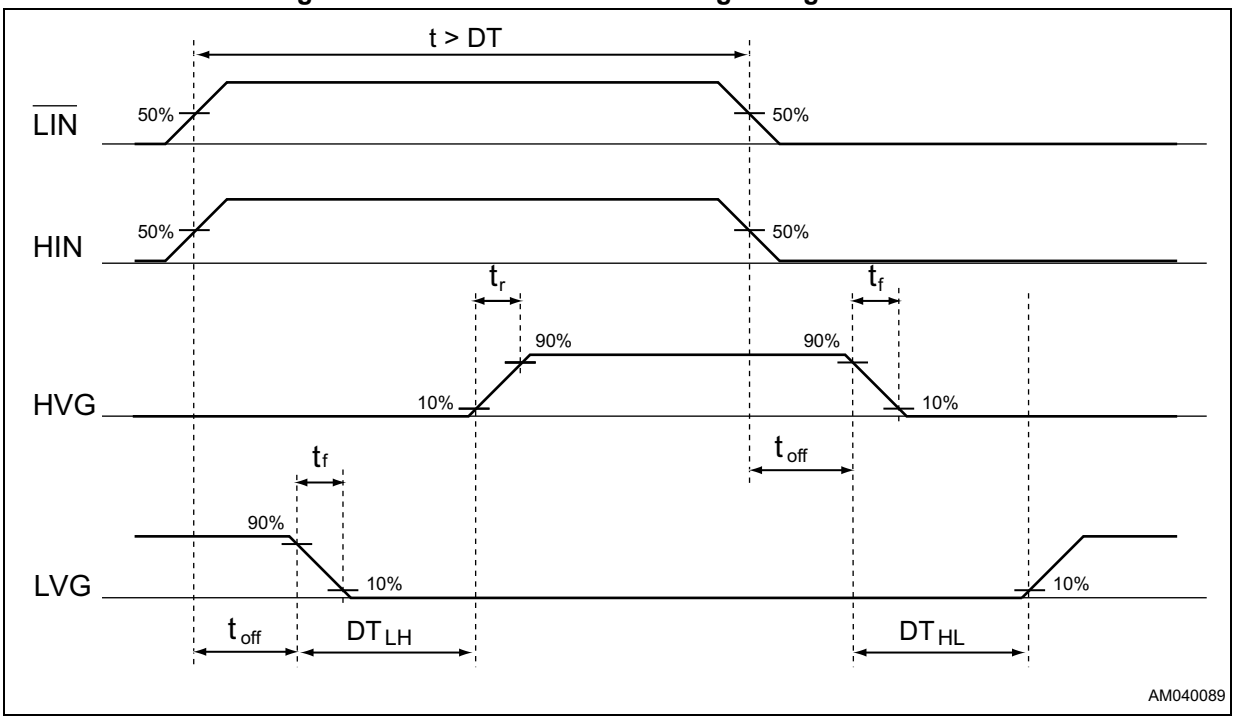
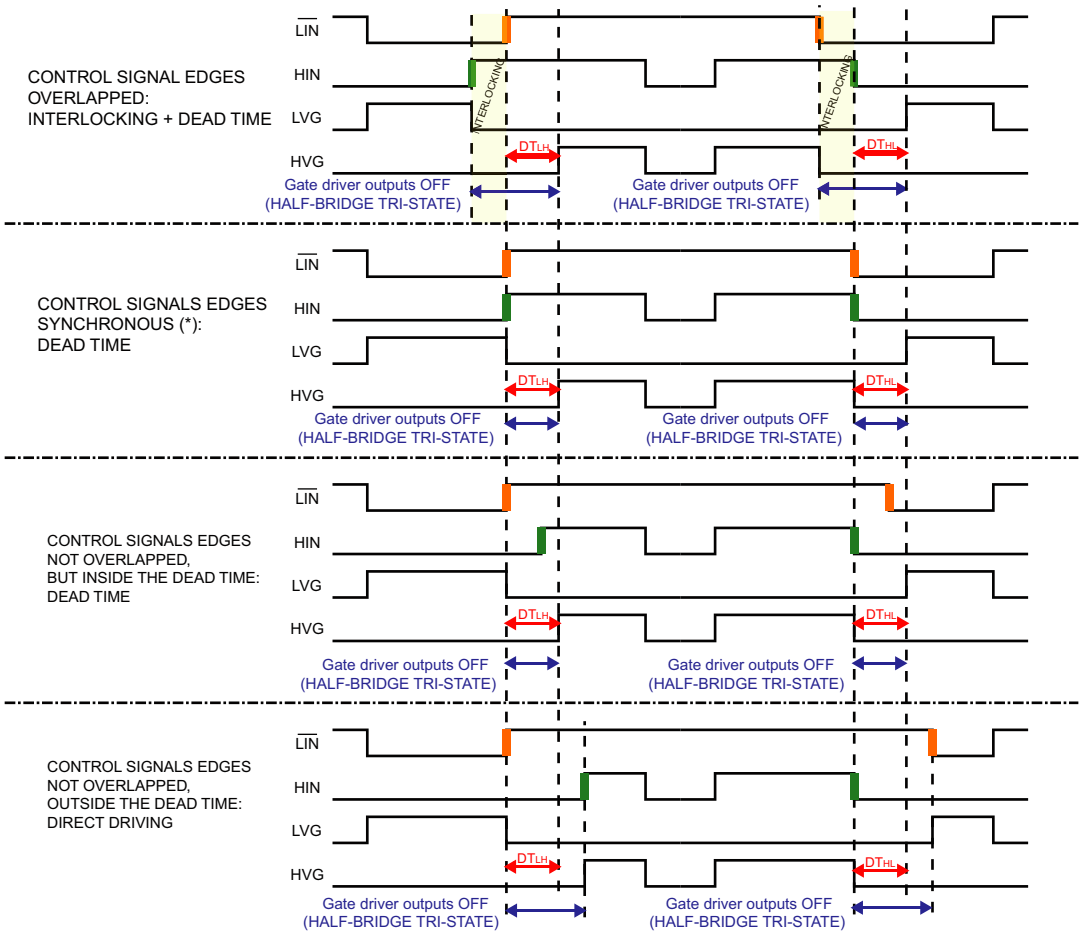


Figure 6. Deadtime and interlocking waveforms definition



(*) HIN and $\overline{\text{LIN}}$ can be connected togheter and driven by just one control signal.

AM040090

6 Input logic

Input logic is provided with an interlocking circuitry which avoids cross-conduction in case of wrong signals on LIN and HIN tries to turn-on both LVG and HVG outputs at the same times. In addition, to prevent cross conduction of the external MOSFETs, after each output is turned off, the other output cannot be turned on before a certain amount of time (DT) (see *Figure 5: Dead time and interlocking timing definitions*).

Table 9. Truth table

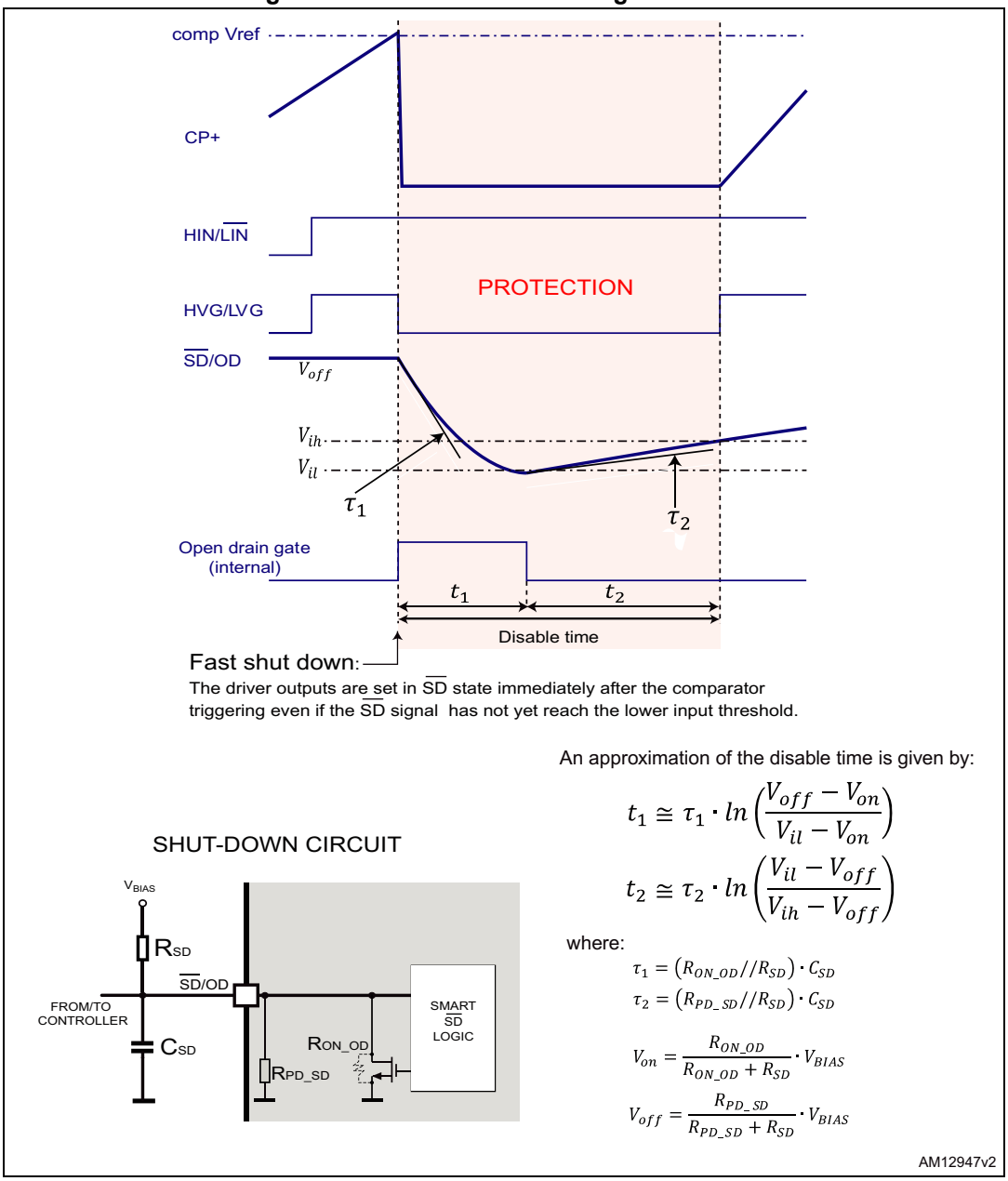
Input			Output	
$\overline{SD}$	$\overline{LIN}$	HIN	LVG	HVG
L	X(1)	X(1)	L	L
H	H	L	L	L
H	L	H	L	L
H	L	L	H	L
H	H	H	L	H

1. X: don't care.

7 Smart shutdown function

The L6390 device integrates a comparator committed to the fault sensing function. The comparator has an internal voltage reference V_{ref} connected to the inverting input, while the non-inverting input is available on the pin 10. The comparator input can be connected to an external shunt resistor in order to implement a simple overcurrent detection function. The output signal of the comparator is fed to an integrated MOSFET with the open drain output available on the pin 2, shared with the $\overline{SD}$ input. When the comparator triggers, the device is set in shutdown state and both its outputs are set to low level leaving the half-bridge in tristate.

Figure 7. Smart shutdown timing waveforms

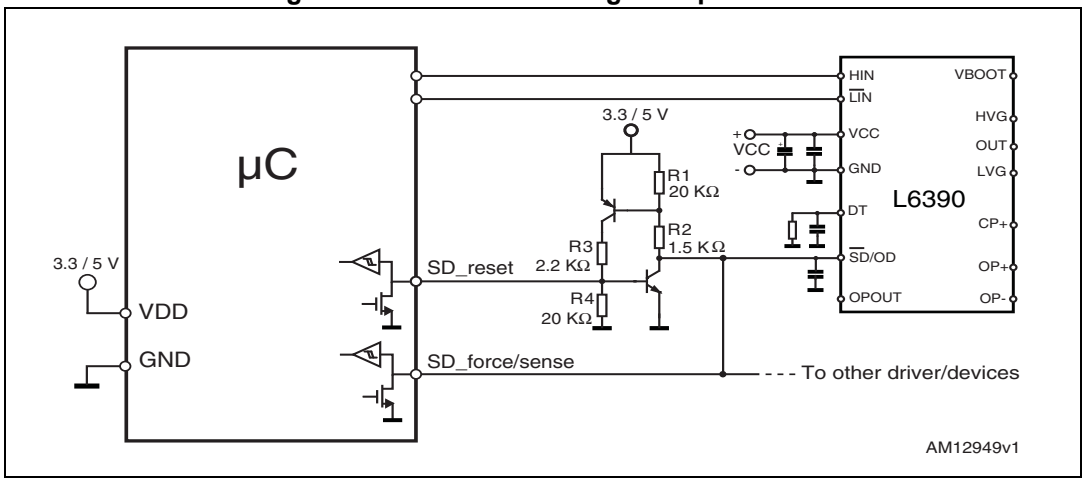


In common overcurrent protection architectures the comparator output is usually connected to the $\overline{SD}$ input and an RC network is connected to this $\overline{SD}$/OD line in order to provide a monostable circuit, which implements a protection time that follows the fault condition. Differently from the common fault detection systems, the L6390 smart shutdown architecture allows immediate turn-off of the outputs of the gate driver in the case of fault, by minimizing the propagation delay between the fault detection event and the actual output switch-off. In fact, the time delay between the fault detection and the output turn-off is no longer dependent on the value of the external RC network connected to the $\overline{SD}$/OD pin. In the smart shutdown circuitry the fault signal has a preferential path which directly switches off the outputs after the comparator triggering. At the same time the internal logic turns on the open drain output and holds it on until the $\overline{SD}$ voltage goes below the $\overline{SD}$ logic input lower threshold. When such threshold is reached, the open drain output is turned off, allowing the external pull-up to recharge the capacitor. The driver outputs restart following the input pins as soon as the voltage at the $\overline{SD}$/OD pin reaches the higher threshold of the $\overline{SD}$ logic input. The smart shutdown system provides the possibility to increase the time constant of the external RC network (that determines the disable time after the fault event) up to very large values without increasing the delay time of the protection.

Any external signal provided to the $\overline{SD}$ pin is not latched and can be used as control signal in order to perform, for instance, PWM chopping through this pin. In fact when a PWM signal is applied to the $\overline{SD}$ input and the logic inputs of the gate driver are stable, the outputs switch from the low level to the state defined by the logic inputs and vice versa.

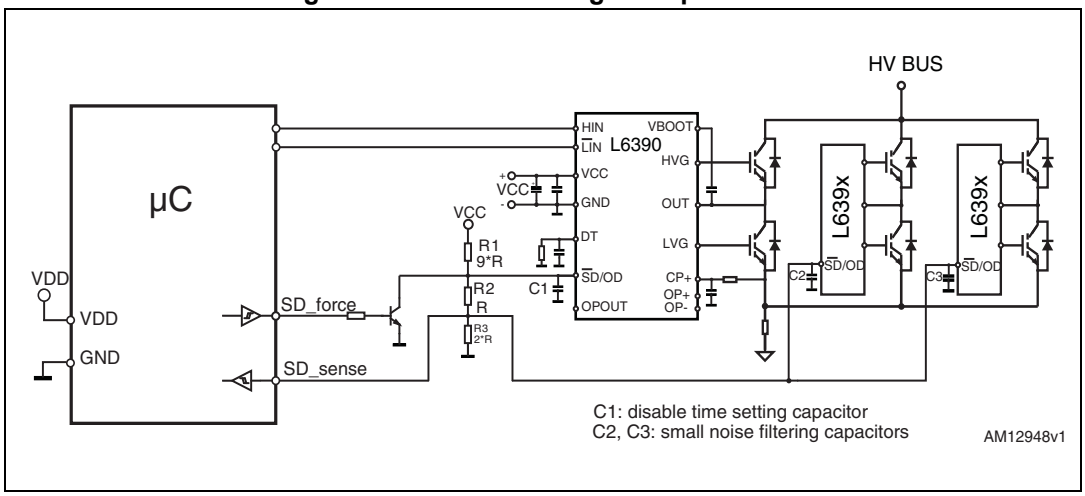
In some applications it may be useful to latch the driver in the shutdown condition for an arbitrary time, until the controller decides to reset it to normal operation. This may, for example, be achieved with a circuit similar to the one shown in *Figure 8*. When the open drain starts pulling down the $\overline{SD}$/OD pin, the external latch turns on and keeps the pin to GND, preventing it from being pulled up again once the $\overline{SD}$ logic input lower threshold is reached and the internal open drain turns off. One pin of the controller is used to release the external latch, and one to externally force a shutdown condition and also to read the status of the $\overline{SD}$/OD pin.

Figure 8. Protection latching example circuit



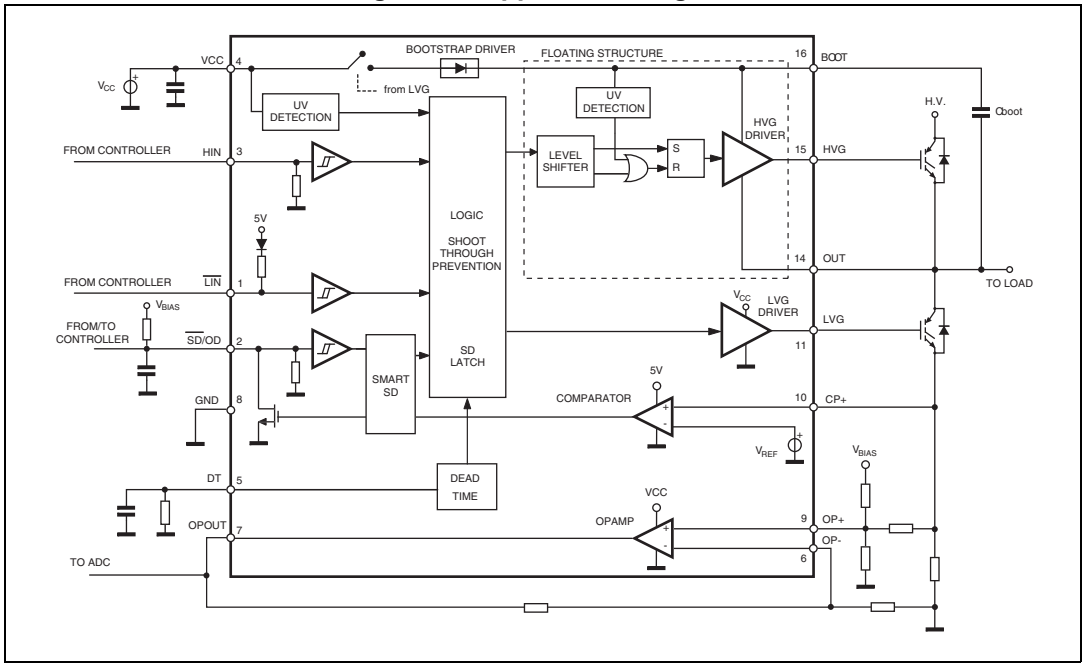
In applications using only one L6390 for the protection of several different legs (such as a single-shunt inverter, for example) it may be useful to implement the resistor divider shown in *Figure 9*. This simple network allows the pushing of the $\overline{SD}$ pins of the other devices to a voltage lower than L6390 V_{il}, so that each device can reach its low logic level regardless of part-to-part variations of the thresholds.

Figure 9. $\overline{SD}$ level shifting example circuit



8 Typical application diagram

Figure 10. Application diagram



9 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (*Figure 11*.a). In the L6390 device a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low-side driver (LVG), with a diode in series, as shown in *Figure 11*.b. An internal charge pump (*Figure 11*.b) provides the DMOS driving voltage.

C_{BOOT} selection and charging

To choose the proper C_{BOOT} value the external MOS can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOS total gate charge:

Equation 1

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss. It must be:

Equation 2

$$C_{BOOT} >>> C_{EXT}$$

E.g.: if Q_{gate} is 30 nC and V_{gate} is 10 V, C_{EXT} is 3 nF. With C_{BOOT} = 100 nF the drop would be 300 mV.

If HVG must be supplied for a long time, the C_{BOOT} selection must also take the leakage and quiescent losses into account.

E.g.: HVG steady-state consumption is lower than 240 µA, so if HVG T_{ON} is 5 ms, C_{BOOT} must supply 1.2 µC to C_{EXT}. This charge on a 1 µF capacitor means a voltage drop of 1.2 V.

The internal bootstrap driver offers important advantages: the external fast recovery diode can be avoided (it usually has a high leakage current).

This structure can work only if V_{OUT} is close to GND (or lower) and, at the same time, the LVG is on. The charging time (T_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it must be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS R_{DSon} (typical value: 120 Ω). This drop can be neglected at low switching frequency, but it should be taken into account when operating at high switching frequency.

The following equation is useful to compute the drop on the bootstrap DMOS:

Equation 3

$$V_{drop} = I_{charge}R_{dson} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}}R_{dson}$$

where Q_{gate} is the gate charge of the external power MOSFET, R_{dson} is the on-resistance of the bootstrap DMOS and T_{charge} is the charging time of the bootstrap capacitor.

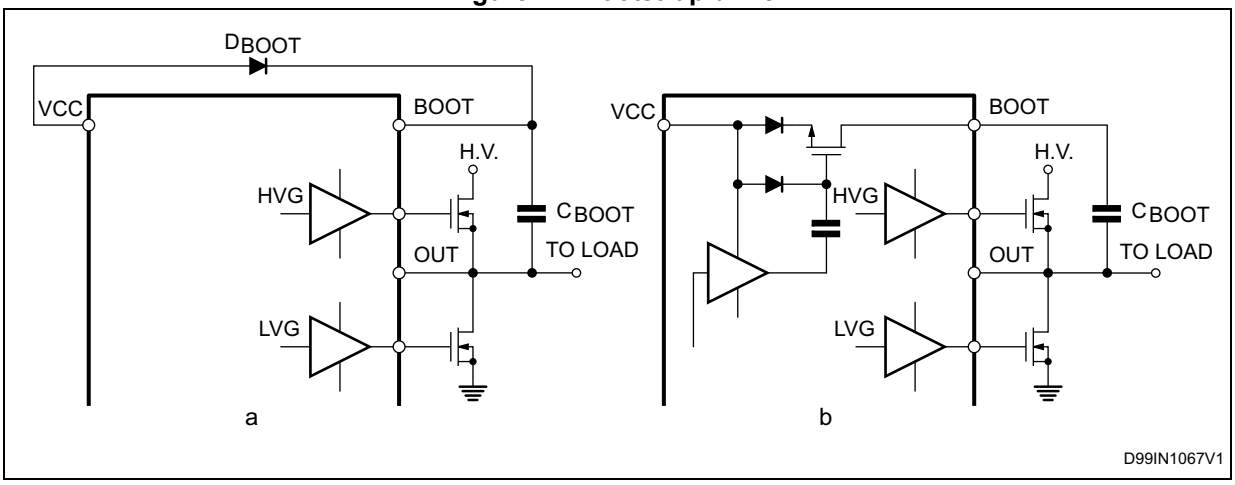
For example: using a power MOSFET with a total gate charge of 30 nC, the drop on the bootstrap DMOS is about 1 V, if the T_{charge} is 5 µs. In fact:

Equation 4

$$V_{drop} = \frac{30nC}{5\mu s} \cdot 120\Omega \sim 0.7V$$

V_{drop} should be taken into account when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

Figure 11. Bootstrap driver



10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 SO-16 package information

Figure 12. SO-16 narrow package outline

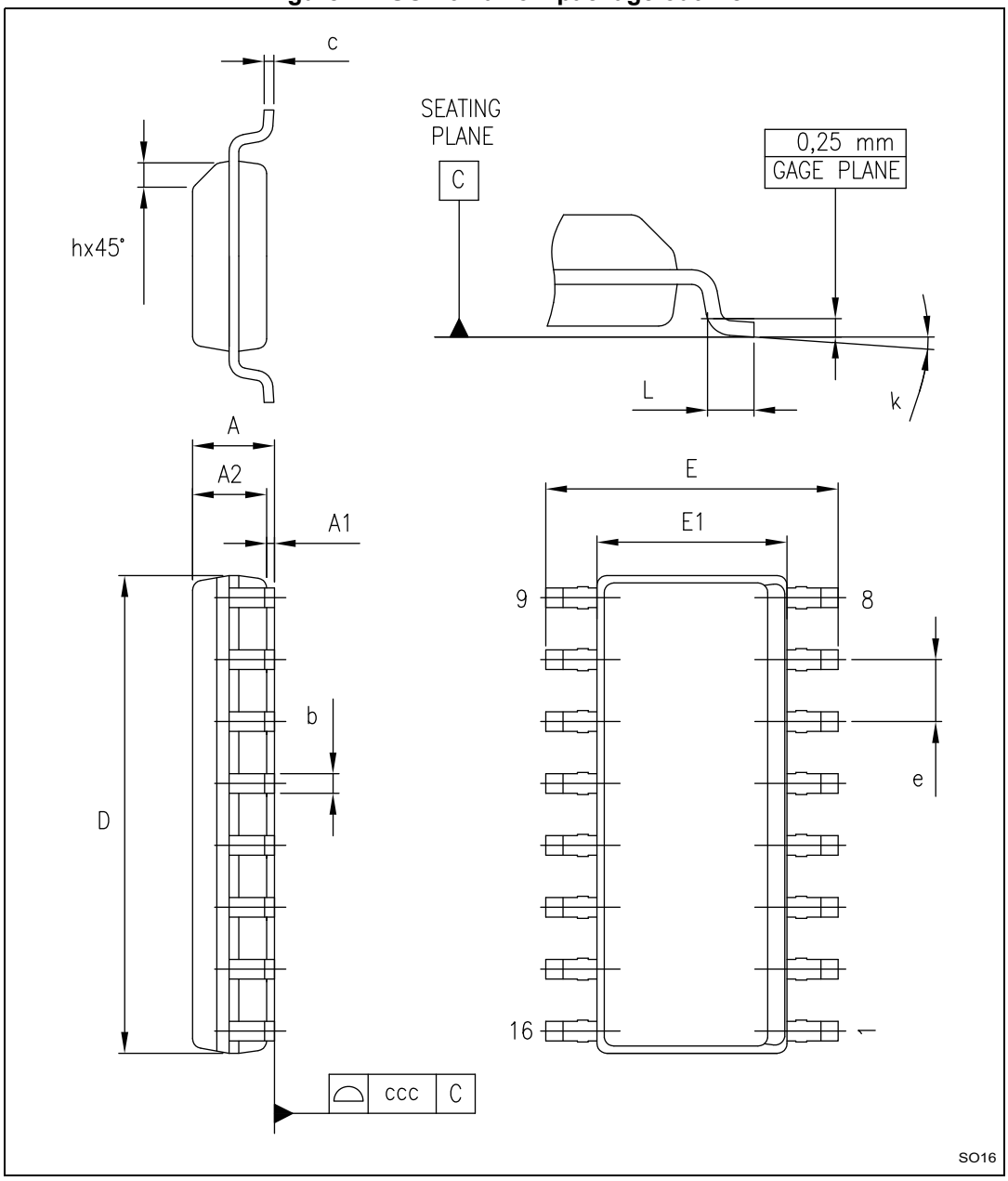
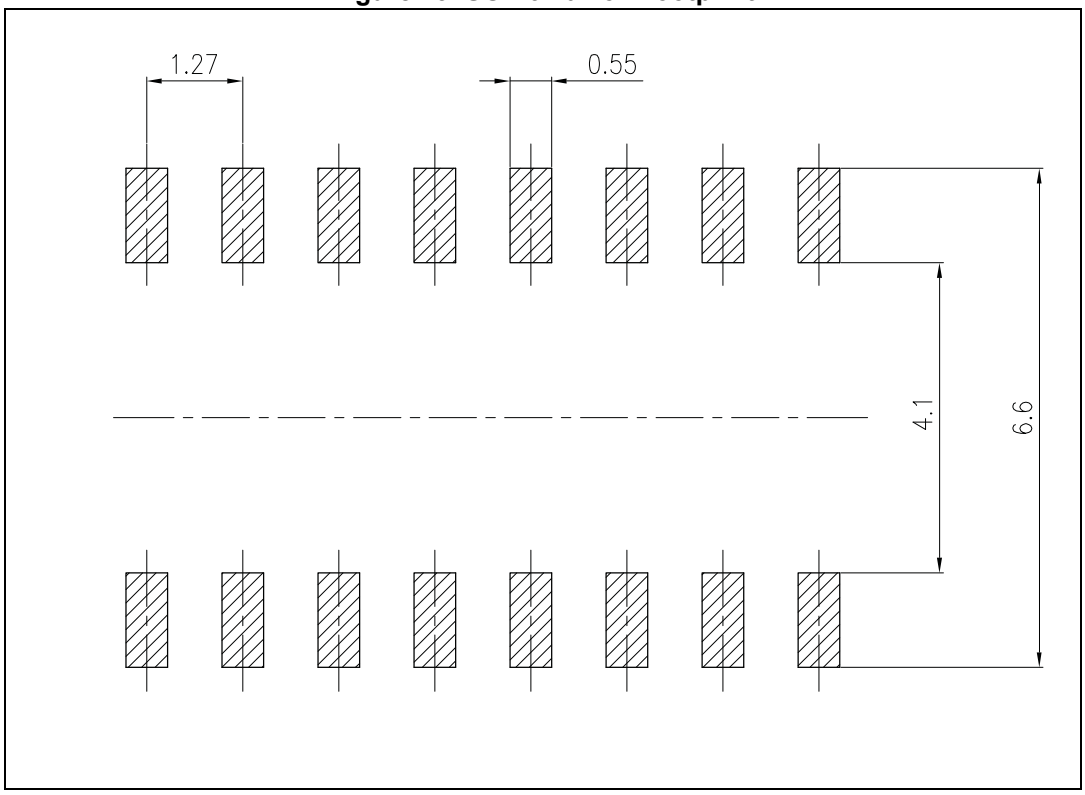


Table 10. SO-16 narrow package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	-	-	1.75
A1	0.10	-	0.25
A2	1.25	-	-
b	0.31	-	0.51
c	0.17	-	0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	-	1.27	-
h	0.25	-	0.50
L	0.40	-	1.27
k	0	-	8°
ccc	-	-	0.10

Figure 13. SO-16 narrow footprint



11 Order codes

Table 11. Order codes

Order code	Package	Packaging
L6390D	SO-16	Tube
L6390DTR	SO-16	Tape and reel

12 Revision history

Table 12. Document revision history

Date	Revision	Changes
11-Sep-2015	9	Removed DIP-16 package from the whole document. Updated *Table 3 on page 6* (added ESD parameter and value). Updated *Table 4 on page 6* (updated $R_{th(JA)}$ value). Updated note *1.*and *2.* below *Table 7 on page 10* (minor modifications, replaced V_{CBOOTx} by V_{BOOTx}). Minor modifications throughout document.
07-Apr-2017	10	Updated *Table 5 on page 7* (updated cross reference to *Figure 4 on page 12* instead of removed *Figure 3. Timing*). Updated *Table 6 on page 9* (added R_{PD_SD}) and *Table 8 on page 11* (added R_{ON_OD}). Updated *Section 5 on page 12* (updated title, added *Figure 4* and *Figure 5*). Added *Section 6 on page 14* (and moved *Table 9: Truth table* to this section). Updated *Figure 11 on page 20* and *Figure 12 on page 21* (replaced by new figure). Minor modifications throughout document.
21-Mar-2018	11	Updated Figure of SO-16 package on page 1 and *Figure 2: Pin connection (top view) on page 4*. Updated *Table 5 on page 7* (updated DT and MDT test conditions). Updated note *2.* below *Table 7 on page 11*. Updated *Section 6 on page 14*. Minor modifications throughout document.