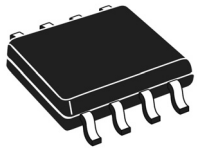
L6726A

Single phase PWM controller

Feature

- Flexible power supply from 5V to 12V
- Power conversion input as low as 1.5V
- 1% output voltage accuracy
- High-current integrated drivers
- Adjustable output voltage
- 0.8V internal reference
- Sensorless and programmable OCP across Low-side R_{dsON}
- Oscillator internally fixed at 270kHz
- Programmable soft-start
- LS-LESS start up
- Disable function
- FB disconnection protection
- SO-8 package



SO-8

Description

L6726A is a single-phase step-down controller with integrated high-current drivers that provides complete control logic, protections and reference voltage to realize in an easy and simple way general DC-DC converters by using a compact SO-8 package.

Device flexibility allows managing conversions with power input V_{IN} as low as 1.5V and device supply voltage ranging from 5V to 12V.

L6726A provides simple control loop with trans-conductance error amplifier. The integrated 0.8V reference allows regulating output voltage with ±1% accuracy over line and temperature variations. Oscillator is internally fixed to 270kHz.

L6726A provides programmable over current protection. Current information is monitored across the Low-Side mosfet R_{dsON} saving the use of expensive and space-consuming sense resistors.

FB disconnection protection prevents excessive and dangerous output voltages in case of floating FB pin.

Applications

- Subsystem power supply (MCH, IOCH, PCI...)
- Memory and termination Supply
- CPU & DSP power supply
- Distributed power supply
- General DC / DC converters

Order codes

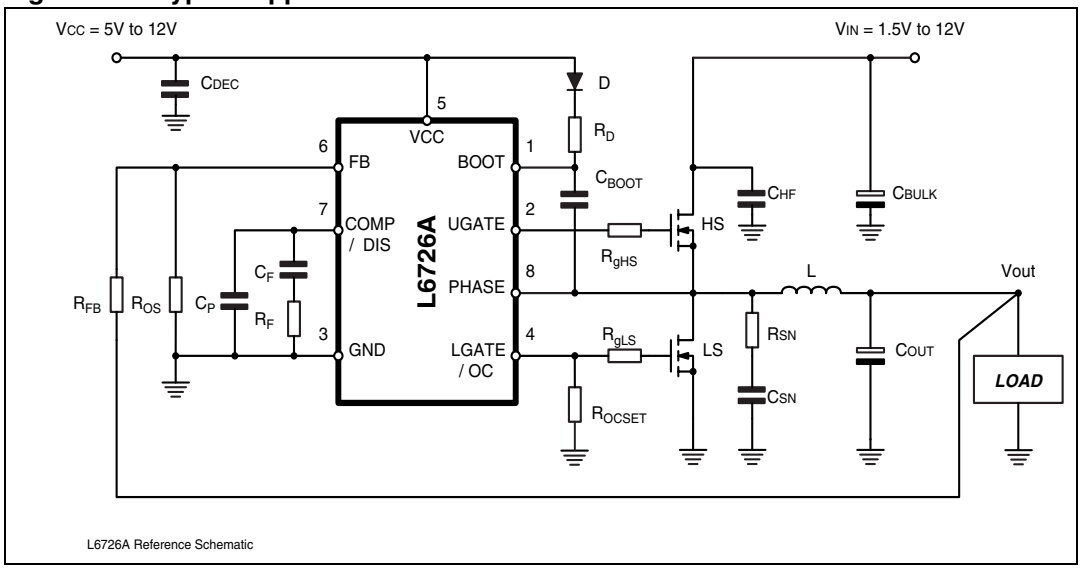
Part Number	Package	Packing
L6726A	SO-8	Tube
L6726ATR	SO-8	Tape & Reel

Contents

1 Typical application circuit and block diagram

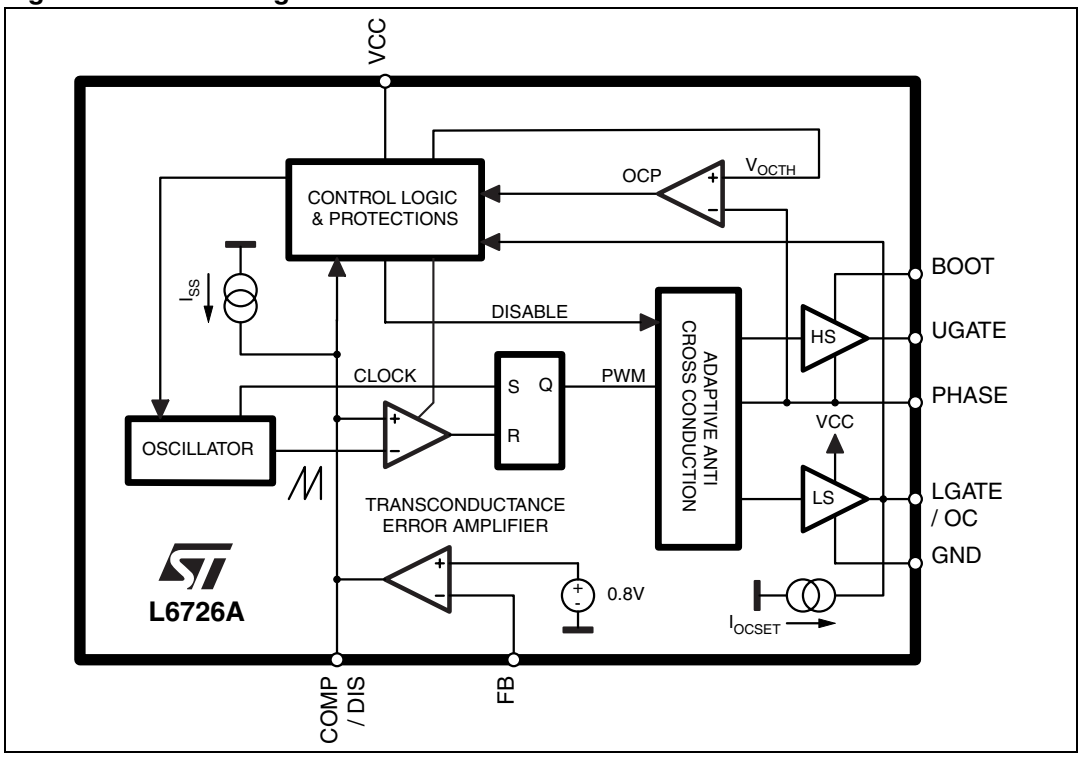
1.1 Application circuit

Figure 1. Typical application circuit



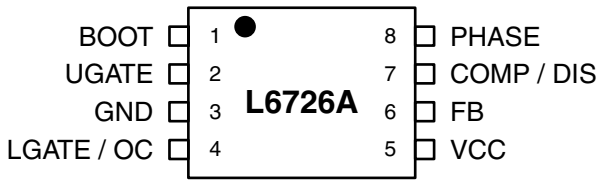
1.2 Block diagram

Figure 2. Block diagram



2 Pins description and connection diagrams

Figure 3. Pins connection (Top View)



2.1 Pin descriptions

Table 1. Pins descriptions

Pin #	Name	Function
1	BOOT	HS Driver Supply. Connect through a capacitor (100nF) to the floating node (LS-Drain) pin and provide necessary bootstrap diode from VCC.
2	UGATE	HS Driver Output. Connect to HS mosfet gate.
3	GND	All internal references, logic and drivers are connected to this pin. Connect to the PCB ground plane.
4	LGATE / OC	*LGATE*. LS Driver Output. Connect to LS mosfet gate. *OC*. Over Current threshold set. During a short period of time following VCC rising over UVLO threshold, a 10µA current is sourced from this pin. Connect to GND with an R_{OCSET} resistor greater than 5kΩ to program OC Threshold. The resulting voltage at this pin is sampled and held internally as the OC set point. Maximum programmable OC threshold is 0.55V. A voltage greater than 0.75V (max) activates an internal clamp and causes OC threshold to be set at 375mV. R_{OCSET} not connected sets the 375mV default threshold.
5	VCC	Device and LS Driver power supply. Operative range from 4.1V to 13.2V. Filter with at least 1µF MLCC to GND.
6	FB	Error Amplifier Inverting Input. Connect with a resistor R_{FB} to the output regulated voltage. Additional resistor R_{OS} to GND may be used to regulate voltages higher than the reference.
7	COMP / DIS	*COMP*. Error Amplifier Output. Connect with an R_F - C_F // C_P to GND to compensate the device control loop in conjunction to the FB pin. During the Soft-Start phase, a 10µA current is sourced from this pin so the compensation capacitors also act to program the SS time. *DIS.* The device can be disabled by pulling this pin lower than 0.4V (min). Setting free the pin, the device enables again.
8	PHASE	HS Driver return path, current-reading and adaptive-dead-time monitor. Connect to the LS drain to sense R_{dsON} drop to measure the output current. This pin is also used by the adaptive-dead-time control circuitry to monitor when HS mosfet is OFF.

2.2 Thermal data

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient(1)	65	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction temperature range	0 to 125	°C

1. Measured with the component mounted on a 2S2P board in free air (6.7mm x 6.7mm, 35µm (P) and 17.5µm (S) copper thickness).

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	to GND	-0.3 to 15	V
V_{BOOT}	to PHASE to GND	15 45	V
V_{UGATE}	to PHASE to PHASE; t < 50ns to GND	-0.3 to (V_{BOOT} - V_{PHASE}) + 0.3 -1 V_{BOOT} + 0.3	V
V_{PHASE}	to GND	-8 to 30	V
V_{LGATE}	to GND to GND; t < 50ns	-0.3 to V_{CC} + 0.3 -1	V
	FB, COMP to GND	-0.3 to 3.6	V
FB pin	Maximum Withstanding Voltage Range Test Condition: CDF-AEC-Q100-002 "HBM" Acceptance Criteria: "Normal Performance"	±1	kV
Other pins		±2	kV

3.2 Electrical characteristics

Table 4. Electrical characteristics

(V_{CC} = 12V; T_A = 25° C unless otherwise specified).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Recommended operating conditions						
V_{CC}	Device supply voltage	See *Figure 1*	4.1		13.2	V
V_{IN}	Conversion input voltage				13.2	V
Supply current and power-ON						
I_{CC}	VCC supply current	UGATE and LGATE = OPEN		6		mA
I_{BOOT}	BOOT supply current	UGATE = OPEN; PHASE to GND		0.5		mA
UVLO	VCC Turn-ON	VCC Rising			4.1	V
	Hysteresis			0.2		V
Oscillator						
F_{SW}	Main oscillator accuracy		243	270	297	kHz
ΔV_{OSC}	PWM ramp amplitude			1.1		V
d_{MAX}	Maximum duty cycle		80			%

Table 4. Electrical characteristics (continued)
(V_{CC} = 12V; T_A = 25° C unless otherwise specified).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Reference						
	Output voltage accuracy	V_{OUT} = 0.8V	-1	-	1	%
Transconductance error amplifier						
gm	Transconductance(1)				5	mS
I_{FB}	Input bias current	Sourced from FB		100		nA
A_0	Open loop gain(1)			70		dB
F_0	Unity gain(1)			4		MHz
I_{COMP}	Current capability	Source current		360		µA
		Sink current		-360		µA
Soft-Start and disable						
I_{SS}	Soft-start current	From COMP pin		10		µA
DIS	Disable threshold	COMP Falling	0.4	0.5		V
Gate drivers						
I_{UGATE}	HS source current	BOOT - PHASE = 5V to 12V		1.5		A
R_{UGATE}	HS sink resistance	BOOT - PHASE = 5V to 12V		1.1		Ω
I_{LGATE}	LS source current	VCC = 5V to 12V		1.5		A
R_{LGATE}	LS sink resistance	VCC = 5V to 12V		0.65		Ω
OVER-CURRENT PROTECTION						
I_{OCSET}	OCSET current source	Sourced from LGATE pin. See *Section 7.1.1*		10		µA
V_{OC_SW}	OC switch-over threshold	$V_{LGATE/OC}$ rising			750	mV
V_{OCTH_FIXED}	Fixed OC threshold	V_{PHASE} to GND		-375		mV

1. Guaranteed by design, not subject to test.

4 Device description

L6726A is a single-phase PWM controller with embedded high-current drivers that provides complete control logic and protections to realize in an easy and simple way a general DC-DC step-down converter. Designed to drive N-channel MOSFETs in a synchronous buck topology, with its high level of integration this 8-pin device allows reducing cost and size of the power supply solution.

L6726A is designed to operate from a 5V or 12V supply bus. Thanks to the high precision 0.8V internal reference, the output voltage can be precisely regulated to as low as 0.8V with ±1% accuracy over line and temperature variations. The switching frequency is internally set to 270kHz.

This device provides a simple control loop with externally compensated transconductance error-amplifier and programmable soft start. Low-Side-Less feature allows the device to perform soft-start over pre-charged output avoiding negative spikes at the load side.

In order to avoid load damages, L6726A provides programmable threshold over current protection. Output current is monitored across Low-Side MOSFET R_{dsON}, saving the use of expensive and space-consuming sense resistor. L6726A also features FB disconnection protection, preventing dangerous uncontrolled output voltages in case of floating FB pin.

5 Driver section

The integrated high-current drivers allow using different types of power MOSFET (also multiple MOSFETs to reduce the equivalent R_{dsON}), maintaining fast switching transition.

The driver for high-side MOSFET uses BOOT pin for supply and PHASE pin for return. The driver for low-side MOSFET uses the VCC pin for supply and GND pin for return.

The controller embodies an anti-shoot-through and adaptive dead-time control to minimize low side body diode conduction time, maintaining good efficiency while saving the use of Schottky diode:

- to check for high-side MOSFET turn off, PHASE pin is sensed. When the voltage at PHASE pin drops down, the low-side MOSFET gate drive is suddenly applied;
- to check for low-side MOSFET turn off, LGATE pin is sensed. When the voltage at LGATE has fallen, the high-side MOSFET gate drive is suddenly applied.

If the current flowing in the inductor is negative, voltage on PHASE pin will never drop. To allow the low-side MOSFET to turn-on even in this case, a watchdog controller is enabled: if the source of the high-side MOSFET doesn't drop, the low side MOSFET is switched on so allowing the negative current of the inductor to recirculate. This mechanism allows the system to regulate even if the current is negative.

Power conversion input is flexible: 5V, 12V bus or any bus that allows the conversion (See maximum duty cycle limitation and recommended operating conditions) can be chosen freely.

5.1 Power dissipation

L6726A embeds high current MOSFET drivers for both high side and low side MOSFETs: it is then important to consider the power that the device is going to dissipate in driving them in order to avoid overcoming the maximum junction operative temperature.

Two main terms contribute in the device power dissipation: bias power and drivers power.

- Device Bias Power (P_{DC}) depends on the static consumption of the device through the supply pins and it is simply quantifiable as follow (assuming to supply HS and LS drivers with the same VCC of the device):

$$P_{DC} = V_{CC} \cdot (I_{CC} + I_{BOOT})$$

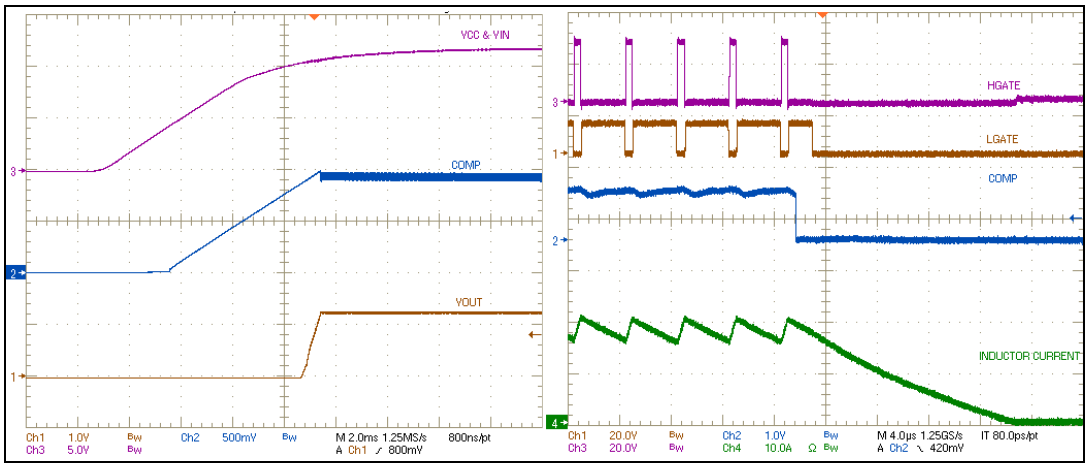
- Drivers power is the power needed by the driver to continuously switch on and off the external MOSFETs; it is a function of the switching frequency, the voltage supply of the driver and total gate charge of the selected MOSFETs. It can be quantified considering that the total power P_{SW} dissipated to switch the MOSFETs (easy calculable) is dissipated by three main factors: external gate resistance (when present), intrinsic MOSFET resistance and intrinsic driver resistance. This last term is the important one to be determined to calculate the device power dissipation. The total power dissipated to switch the MOSFETs results:

$$P_{SW} = F_{SW} \cdot [Q_{gHS} \cdot (V_{BOOT} - V_{PHASE}) + Q_{gLS} \cdot V_{CC}]$$

where V_{BOOT} - V_{PHASE} is the voltage across the bootstrap capacitor.

External gate resistors helps the device to dissipate the switching power since the same power P_{SW} will be shared between the internal driver impedance and the external resistor resulting in a general cooling of the device.

Figure 4. Soft start (left) and Disable (right)



6 Soft start and disable

L6726A implements a soft start to smoothly charge the output filter avoiding high in-rush currents to be required from the input power supply. The device sources a 10µA soft start current from COMP, linearly charging the compensation network capacitors. The ramping COMP voltage is compared to the oscillator triangular waveform generating PWM pulses of increasing width that charge the output capacitors.

When the FB voltage crosses 800 mV, the output voltage is in regulation: soft start phase will end and the transconductance error amplifier output will be enabled closing the control loop.

In the event of an over current during soft start, the over current logic will override the soft start sequence and will shut down the PWM logic and both the high side and low side gates. This condition is latched, cycle VCC to recover.

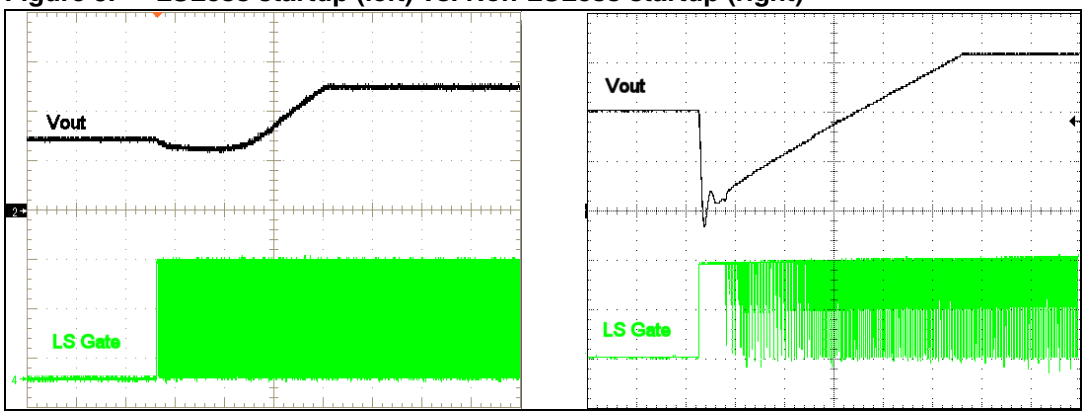
The device sources soft start current only when VCC power supply is above UVLO threshold and over current threshold setting phase has been completed.

6.1 Low-Side-Less start up (LSLess)

L6726A performs a special sequence in enabling LS driver to switch: during the soft-start phase, the LS driver results disabled (LS = OFF) until the HS starts to switch. This avoids the dangerous negative spike on the output voltage that can happen if starting over a pre-charged output and limits the output discharge (amount of output discharge depends on programmed SS time length: the shorter the programmed SS, the more limited the output discharge).

If the output voltage is pre-charged to a voltage higher than the final one, the HS would never start to switch. In this case, LS is enabled and discharges the output to the final regulation value.

Figure 5. LSLess startup (left) vs. Non-LSLess startup (right)



6.2 Enable / Disable

The device can be disabled by pushing COMP / DIS pin under 0.4V (min). In this condition HS and LS MOSFETs are turned off, and the 10µA SS current is sourced from COMP / DIS pin. Setting free the pin, the device enables again performing a new SS.

7 Protections

7.1 Over current protection

The over current feature protects the converter from a shorted output or overload, by sensing the output current information across the Low Side MOSFET drain-source on-resistance, R_{dsON}. This method reduces cost and enhances converter efficiency by avoiding the use of expensive and space-consuming sense resistors.

The low side R_{dsON} current sense is implemented by comparing the voltage at the PHASE node when LS MOSFET is turned on with the programmed OCP threshold voltage, internally held. If the monitored voltage drop (GND to PHASE) exceeds this threshold, an Over Current Event is detected. If two Over Current Events are detected in two consecutive switching cycles, the protection will be triggered and the device will turn off both LS and HS MOSFETs in a latched condition.

To recover from Over Current Protection triggered, VCC power supply must be cycled.

7.1.1 Over current threshold setting

L6726A allows to easily program an Over Current Threshold ranging from 50mV to 550mV, simply by adding a resistor (R_{OCSET}) between LGATE and GND.

During a short period of time (5.5ms - 6.5ms) following VCC rising over UVLO threshold, an internal 10µA current (I_{OCSET}) is sourced from LGATE pin, determining a voltage drop across R_{OCSET}. This voltage drop will be sampled and internally held by the device as Over Current Threshold. The OC setting procedure overall time length ranges from 5.5ms to 6.5ms, proportionally to the threshold being set.

Connecting a R_{OCSET} resistor between LGATE and GND, the programmed threshold will be:

$$I_{OCth} = \frac{I_{OCSET} \cdot R_{OCSET}}{R_{dsON}}$$

R_{OCSET} values range from 5kΩ to 55kΩ

If the voltage drop across R_{OCSET} is too low, the system will be very sensitive to start-up inrush current and noise. This can result in undesired OCP triggering. In this case, consider increasing R_{OCSET} value.

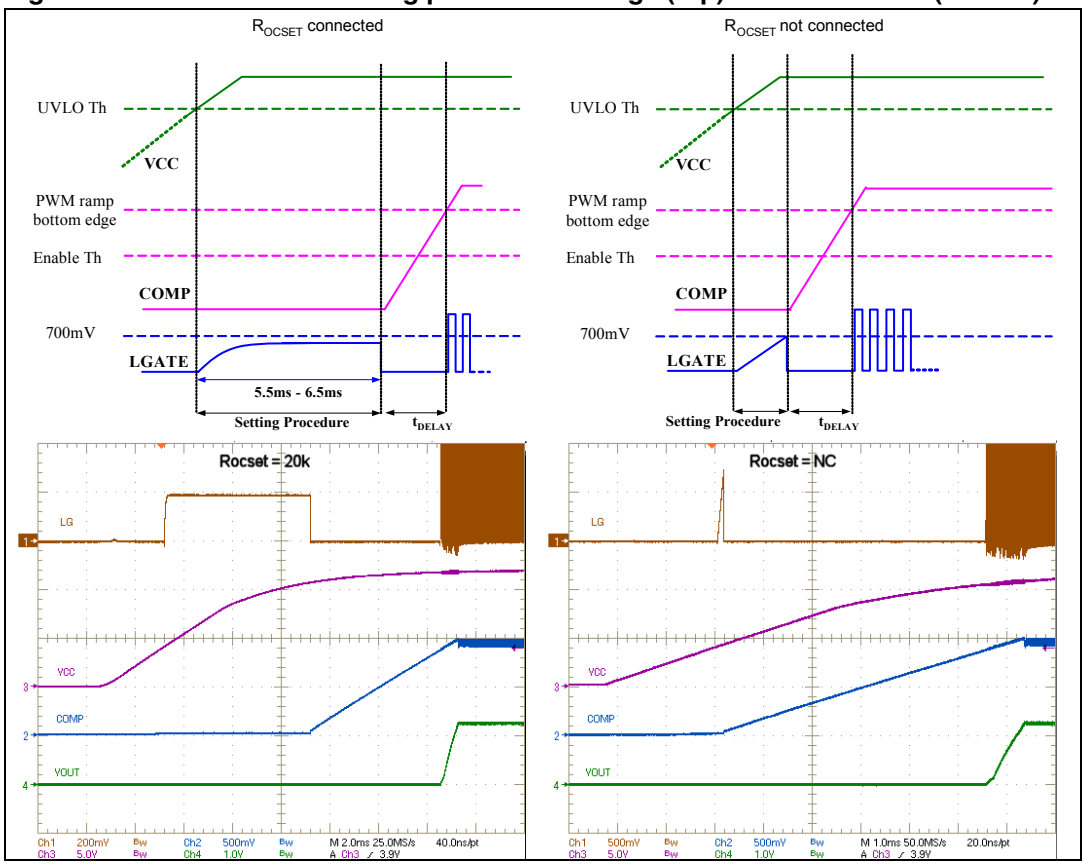
In case R_{OCSET} is not connected, the device switches the OCP threshold to a 375mV default value: an internal safety clamp on LGATE is triggered as soon as LGATE voltage reaches 700mV (typ), enabling the 375mV default threshold and suddenly ending OC setting phase.

See *Figure 6* for OC threshold setting procedure timings picture and oscilloscope sample waveforms.

7.2 Feedback disconnection protection

In order to provide load protection even if FB pin is not connected, a 100nA bias current is always sourced from this pin. If FB pin is not connected, bias current will permanently pull up FB: this forces COMP pin low, avoiding output voltage rising to dangerous levels.

Figure 6. OC threshold setting procedure timings (top) and waveforms (bottom)

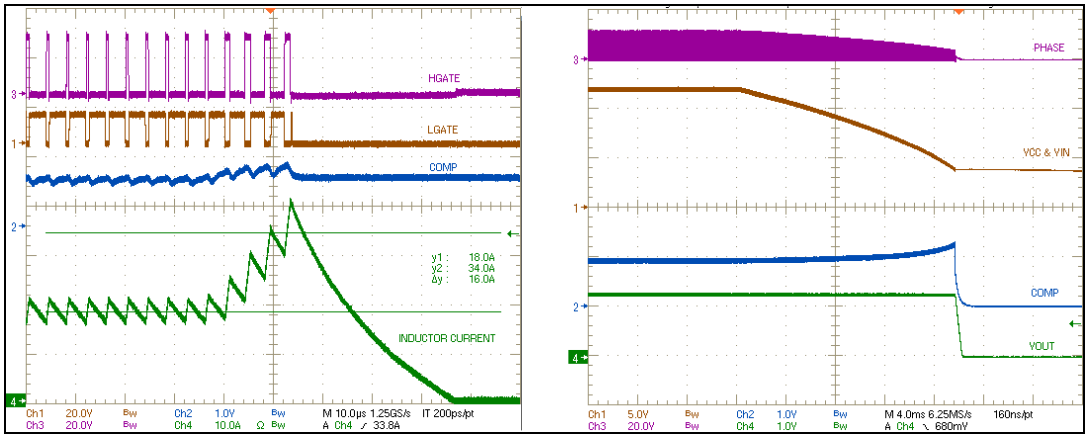


7.3 Under Voltage Lock Out

In order to avoid anomalous behaviors of the device when the supply voltage is too low to support its internal rails, UVLO is provided: the device will start up when VCC reaches UVLO upper threshold and will shutdown when VCC drops below UVLO lower threshold.

The 4.1V maximum UVLO upper threshold allows L6726A to be supplied from 5V and 12V busses in or-ing diode configuration.

Figure 7. OCP trip, default threshold, LS: STD38NH02L (left). UVLO turn off (right)



8 Application details

8.1 Output voltage selection

L6726A is capable to precisely regulate an output voltage as low as 0.8V. In fact, the device comes with a fixed 0.8V internal reference that guarantees the output regulated voltage to be within ±1% tolerance over line and temperature variations (excluding output resistor divider tolerance, when present).

Output voltage higher than 0.8V can be achieved by adding a resistor R_{OS} between FB pin and ground. Referring to *Figure 1*, the steady state DC output voltage will be:

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R_{FB}}{R_{OS}}\right)$$

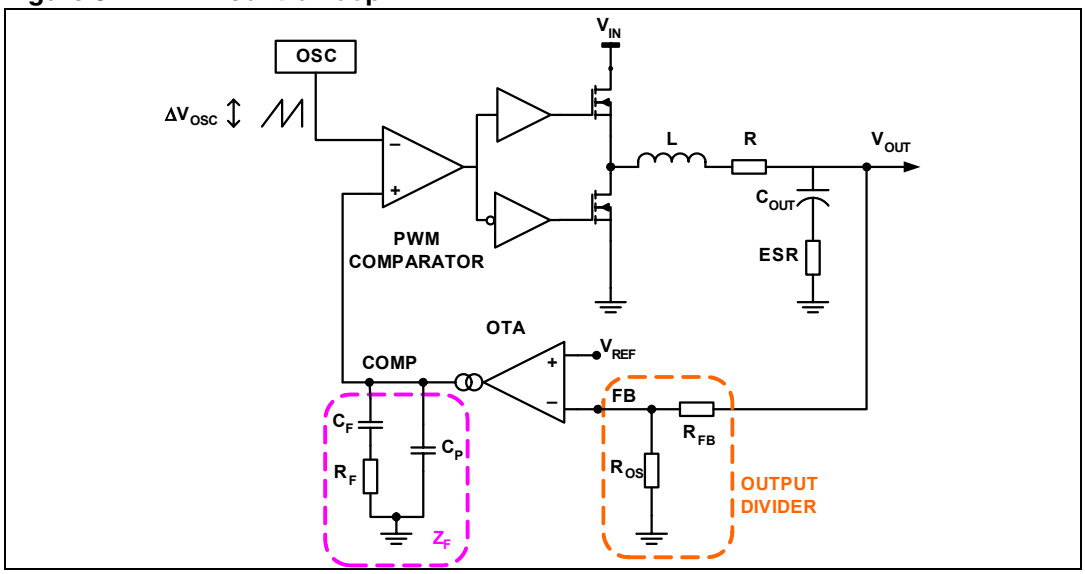
where V_{REF} is 0.8V.

8.2 Compensation network

The control loop shown in *Figure 8* is a voltage mode control loop. The error amplifier is a transconductance type with fixed gain (3.3mS typ.). The FB voltage is regulated to the internal reference, thus the output voltage is fixed accordingly to the output resistor divider (when present).

Transconductance error amplifier output current generates a voltage across Z_F, which is compared to oscillator saw-tooth waveform to provide PWM signal to the driver section. PWM signal is then transferred to the switching node with V_{IN} amplitude. This waveform is filtered by the output filter.

Figure 8. PWM control loop



The converter transfer function is the small signal transfer function between the voltage at the output node of the EA (COMP) and V_{OUT}. This function has a double pole (complex conjugate) at frequency F_{LC} depending on the L-C_{OUT} resonance and a zero at F_{ESR}

depending on the output capacitor ESR. The DC Gain of the modulator is simply the input voltage V_{IN} divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

V_{OUT} is scaled and transferred to FB node by the output resistor divider.

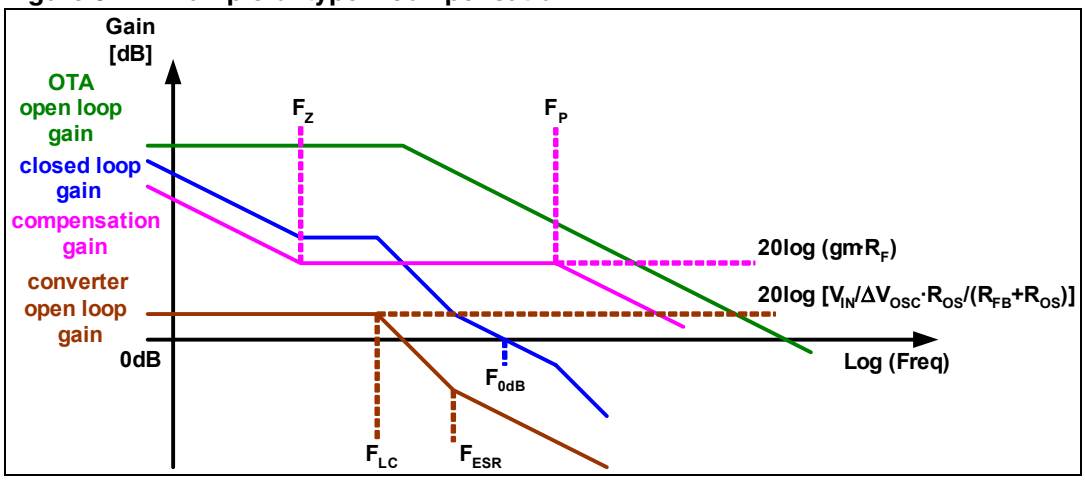
The compensation network closes the loop joining FB and COMP node with transfer function ideally equal to $-gm \cdot Z_F$.

Compensation goal is to close the control loop assuring high DC regulation accuracy, good dynamic performances and stability. To achieve this, the overall loop needs high DC gain, high bandwidth and good phase margin.

High DC gain is achieved giving an integrator shape to compensation network transfer function. Loop bandwidth (F_{0dB}) can be fixed choosing the right R_F; however, for stability, it should not exceed $F_{SW}/2\pi$. To achieve a good phase margin, the control loop gain has to cross 0dB axis with -20dB/decade slope.

As an example, *Figure 9* shows an asymptotic bode plot of a type II compensation.

Figure 9. Example of type II compensation.



- Open loop converter singularities:

  a) $$F_{LC} = \frac{1}{2\pi\sqrt{L \cdot C_{OUT}}}$$

  b) $$F_{ESR} = \frac{1}{2\pi \cdot C_{OUT} \cdot ESR}$$

- Compensation Network singularities frequencies:

  a) $$F_Z = \frac{1}{2\pi \cdot R_F \cdot C_F}$$

  b) $$F_P = \frac{1}{2\pi \cdot R_F \cdot \left(\frac{C_F \cdot C_P}{C_F + C_P}\right)}$$

Type II compensation relies on the zero introduced by the output capacitors bank to achieve stability. Thus, a needed condition to successfully apply type II compensation is $F_{ESR} < F_{0dB}$ (usually true when output capacitor is based on electrolytic, aluminium electrolytic or tantalum capacitor).

To define compensation network components values, the below suggestions may be followed:

a) Set the output resistor divider in order to obtain the desired output voltage:

$$\frac{R_{FB}}{R_{OS}} = \frac{V_{OUT}}{V_{REF}} - 1$$

Usual values of R_{FB} and R_{OS} ranges from some hundreds of Ω to some kΩ (consider trade-off between power dissipation on output resistor divider and offset introduced by FB bias current).

If the desired output voltage is equal to internal reference, R_{OS} has to be NC and FB pin can be directly connected to V_{OUT}.

b) Set R_F in order to obtain the desired closed loop regulator bandwidth according to the approximated formula:

$$R_F = \frac{F_{0dB} \cdot F_{ESR}}{F_{LC}^2} \cdot \frac{\Delta V_{OSC}}{V_{IN}} \cdot \frac{1}{gm} \cdot \frac{R_{FB} + R_{OS}}{R_{OS}}$$

If $V_{OUT} = V_{REF}$, just consider $(R_{FB}+R_{OS})/R_{OS}$ factor equal to 1.

c) Place F_Z below F_{LC} (typically $0.2 \cdot F_{LC}$):

$$C_F = \frac{5}{2\pi \cdot R_F \cdot F_{LC}}$$

d) Place F_P at $0.5 \cdot F_{SW}$:

$$C_P = \frac{C_F}{\pi \cdot R_F \cdot C_F \cdot F_{SW} - 1} \cong \frac{1}{\pi \cdot R_F \cdot F_{SW}}$$

e) Check that compensation network gain is lower than open loop transconductance EA gain.

f) Estimate phase margin obtained (it should be greater than 45°) and repeat, modifying parameters, if necessary.

8.3 Soft Start time calculation

To calculate SS time (t_{SS}), the following approximated equation can be used ($C_P << C_F$):

$$t_{SS} = \frac{C_F \cdot \frac{V_{OUT}}{V_{IN}} \cdot \Delta V_{OSC}}{I_{SS}}$$

The previous equation refers only to V_{OUT} ramp up time. The time elapsed from the end of OC setting phase or COMP set free to the beginning of V_{OUT} ramp up (see *Figure 6*) can be approximately estimated as follow:

$$t_{delay} = \frac{C_F \cdot 0.8V}{I_{SS}}$$

Once calculated t_{SS}, also the current delivered by the converter during SS to charge the output capacitor bank can be estimated:

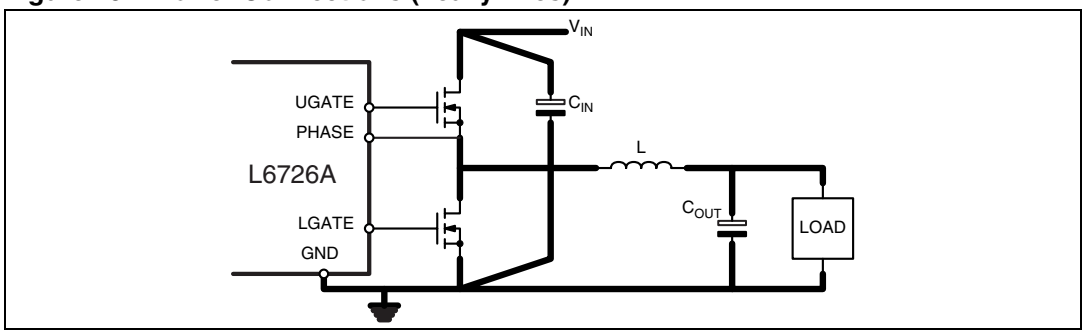
$$I_{startup} = \frac{C_{OUT} \cdot V_{OUT}}{t_{SS}}$$

8.4 Layout guidelines

L6726A provides control functions and high current integrated drivers to implement high-current step-down DC-DC converters. In this kind of application, a good layout is very important.

The first priority when placing components for these applications has to be reserved to the power section, minimizing the length of each connection and loop as much as possible. To minimize noise and voltage spikes (EMI and losses) power connections (highlighted in *Figure 10*) must be a part of a power plane and anyway realized by wide and thick copper traces: loop must be anyway minimized. The critical components, i.e. the power MOSFETs, must be close one to the other. The use of multi-layer printed circuit board is recommended.

Figure 10. Power Connections (heavy lines)



The input capacitance (C_{IN}), or at least a portion of the total capacitance needed, has to be placed close to the power section in order to eliminate the stray inductance generated by the copper traces. Low ESR and ESL capacitors are preferred, MLCC are suggested to be connected near the HS drain.

Use proper VIAs number when power traces have to move between different planes on the PCB in order to reduce both parasitic resistance and inductance. Moreover, reproducing the same high-current trace on more than one PCB layer will reduce the parasitic resistance associated to that connection.

Connect output bulk capacitors (C_{OUT}) as near as possible to the load, minimizing parasitic inductance and resistance associated to the copper trace, also adding extra decoupling capacitors along the way to the load when this results in being far from the bulk capacitors bank.

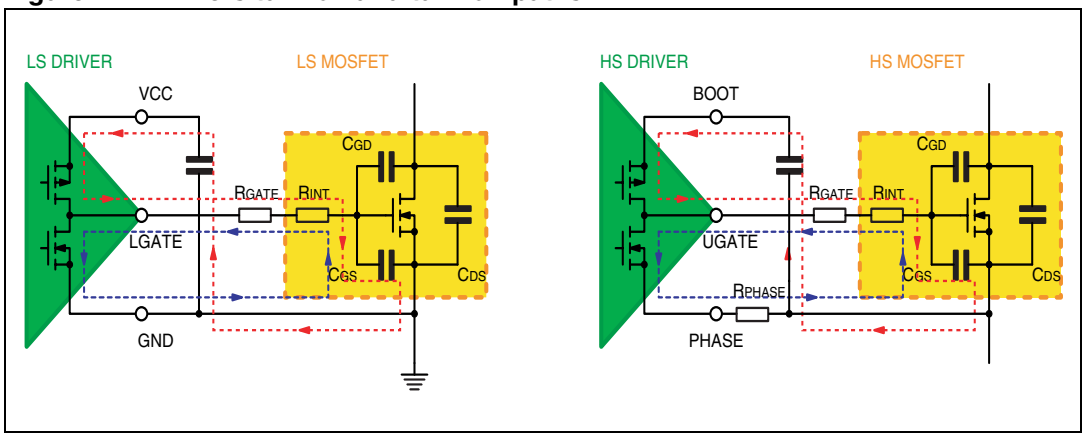
Gate traces and phase trace must be sized according to the driver RMS current delivered to the power MOSFET. The device robustness allows managing applications with the power

section far from the controller without losing performances. Anyway, when possible, it is recommended to minimize the distance between controller and power section. See *Figure 11* for drivers current paths.

Small signal components and connections to critical nodes of the application, as well as bypass capacitors for the device supply, are also important. Locate bypass capacitor (VCC and Bootstrap capacitor) and loop compensation components as close to the device as practical. For over current programmability, place R_{OCSET} close to the device and avoid leakage current paths on LGATE / OC pin, since the internal current source is only 10µA

Systems that do not use Schottky diode in parallel to the Low-Side MOSFET might show big negative spikes on the PHASE pin. This spike must be limited within the absolute maximum ratings (for example, adding a gate resistor in series to HS MOSFET gate, or a phase resistor in series to PHASE pin), as well as the positive spike, but has an additional consequence: it causes the bootstrap capacitor to be over-charged. This extra-charge can cause, in the worst case condition of maximum input voltage and during particular transients, that boot-to-phase voltage overcomes the absolute maximum ratings also causing device failures. It is then suggested in this case to limit this extra-charge by adding a small resistor in series to the bootstrap diode (R_D in *Figure 1*).

Figure 11. Drivers turn-on and turn-off paths



8.5 Embedding L6726A-based VRs…

When embedding the VR into the application, additional care must be taken since the whole VR is a switching DC/DC regulator and the most common system in which it has to work is a digital system such as MB or similar. In fact, latest MBs have become faster and more powerful: high speed data busses are more and more common and switching-induced noise produced by the VR can affect data integrity if additional layout guidelines are not followed. Few easy points must be considered mainly when routing traces in which switching high currents flow (switching high currents cause voltage spikes across the stray inductance of the traces causing noise that can affect the near traces):

When reproducing high current path on internal layers, keep all layers the same size in order to avoid "surrounding" effects that increase noise coupling.

Keep safe guard distance between high current switching VR traces and data busses, especially if high-speed data busses, to minimize noise coupling.

Keep safe guard distance or filter properly when routing bias traces for I/O sub-systems that must walk near the VR.

Possible causes of noise can be located in the PHASE connections, MOSFETs gate drive and Input voltage path (from input bulk capacitors and HS drain). Also GND connection must be considered if not insisting on a power ground plane. These connections must be carefully kept far away from noise-sensitive data busses.

Since the generated noise is mainly due to the switching activity of the VR, noise emissions depend on how fast the current switches. To reduce noise emission levels, it is also possible, in addition to the previous guidelines, to reduce the current slope and thus to increase the switching times: this will cause, as a consequence of the higher switching time, an increase in switching losses that must be considered in the thermal design of the system.

9 Package mechanical data

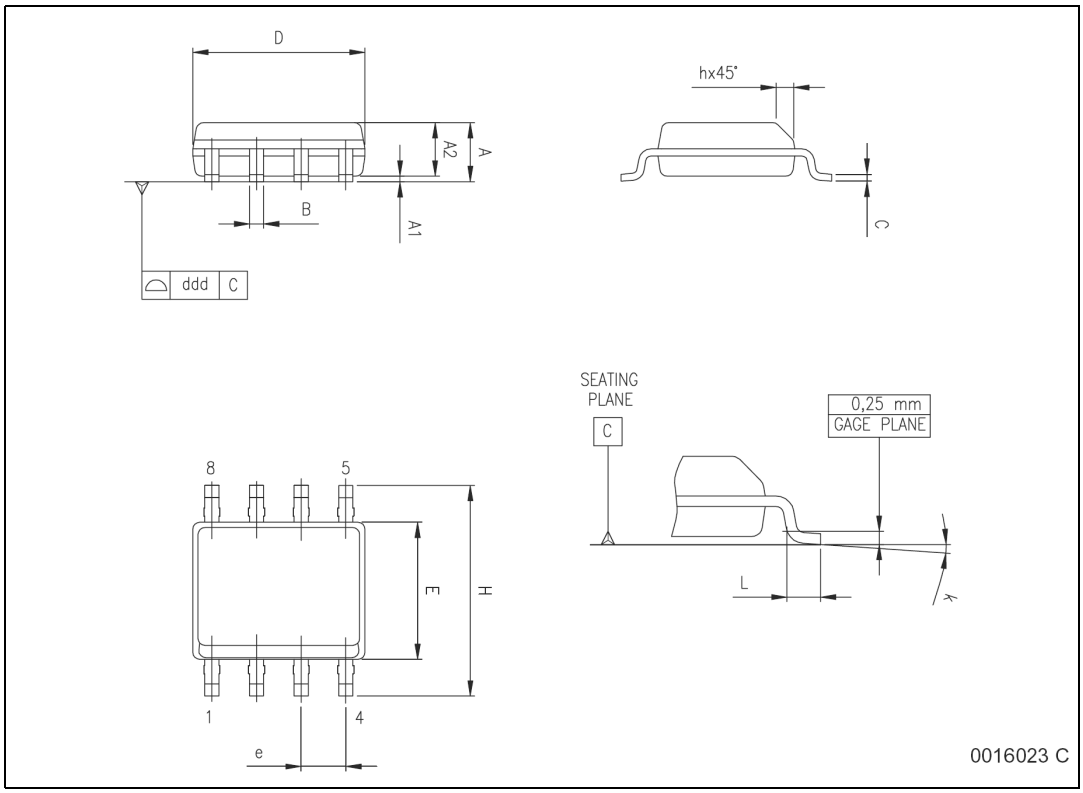
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 5. SO-8 Mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D (1)	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

1. D and F does not include mold flash or protrusions. Mold flash or potrusions shall not exceed 0.15mm (.006inch) per side.

Figure 12. Package dimensions



10 Revision history

Table 6. Revision history

Date	Revision	Changes
16-Oct-2006	1.0	Initial release.
26-Oct-2006	2.0	Mechanical data dimensions updated

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