ANALOG Switch

with LSTTL–Compatible Inputs

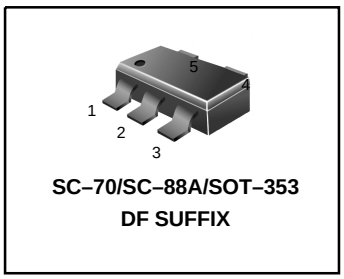
L74VHC1GT66

The L74VHC1GT66 is an advanced high speed CMOS bilateral analog switch fabricated with silicon gate CMOS technology. It achieves high speed propagation delays and low ON resistances while maintaining low power dissipation. This bilateral switch controls analog and digital voltages that may vary across the full power–supply range (from VCC to GND).

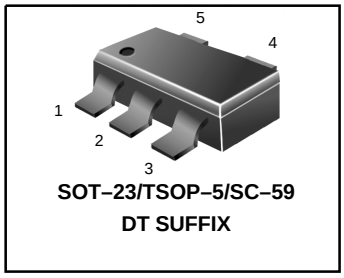
The L74VHC1GT66 is compatible in function to a single gate of the very High Speed CMOS MC74VHCT4066. The device has been designed so that the ON resistances (RON) are much lower and more linear over input voltage.

The ON/OFF Control input is compatible with TTL–type input thresholds allowing the device to be used as a logic–level translator from 3.0 V CMOS logic to 5.0 V CMOS logic or from 1.8 V CMOS logic to 3.0 V CMOS logic while operating at the high–voltage power supply. The input protection circuitry on this device allows overvoltage tolerance on the input, which provides protection when voltages of up to 7 V are applied, regardless of the supply voltage. This allows the L74VHC1GT66 to be used to interface 5 V circuits to 3 V circuits.

- High Speed: t_{PD} = 20 ns (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 1 μA (Max) at T_A = 25°C
- Diode Protection Provided on Inputs and Outputs
- Improved Linearity and Lower ON Resistance over Input Voltage
- On/Off Control Input Has OVT
- We declare that the material of product is ROHS compliant and halogen free.

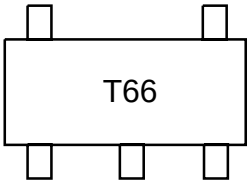


SC–70/SC–88A/SOT–353
DF SUFFIX



SOT–23/TSOP–5/SC–59
DT SUFFIX

MARKING DIAGRAMS



Pin 1

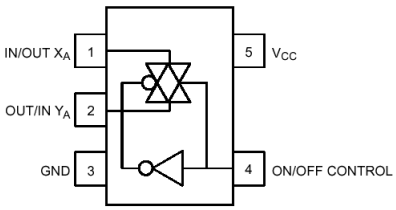


Figure 1. Pinout (Top View)

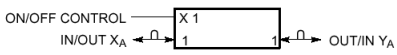


Figure 2. Logic Symbol

PIN ASSIGNMENT	
1	IN/OUT X_A
2	OUT/IN Y_A
3	GND
4	ON/OFF CONTROL
5	V_{CC}

FUNCTION TABLE

On / Off Control Input	State Analog Switch
L	Off
H	On

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

L74VHC1GT66

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		– 0.5 to + 7.0	V
V_{IN}	DC Input Voltage		– 0.5 to +7.0	V
V_{IS}	Analog Output Voltage		–0.5 to +7.0	V
I_{IK}	Input Diode Current		–20	mA
I_{CC}	DC Supply Current, V_{CC} and GND		+25	mA
P_D	Power dissipation in still air	SC–88A (Note 2.)	200	mW
		TSOP5 (Note 2.)	450	
T_L	Lead Temperature, 1 mm from Case for 10 s		260	°C
T_{stg}	Storage temperature		–65 to +150	°C
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 3)	>5000	V
		Machine Model (Note 4)	> 400	
		Charged Device Model (Note 5)	N/A	
$I_{LATCH-UP}$	Latch–Up Performance	Above V_{CC} and Below GND at 125°C (Note 6)	Class 2	

1. Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions eyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.
2. Derating – SC–88A Package: –3 mW/°C from 65°C to 125°C
   – TSOP5 Package: –6 mW/°C from 65°C to 125°C
3. Tested to EIA/JESD22–A114–A
4. Tested to EIA/JESD22–A115–A
5. Tested to JESD22–C101–A
6. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage		GND	5.5	V
V_{IS}	Analog Input Voltage		GND	V_{CC}	V
T_A	Operating Temperature Range		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3 ± 0.3 V	0	100	ns/V
		V_{CC} = 5.0 ± 0.5 V	0	20	

The θ_{JA} of the package is equal to 1/Derating. Higher junction temperatures may affect the expected lifetime of the device per the table and figure below.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

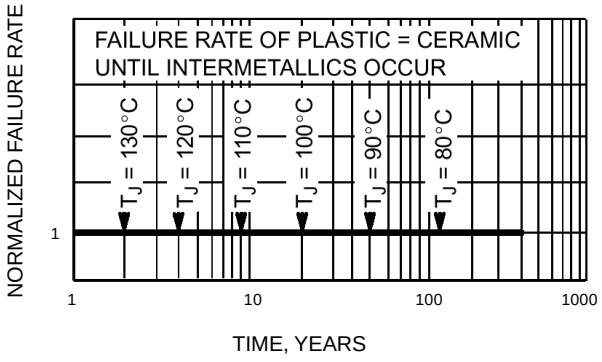


Figure 3. Failure Rate vs. Time Junction Temperature

L74VHC1GT66

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Max	$T_A \leq$ 85°C Min	$T_A \leq$ 85°C Max	$T_A \leq$ 125°C Min	$T_A \leq$ 125°C Max	Unit
V_{IH}	Minimum High–Level Input Voltage On/Off Control Input	R_{ON}=Per Spec	3.0	1.2		1.2		1.2		V
			4.5	2.0		2.0		2.0		
			5.5	2.0		2.0		2.0		
V_{IL}	Maximum Low–Level Input Voltage	R_{ON}=Per Spec	3.0		0.53		0.53		0.53	V
			4.5		0.8		0.8		0.8	
			5.5		0.8		0.8		0.8	
I_{IN}	Maximum Input Leakage Current On/Off Control Input	V_{IN} =x V_{cc} or GND	0 to 5.5		±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5		1.0		20		40	μA
I_{CCT}	Quiescent Supply Current	On/Off Control at 3.4 V	5.5		1.35		1.50		1.65	mA
R_{ON}	Maximum "ON" Resistance	V_{IN} = V_{IH}	3.0		60		70		100	Ω
		V_{IS} = V_{CC} or GND	4.5		45		50		60	
		$|I_{IS}| \leq$10 mA (Figure 4.)	5.5		40		45		55	
I_{OFF}	Maximum Off–Channel Leakage Current	V_{IN} = V_{IL} V_{IS} = V_{CC} or GND Switch Off (Figure 5.)	5.5		0.1		0.5		1.0	mA

AC ELECTRICAL CHARACTERISTICS C_{load} = 50 pF, Input t_r / t_f = 3.0 ns

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \leq$ 85°C Min	$T_A \leq$ 85°C Max	–55°C≤T_A≤125°C Min	–55°C≤T_A≤125°C Max	Unit
t_{PLH}, t_{PHL}	Maximum Propogation Delay, Input X to Y	Y_A = Open (Figure 14.)	2.0		1	5		6		7	ns
			3.0		0	2		3		4	
			4.5		0	1		1		2	
			5.5		0	1		1		1	
t_{PLZ}, t_{PHZ}	Maximum Propogation Delay, ON/OFF Control to Analog Output	R_L = 1000 Ω (Figure 15.)	2.0		32	40		45		50	ns
			3.0		28	35		40		45	
			4.5		24	30		35		40	
			5.5		20	25		30		35	
t_{PZL}, t_{PZH}	Maximum Propogation Delay, ON/OFF Control to Analog Output	R_L = 1000 Ω (Figure 15.)	2.0		32	40		45		50	ns
			3.0		28	35		40		45	
			4.5		24	30		35		40	
			5.5		20	25		30		35	
C_{IN}	Maximum Input Capacitance	ON/OFF Control Input	0.0		3	10		10		10	pF
		Contol Input = GND	5.0								
		Analog I/O			4	10		10		10	
		Feedthrough			4	10		10		10	

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 6)	18	pF

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

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ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Test Conditions	V_{CC}	Limit 25°C	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 10.)	f_{in} = 1 MHz Sine Wave Adjust f_{in} voltage to obtain 0 dBm at V_{OS} Increase f_{in} = frequency until dB meter reads –3 dB R_L = 50 Ω, C_L = 10 pF	3.0 4.5 5.5	150 175 180	MHz
ISO_{off}	Off–Channel Feedthrough Isolation (Figure 11.)	f_{in} = Sine Wave Adjust f_{in} voltage to obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	3.0 4.5 5.5	–80 –80 –80	dB
$NOISE_{feed}$	Feedthrough Noise Control to Switch (Figure 12.)	V_{in}≤1 MHz Square Wave ($t_r = t_f$ = 2ns) Adjust R_L at setup so that I_s = 0 A R_L = 600 Ω, C_L = 50 pF	3.0 4.5 5.5	45 60 130	mV_{PP}
THD	Total Harmonic Distortion (Figure 13.)	f_{in} = 1 kHz, R_L = 10 k Ω, C_L = 50 pF THD = $THD_{Measured}$ – THD_{Source} V_{IS} = 3.0 V_{PP} sine wave V_{IS} = 5.0 V_{PP} sine wave	 3.3 5.5	 0.30 0.15	%

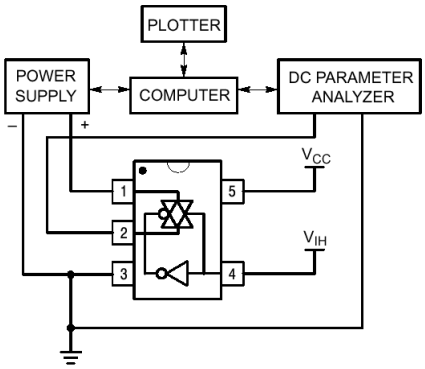

Figure 4. On Resistance Test Set–Up

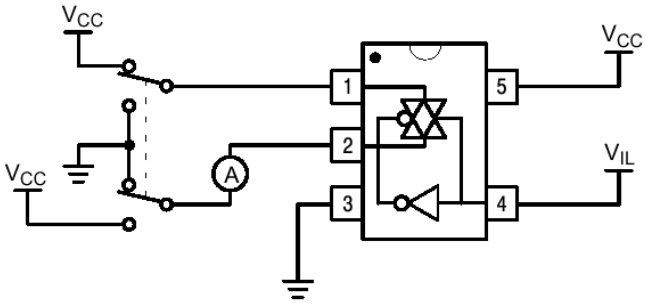

Figure 5. Maximum Off–Channel Leakage Current Test Set–Up

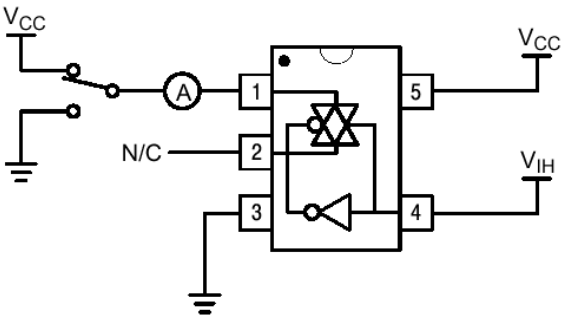

Figure 6. Maximum On–Channel Leakage Current Test Set–Up

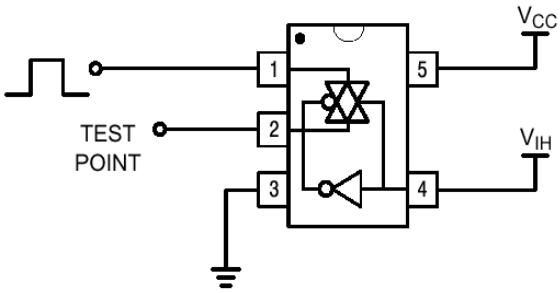

Figure 7. Propagation Delay Test Set–Up

L74VHC1GT66

Switch to Position 1 when testing t_{PLZ} and t_{PZL}
Switch to Position 2 when testing t_{PHZ} and t_{PZH}

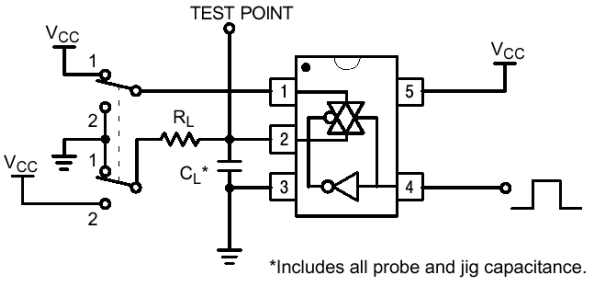

Figure 8. Propagation Delay Output Enable/Disable Test Set–Up

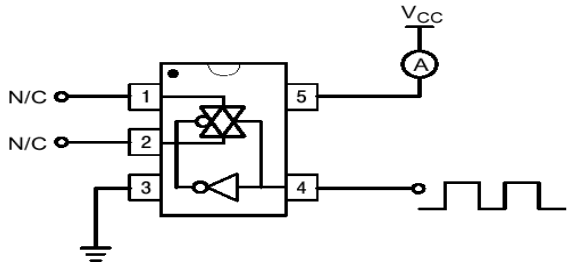

Figure 9. Power Dissipation Capacitance Test Set–Up

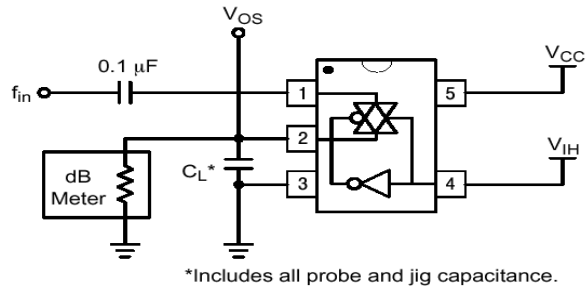

Figure 10. Maximum On–Channel Bandwidth Test Set–Up

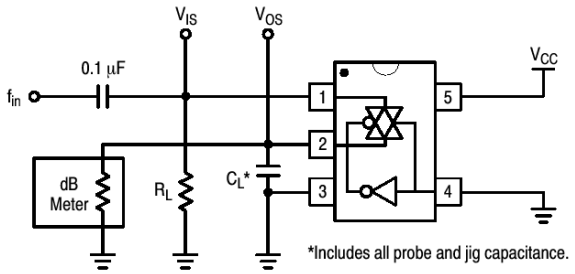

Figure 11. Off–Channel Feedthrough Isolation Test Set–Up

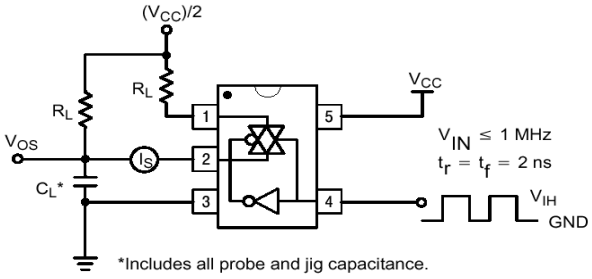

Figure 12. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set–Up

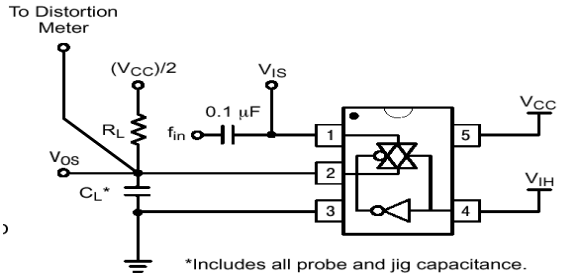

Figure 13. Total Harmonic Distortion Test Set–Up

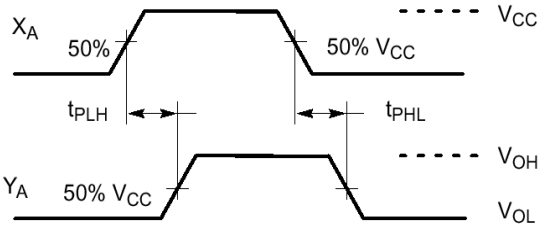

Figure 14. Propagation Delay, Analog In to Analog Out Waveforms

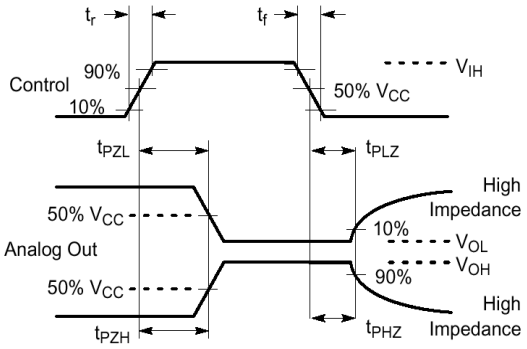

Figure 15. Propagation Delay, ON/OFF Control

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type (Name/SOT#/ Common Name)	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
L74VHC1GT66DFT1	L	74	VHC1G	T66	DF	T1	SC–70/SC–88A/ SOT–353	178 mm (7 in) 3000 Unit
L74VHC1GT66DFT2	L	74	VHC1G	T66	DF	T2	SC–70/SC–88A/ SOT–353	178 mm (7 in) 3000 Unit
L74VHC1GT66DFT4	L	74	VHC1G	T66	DF	T4	SC–70/SC–88A/ SOT–353	330 mm (13 in) 10,000 Unit
L74VHC1GT66DTT1	L	74	VHC1G	T66	DT	T1	SOT–23/TSOPS/ SC–59	178 mm (7 in) 3000 Unit
L74VHC1GT66DTT3	L	74	VHC1G	T66	DT	T3	SOT–23/TSOPS/ SC–59	330 mm (13 in) 10,000 Unit