

## Dual DMOS full bridge stepper/DC motor driver

Preliminary Data

### Features

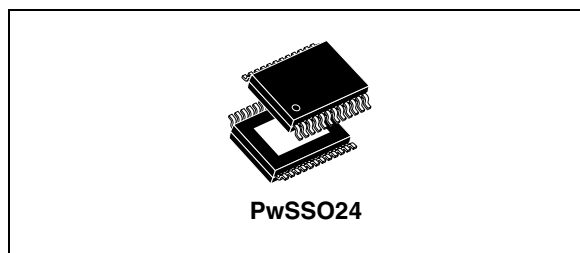
- Flexible Motor Driver configurations:
  - Dual Full Bridge for one bipolar Stepping motor.
  - Dual or single DC motor driver.
- Programmable by two input pins to achieve one of the following functionalities:
  - Pin to pin compatible with ST L6219 or
  - Stepping motor direct control with 8 current levels or
  - Driver parameters control by means of Serial Port.
- Mixed Decay.
- Micro stepping function.
- BCD5 technology (No Charge Pump required).
- Supply Range from 8V to 38V.
- $I_{OUT}$  up to 1.2A (1.5A peak).
- $R_{DSon}$  = 0.85 $\Omega$  (typ) for each switch.
- Input logic level compatible with 3.3V or 5V control signals.
- Package: PwSSO24.

### Description

This IC is designed to be very flexible in driving Stepping or DC motors.

By connecting to Vcc or to Gnd two program pins (pin 7 and 18) the user has the possibility to set up the device in different configurations.

1. The first configuration is an identical application of ST L6219 but with increased current. In this configuration L8229 provides a continuous current of the output stage up to 1.2A (1.5A peak).
2. The second configuration allows a functionality similar to previous one but with the possibility of choosing 8 different current



levels to perform a more accurate stepping functionality. This is achieved by multiplexing the input pins dedicated to set the level of the current. Additionally the user can set the mixed mode decay for current recirculation.

- 3,4. The third and fourth configurations are intended to provide a very flexible programming for several parameters useful to drive different kind of Stepping and DC motors. This is achieved by means of a serial port interface that allows the user to configure the following parameters:
  - a) Current levels (32 values for each bridge).
  - b) Current direction.
  - c) Type of decay for Stepping motors (Mix/Slow) or for DC motors (Fast/Slow).
  - d) Vref input (Ext/Int).
  - e) Vref divider (:5/:10).
  - f) Blanking time (4 values).
  - g) Oscillator freq divider (4 values).
  - h) Off time (32 values).
  - i) Fast decay time (16 values).
  - j) Synchronous rectification.

The functionalities of the two configurations are identical except that the internal bit address (first bit of SPI words) can be programmed to be 1 or 0: this enables two different L8229 to share a common serial bus.

### Order code

Part number	Package	Packing
L8229	PwSSO24	Tube

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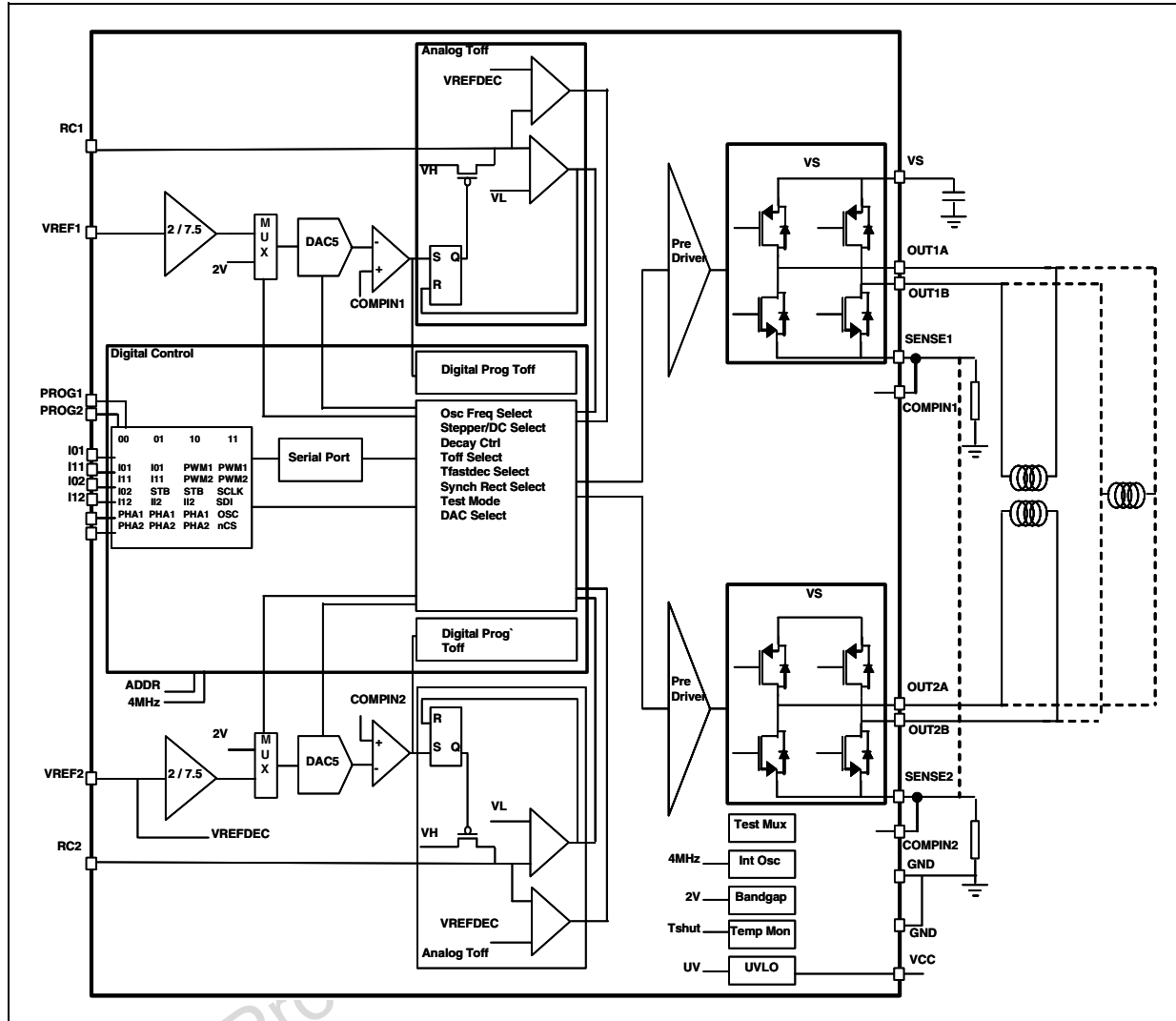
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Obsolete Product(s) - Obsolete Product(s)

# 1 Block diagram

Figure 1. Block Diagram

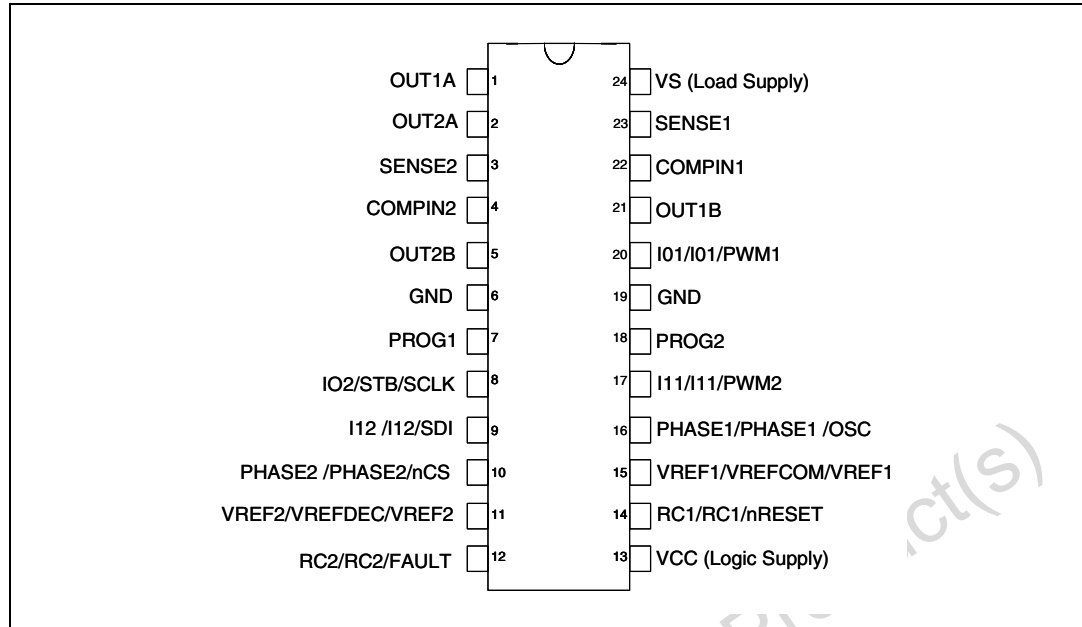


Note: The sensing resistors used for the stepping motor configurations must be not inductive.

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## 2 Pin description

Figure 2. Pin Connection (Top view)



Note: The pin functionality is different according to different configurations, so the relative pin function and name are different: the first name is relative to first configuration (L6219\_HI), the second name is relative to second configuration (L6219\_8), and the third name is relative to third and fourth configuration (L8229\_0 and L8229\_1).

Table 1. Pin Description

Pin N#	L6219_HI (Pin7&18=00)	L6219_8 (Pin7&18=01)	L8229_x (Pin7&18=10 or 11)	Function
1	OUT1A			Motor Driver Bridge 1 Output A.
2	OUT2A			Motor Driver Bridge 2 Output A.
3	SENSE2			Motor Driver Bridge 2 Sense Resistor.
4	COMPIN2			Current Comparator input for Bridge2.
5	OUT2B			Motor Driver Bridge 2 Output B.
6	GND			Ground.
7	PROG1			Configuration Program pin. When used together with pin 18, it programs device into one of the four configurations (see following Programmable Modes table)
8	IO2	STB	SCLK	I02: Current level control bit for Bridge 2. STB: Strobe input pin for current setting. SCLK: Clock input pin for serial protocol.
9	I12	I12	SDI	I12: Current level control bit for Bridge 2. SDI: Data input pin for serial protocol.

Table 1. Pin Description (continued)

Pin N#	L6219_HI (Pin7&18=00)	L6219_8 (Pin7&18=01)	L8229_x (Pin7&18=10 or 11)	Function
10	PHASE2	PHASE2	nCS	PHASE2: Direction input control pin for Bridge 2. nCS: Chip Select input pin for serial protocol.
11	VREF2	VREFDEC	VREF2	VREF2: Reference voltage input for Bridge 2. VREFDEC: Mixed Decay Reference voltage for both Bridges 1 and 2.
12	RC2	RC2	FAULT	RC2: Toff input pin for Bridge 2. FAULT: This pin is high when a generic fault is present.
13	VCC			Logic and Low voltage analog Supply.
14	RC1	RC1	nRESET	RC1: Toff input pin for Bridge 1. nRESET: Input pin for reset of serial port.
15	VREF1	VREFCOM	VREF1	VREF1: Reference voltage input for Bridge 1. VREFCOM: Common Reference voltage input for both Bridges 1 and 2.
16	PHASE1	PHASE1	OSC	PHASE1: Direction input control pin for Bridge 1. OSC: Input for external oscillator used for timings.
17	I11	I11	PWM2	I11: Current level control bit for Bridge 1. PWM2: PWM input control pin for Bridge 2 when used as a DC motor driver.
18	PROG2			Configuration Program pin. When used together with pin 7, it programs device into one of the four configurations (see following Programmable Modes table).
19	GND			Ground.
20	I01	I01	PWM1	I01: Current level control bit for Bridge 1. PWM1: PWM input control pin for bridge 1 when used as a DC motor driver
21	OUT1B			Motor Driver Bridge 1 Output B.
22	COMPIN1			Current Comparator input for Bridge1.
23	SENSE1			Motor Driver Bridge 1 Sense Resistor.
24	VS			Supply voltage for output stages.

Note: ESD on pin PROG1 vs.  $V_S$  is guaranteed up to +2KV/-1.75KV (Human Body Model, 1500Ohm, 100pF)



**Table 2. Programmable modes**

Pin #7 PROG1	Pin # 18 PROG2	Description	Mode name	Drive Configurations
0	0	L6219 compatible (up to 1.2A Iout)	L6219_HI	1 x Stepping MotorDriver.
0	1	L6219 like with 8 current levels (up to 1.2A Iout) and Mixed Decay.	L6219_8	1 x Stepping MotorDriver.
1	0	SPI operation, Chip Address = 0	L8229_0	1 x Stepping MotorDriver or 2 x DC Motor Driver.
1	1	SPI operation, Chip Address = 1	L8229_1	1 x Stepping MotorDriver or 2 x DC Motor Driver.

Obsolete Product(s) - Obsolete Product(s)

### 3 Electrical Characteristics

Independently from the selected configurations, L8229 has some electrical characteristics that are common for all modes. These are listed below while specific characteristics are listed in their respective functionality descriptions.

In all modes L8229 is powered by  $V_s$  supply voltage. The anti cross-conduction delay is controlled to provide sufficient time for cross-conduction suppression so that at no time both the upper and lower output devices (on the same side of the H bridge) are allowed to conduct simultaneously.

During an over-temperature event, when the device  $T_j$  is above  $T_j(\text{shutdown})$ , the internal thermal protection circuit disables the drive outputs until the device temperature drops below the lower thermal threshold temperature.

*Note:* The programming pins, *PROG1* and *PROG2*, must be soldered to *Vcc* or to *GND* and must not be driven when supplies are on.

#### 3.1 Absolute maximum ratings

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_s$	Supply voltage (including ripple).	40	V
$V_{cc}$	Logic and Low voltage analog supply voltage	7	V
$I_{peak}$	Motor Driver Output Peak Current (see Note <sup>(1)</sup> ).	1.5	A
$V_{ref}$	$V_{ref}$ input voltage.	7.5	V
$V_{sense}$	$V_{sense}$ output voltage.	2	V
$V_{in}$	Logic input voltage.	-0.3 to +7	V
$T_j$	Junction Temperature.	170	°C
$T_{stg}$	Storage Temperature.	-25 to 150	°C

1. This peak current is intended as start up current for max 1 second with D.C.  $\leq 10\%$

#### 3.2 Operating ratings

**Table 4. Operating ratings ( $0^\circ\text{C} \leq T_j \leq 125^\circ\text{C}$ )**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_s$	Supply voltage (including ripple).		8.5	32	38	V
$V_{cc}$	Logic and Low voltage analog supply voltage.		3.135	5	5.25	V
$I_{Vs}$	$V_s$ Standby Current	L8229_0/1 configuration Sleep mode: NSLEEP (W1, bit3) = 0		3	6	mA

Table 4. Operating ratings ( $0^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$ ) (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$I_{VCC_{L6219}}$	Vcc total supply current (L6219_HI and L6219_8 modes)	Vcc=5.25V			7	mA
$I_{VCC_{L8229\_0/1}}$	Vcc total supply current (L8229_0 or L8229_1 mode)	Vcc=5.25V			7	mA
		Vcc=5.25V, NSLEEP (W1, bit3) = 0			3	mA
Vin	Logic input voltage		0		Vcc	V
Iout	Motor Driver Output Current (continuous)				1.2	A

### 3.3 General electrical characteristics

( $0^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$ ,  $V_S = 32\text{V}$ , unless otherwise specified)

#### 3.3.1 Output Drivers (OUTA or OUTB)

Table 5. Output Drivers (OUTA or OUTB)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$R_{DSON}$	Output ON Resistance ( $T_j = 70^{\circ}\text{C}$ )	Source Driver, $I_{LOAD} = -1.2\text{A}$			1.3	$\Omega$
		Sink Driver, $I_{LOAD} = +1.2\text{A}$			1.3	$\Omega$
Icex	Output leakage current	Vout = Vs or Gnd		50		$\mu\text{A}$
$V_F$	Body Diode Forward Voltage	Sink Diode, $I_F = 1.2\text{A}$		1	1.5	V
		Source Diode, $I_F = 1.2\text{A}$		1	1.5	V
tr	Output rising time	Vs=12V, $R_L=12\Omega$ connected to Vs or Gnd	100		350	ns
		Vs=24V, $R_L=38\Omega$ connected to Vs or Gnd				
		Vs=36V, $R_L=58\Omega$ connected to Vs or Gnd				
tf	Output falling time	Vs=12V, $R_L=12\Omega$ connected to Vs or Gnd	75		300	ns
		Vs=24V, $R_L=38\Omega$ connected to Vs or Gnd				
		Vs=36V, $R_L=58\Omega$ connected to Vs or Gnd				
Tdead	Shoot through delay			1		$\mu\text{A}$

### 3.3.2 Control Logic pins

Table 6. Control Logic pins

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{IN(H)}$	Input Voltage	All logic input for $V_{CC} = 3.3V$ or $5V$ .	2			V
$V_{IN(L)}$	Input Voltage	All logic input for $V_{CC} = 3.3V$ or $5V$ .			0.8	V
$I_{IN(H)}$	Input Current	$V_{IN} = 2.0V$	-20		20	$\mu A$
$I_{IN(L)}$	Input Current	$V_{IN} = 0.8V$	-20		20	$\mu A$
$I_{sdi}$	SDI Input Current		-200		50	$\mu A$

### 3.3.3 Analog Input Pins

Table 7. Analog Input Pins

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
$V_{ref}$	$V_{ref}$ Input Voltage		1.5		7.5	V
$I_{Vref}$	$V_{ref}$ Input Current	$V_{ref} = 5.0V$			200	$\mu A$
$V_{compin}$	$V_{compin}$ Input Voltage				0.75	V
$I_{compin}$	$V_{compin}$ Input Current			1	20	$\mu A$
$V_{sense}$	$V_{sense}$ Input Voltage				0.75	V
$I_{sense}$	$V_{sense}$ Output Current			50	100	$\mu A$

### 3.3.4 General

Table 8. General

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{sc\_off}$	Sense comparator offset			$\pm 10$		mV
$V_{s\_UV}$	$V_s$ undervoltage threshold			7.5		V
$V_{s\_UVhys}$	$V_s$ undervoltage hysteresis			300		mV
$V_{cc\_UV}$	$V_{CC}$ undervoltage threshold			2.9		V
$V_{cc\_UVhys}$	$V_{CC}$ undervoltage hysteresis			150		mV
$T_j(\text{shutdown})$	Thermal shutdown junction temperature			160		$^{\circ}C$
$T_j(\text{enable\_hysteresis})$	Thermal enable junction temperature hysteresis			25		$^{\circ}C$

## 4 L6219\_HI and L6219\_8 modes

When configured in one of these modes the device has a functionality similar to ST L6219 with some improvements. The output stage is made by LDMOS devices instead of the BJT present in ST L6219. This allows a reduced saturation drop and an higher current handling with similar power dissipation. Additionally the recirculation diodes are internally available as a part of the LDMOS structure.

In case of:

- a) Undervoltage detection (UVD) or
- b) Thermal shutdown (TSD),

the outputs will be in Hi-Z mode (all outputs off) respectively until the supplies voltage goes over the UV threshold plus hysteresis or the themperature decreases below TSD threshold minus hysteresis.

In case of:

- c) Overcurrent detection (OCD)

the outputs will be in Hi-Z mode (all outputs off) and will remain in this condition until the device is reset by turning off and on VCC supply voltage.

Common electrical characteristics of both L6219\_HI and L6219\_8 modes are listed below, while specific characteristics are listed in their respective functionality descriptions.

## 5 L6219\_HI and L6219\_8 Electrical characteristics

( $0^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$ ,  $V_S = 32\text{ V}$ , unless otherwise specified)

### 5.1 DC specifications

Table 9. DC specifications

Symbol	Description	Condition	Min	Typ	Max	Unit
Vref/Vsense	Current Limit Threshold (at trip point ) for $V_{\text{ref}} = 5\text{V}$ and $T_j \leq 70^{\circ}\text{C}$	$I_0 \leq 0.8\text{V}$ , $I_1 \leq 0.8\text{V}$	9.25	10	10.5	
		$I_0 \geq 2.0\text{V}$ , $I_1 \leq 0.8\text{V}$	13.5	15	16.5	
		$I_0 \leq 0.8\text{V}$ , $I_1 \geq 2.0\text{V}$	25.5	30	34.5	

### 5.2 AC/transient specifications

Table 10. AC/transient specifications

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Toff	Cut off time	$R_t=56\text{Kohm}$ , $C_t =820\text{pF}$		50		$\mu\text{A}$
Tdelay	Turn Off Delay for comparator			1		$\mu\text{A}$
Tblank	Blanking time for Sense comparator			1		$\mu\text{A}$

## 6 L6219\_HI mode

The device will be set into the L6219\_HI mode by asserting PROG1 and PROG2 pins (pin 7 and 18) to 00.

In the L6219\_HI mode, the device is pin and function compatible with the ST L6219 device. Please note that while ST L6219 allows good power dissipation by simply connecting to gnd the center pins because of the batwing frame, the L8229 power dissipation will be good only by connecting the exposed pad to a proper heat sink.

The circuit is intended to drive both windings of a bipolar stepping motor. The peak current control is made through switch mode regulation. There is a choice of three different current levels with the two logic inputs I01 and I11 for winding 1 and I02 and I12 for winding 2. The current can also be completely switched off.

### 6.1 Input Logic (I0 and I1)

The current level in the motor winding is selected with these inputs (see [Figure 1](#)). If any of the logic inputs is left open, the circuit will treat it as a high level input.

**Table 11. Input Logic (I0 and I1)**

I0X	I1X	Current Level
H	H	No Current
L	H	Low Current: 1/3 I <sub>o max</sub>
H	L	Medium Current: 2/3 I <sub>o max</sub>
L	L	Maximum Current: I <sub>o max</sub>

### 6.2 Phase

This input pin determines the direction of current flow in the windings, depending on the motor connections. The signal is fed through a Schmitt trigger for noise immunity, and through a time delay in order to guarantee that no cross conduction occurs in the output stage during phase-shift. High level on the PHASE input causes the motor current to flow from OutA through the motor winding to OutB.

### 6.3 Current Sensing

This part contains a low pass filter for the external current sensing resistor (R<sub>s</sub>) and three comparators. Only one comparator is active at a time: it is activated by the input logic according to the current level chosen with signals I0 and I1.

The motor current flows through the sensing resistor R<sub>s</sub> and when the current has increased so that the voltage across R<sub>s</sub> becomes higher than the reference voltage on the other comparator input, the comparator output goes high, triggering the pulse generator.

The max peak current I<sub>max</sub> can be defined by:

$$I_{max} = V_{ref} / 10 R_s$$

Note that  $I_{out\ max}$  is 1.2A and the wide range allowed for  $V_{ref}$  requires the choice of a suitable sense resistor to prevent current range over the maximum.

## 6.4 Single-pulse Generator

The pulse generator is a monostable circuit triggered on the positive going edge of the comparator output. The circuit output is high during the pulse time  $T_{off}$  that is determined by the time components  $R_t$  and  $C_t$ .

$$T_{off} \approx 1.1 \times R_t C_t$$

(including switching dead time)

The single pulse turns off the power switch connected to the motor winding, causing the winding current to decrease during  $T_{off}$ . If a new trigger signal should occur during  $T_{off}$  it will be ignored.

## 6.5 Output Stage

Each of the two outputs stage contains four LDMOS transistors (P and N channel) connected in two H Bridges. The intrinsic body diode of the LDMOS serve as recirculation diode for flyback current.

The LDMOS are used to switch the power supply to the motor winding, thus driving a constant current through the winding. It should be noted however, that is not permitted to short-circuit the outputs. Internal circuitry is added in order to increase the accuracy of the motor current particularly with low current levels.

## 6.6 $V_s$ , $V_{cc}$ , $V_{ref}$

The circuit will stand any order of turn-on or turn-off of the supply voltages  $V_s$  and  $V_{cc}$ . Normal  $dV/dt$  values are then assumed.

Preferably,  $V_{ref}$  should be tracking  $V_{cc}$  during power-on and power-off if  $V_s$  is established.

**Figure 3.  $T_{on}$  and  $T_{off}$**

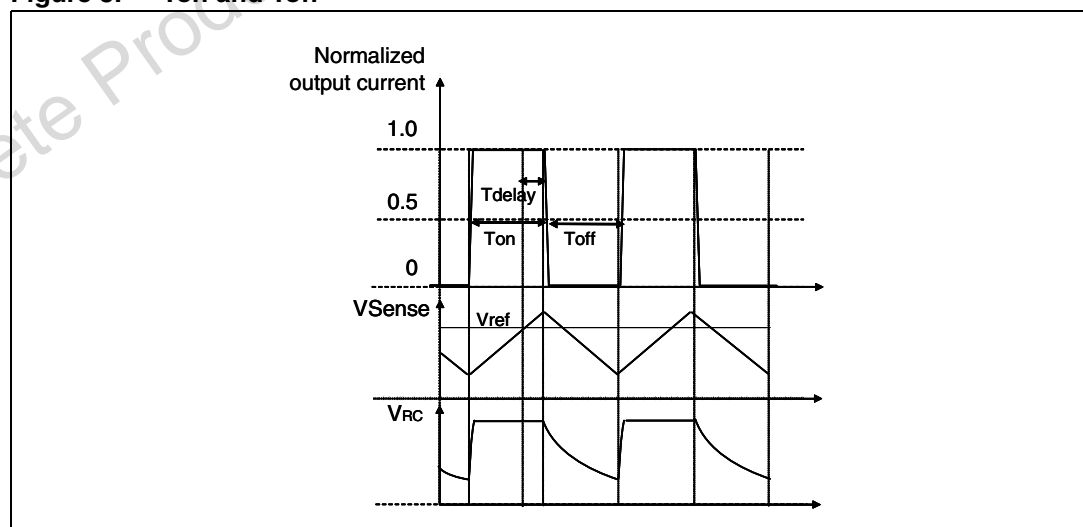




Figure 4. Half and Full Step Drive with  $I_{max}=1.2A$

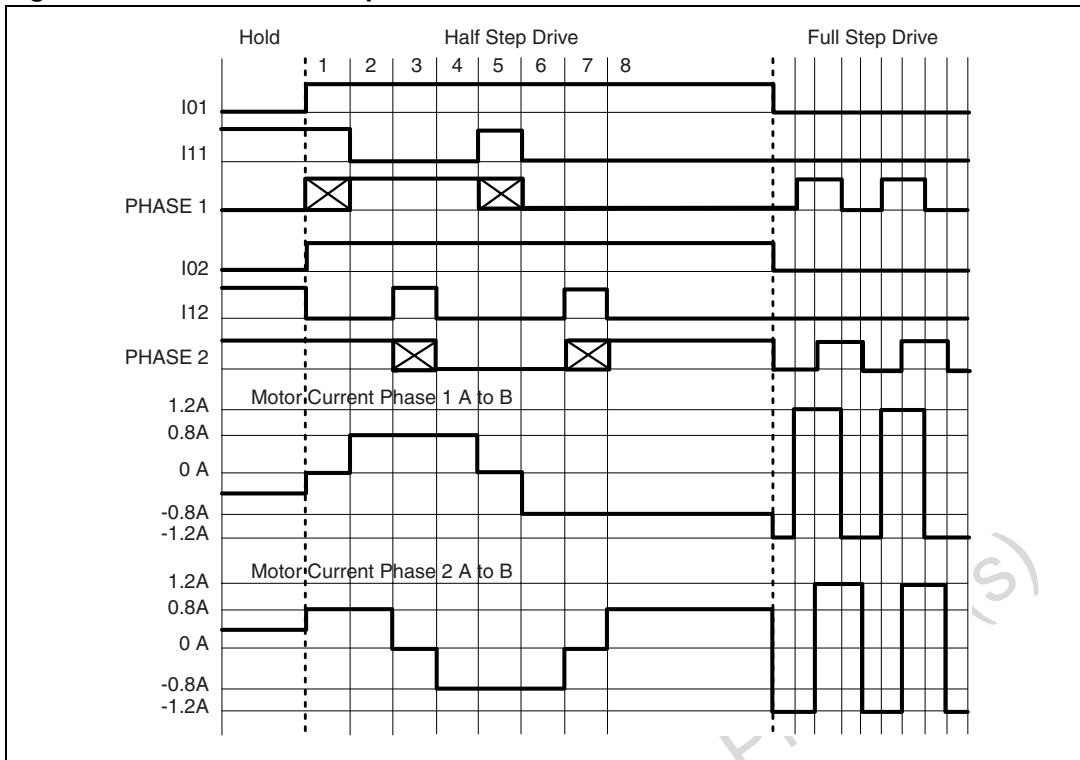
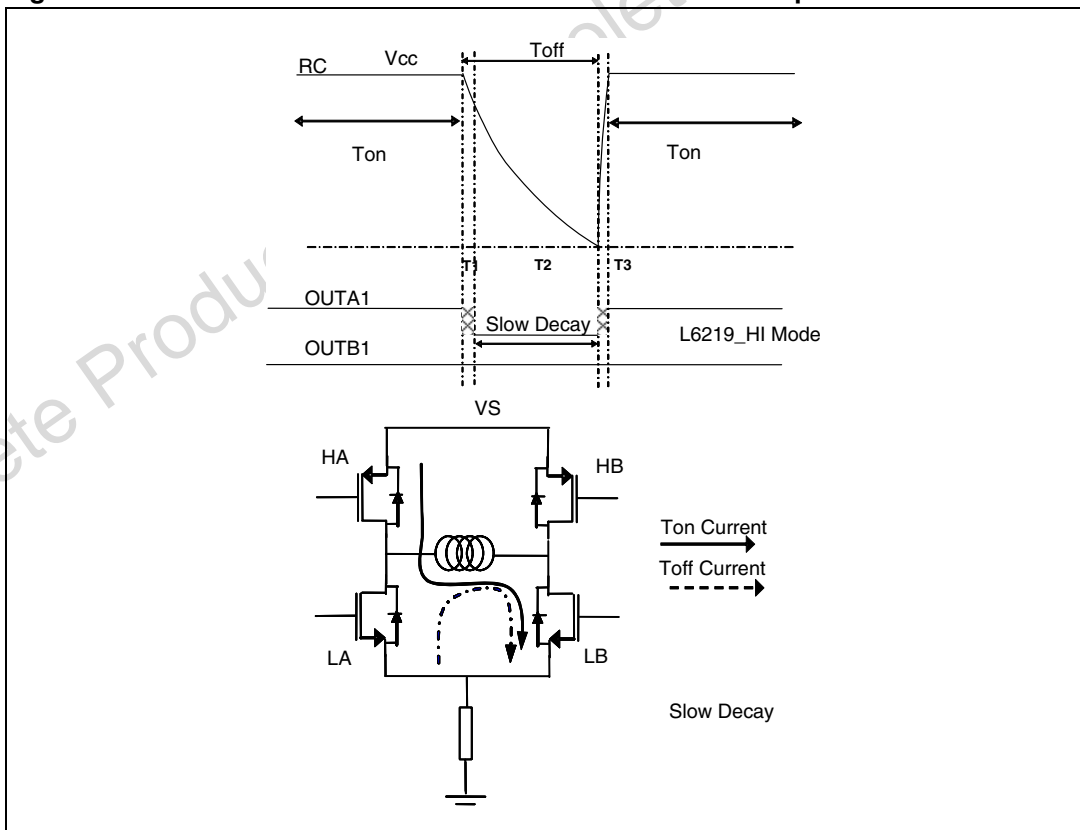


Figure 5. Normal conduction and slow recirculation current paths.



## 7 L6219\_8 mode

A second configuration of the device is achieved when PROG1 and PROG2 pins (pin 7 and 18) are asserted to 01. The device is now configured into the L6219\_8 configuration. This device mode function is similar to L6219\_HI, but with the possibility of using 8 current levels instead of 4, to implement a more accurate microstepping function and with the possibility to set a mixed decay for recirculation current. The remaining functionalities are identical to L6219\_HI mode.

### 7.1 8 Level Current Setting

This setting is achieved by using pin 8 (STB) as a strobe for latching the current setting control inputs. The rising edge of STB will latch the I01, I11 and I12 inputs for decoding current levels settings for Bridge 1. Similarly the falling edge will latch the I01, I11 and I12 inputs for decoding current levels settings for Bridge 2.

In order to allow a good similitude to sine drive, the levels set by the input pins are not equally spaced but are chosen to approximate a sinusoidal wave.

On power up, the device is by default into a no current drive state for both H Bridges and will start driving only upon the rising or falling edges of STB.

### 7.2 Mixed Decay

VREFCOM input (pin 15) is the reference voltage for both bridges while VREFDEC input (pin 11) is a voltage reference for decay control. When the current setting is set from an higher level to a lower level, the device can be set to perform:

1. Slow decay (current is recirculated through the low side drivers) when  $VREFDEC > 0.94V_{cc}$ .
2. A mix of Fast followed by Slow decay when  $0.33V_{cc} < VREFDEC < 0.94V_{cc}$ .
3. Fast decay (current is recirculated from Sense to Vs) when  $VREFDEC < 0.33V_{cc}$ .

In case 2, VREFDEC voltage is compared with the RC discharging voltage during the Toff duration. Until the RC voltage is above VREFDEC there will be fast decay: the bridge outputs will be driven to enable recirculation from Rsense to VS. For RC voltages below VREFDEC, the bridges will be driven to recirculate through the low side drivers. (see [Figure 8](#))

**Table 12. Current levels**

STB	I01	I11	I12	Current level	
$\downarrow$				Bridge1	Bridge 2
$\downarrow$	0	0	0	No current	-
$\downarrow$	0	0	1	$I_{OUT} / I_{max}=0.22$	-
$\downarrow$	0	1	0	$I_{OUT} / I_{max}=0.42$	-
$\downarrow$	0	1	1	$I_{OUT} / I_{max}=0.61$	-
$\downarrow$	1	0	0	$I_{OUT} / I_{max}=0.77$	-
$\downarrow$	1	0	1	$I_{OUT} / I_{max}=0.87$	-

**Table 12. Current levels (continued)**

STB	I01	I11	I12	Current level	
$\overline{\text{STB}}$	1	1	0	$I_{\text{OUT}} / I_{\text{max}}=0.93$	-
$\overline{\text{STB}}$	1	1	1	$I_{\text{OUT}} / I_{\text{max}}=1$	-
$\overline{\text{STB}}$	0	0	0	-	$I_{\text{OUT}} / I_{\text{max}}=1$
$\overline{\text{STB}}$	0	0	1	-	$I_{\text{OUT}} / I_{\text{max}}=0.93$
$\overline{\text{STB}}$	0	1	0	-	$I_{\text{OUT}} / I_{\text{max}}=0.87$
$\overline{\text{STB}}$	0	1	1	-	$I_{\text{OUT}} / I_{\text{max}}=0.77$
$\overline{\text{STB}}$	1	0	0	-	$I_{\text{OUT}} / I_{\text{max}}=0.61$
$\overline{\text{STB}}$	1	0	1	-	$I_{\text{OUT}} / I_{\text{max}}=0.42$
$\overline{\text{STB}}$	1	1	0	-	$I_{\text{OUT}} / I_{\text{max}}=0.22$
$\overline{\text{STB}}$	1	1	1	-	No current

**Table 13. AC/Transient Specification**

Symbol	Description	Min	Typ	Max
MD_h	Mixed decay trip point high		$0.93V_{\text{cc}} \pm 75\text{mV}$	
MD_l	Mixed decay trip point low		$0.33V_{\text{cc}} \pm 50\text{mV}$	

**Table 14. Timing specifications**

( $0^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$ ,  $V_S = 32\text{ V}$ , unless otherwise specified)

Name	Description	MIN	TYP	MAX	Units
Fstb	Strobe frequency			6	MHz
Thstb	Strobe high width	20			ns
Tlstb	Strobe low width	20			ns
Trd_stb	STB rise time	0		10	ns
Tfd_stb	STB fall time	0		10	ns
Trd_lxx	I01,I11,I12 rise time	0		10	ns
Tfd_lxx	I01,I11,I12 fall time	0		10	ns
Tsu_lxx	I01,I11,I12 setup time	15			ns
Thd_lxx	I01,I11,I12 hold time	15			ns

Figure 6. L6219\_8 mode Stepping Driving

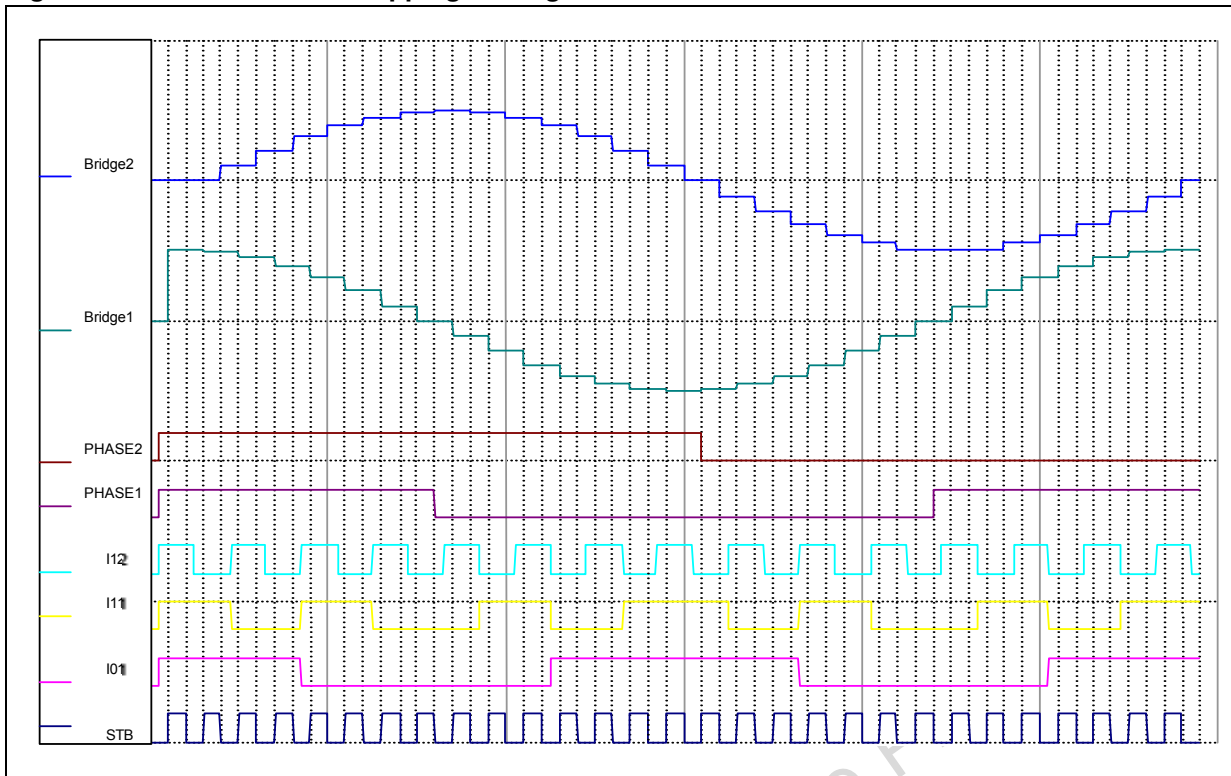
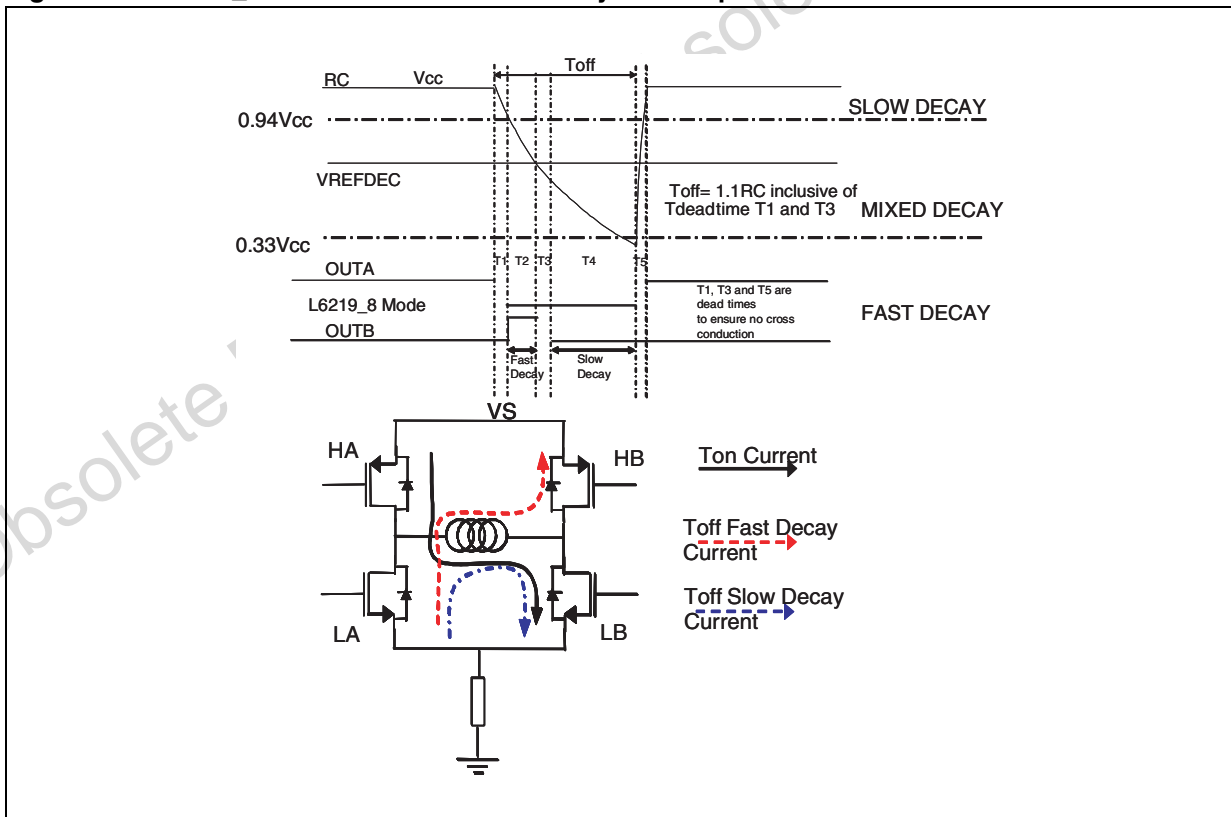


Figure 7. L6219\_8 mode Fast and Slow Decay current paths



## 8 L8229\_0 and L8229\_1 modes

When in these modes, the device can be programmed via a serial interface. This allows a very precise microstepping functionality as well as the control of several parameters related to the motor functionality.

In this configuration there is also the possibility of driving two DC motors by means of two pulse width modulated (PWM) control signals.

The parameters that can be set are the following:

1. Current levels (32 values for each bridge).
2. Current direction.
3. Type of decay for stepping motor (Mix/Slow).
4. Vref input (Ext/Int)
5. Vref divider (:5/:10).
6. Blanking time (4 values).
7. Oscillator freq divider (4 values).
8. Off time (32 values).
9. Fast decay time (16 values).
10. Synchronous rectification (Active/Passive/LowSide/Off).
11. Choose of driving a Stepping or DC motor.
12. Possibility of paralleling bridges (in DC motor drive).
13. Slow or fast decay (in DC motor drive).
14. Possibility of setting outputs in brake mode.
15. Possibility of asserting Sleep mode to reduce current consumption and put outputs in HI-Z.

When in L8229 modes, pin 12 (FAULT) is used to provide a "Generic Fault" signal that is intended as a warning for the user. In case of:

- a) Undervoltage detection (UVD): no action is taken on output bridges and the device will be working, leaving to the user the action of stopping the output bridges functionality.  
During UVD event, the Generic Fault signal is pulled high.
- b) Thermal shutdown (TSD): output bridges will be in Hi-Z mode (all outputs off) until the temperature decreases below TSD threshold minus hysteresis.  
During TSD event, the Generic Fault signal is pulled high.
- c) Over current detection (OCD): output bridges will be in Hi-Z mode. Depending on the motor (Stepping or DC according to W2 bit 14), the OCD status will be latched as follows:
  - for stepping motor driving the OCD status will be latched until SPI is reset by means of nRESET pin.
  - for DC motor driving the OCD status will be latched until next positive PWM edge occurs.For both above cases, the Generic Fault signal is pulled high until the OCD status persists.

**Table 15. DC Specifications**  
( $0^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$ ,  $V_S = 32\text{ V}$ , unless otherwise specified)

Name	Description	Conditions	Min	Typ	Max	Units
Vref voltage	Internal reference voltage		1.94	2	2.06	V
$I_{\text{off-rev}}$	Reverse current detection offset (in Active Sync recirculation)			$\pm 50$		mA

**Table 16. AC/Transient Specifications**  
( $0^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$ ,  $V_S = 32\text{ V}$ , unless otherwise specified)

Name	Description	Conditions	Min	Typ	Max	Units
Osc	Oscillator frequency			4		MHz

## 8.1 Serial interface specification

This device, when in L8229\_0 or L8229\_1 configuration, is managed via a Serial Interface Port for a total of 16 bits with 4 different words. This port provides an interface between the chip and external digital ASIC. For the user this port is write-only: assigned read registers are for test mode purposes only.

The interface consists of 3 signal lines: chip select (nCS, active low), serial clock (SCLK) and serial data input (SDI).

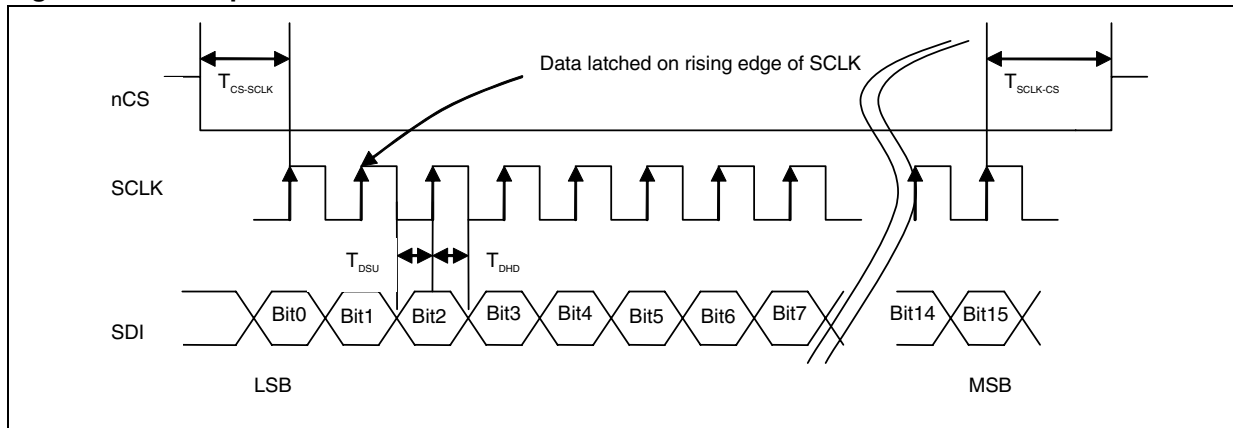
The digital ASIC initiates a serial transfer by pulling low the chip select line, nCS. Then it generates 16 clock pulses on SCLK while presenting the serial data on input SDI. The data is shifted into the L8229 on the rising edge of SCLK. The digital ASIC presents the data on SDI one setup time ( $T_{\text{dsu}}$ ) before the rising edge of SCLK. The data is held constant for the data hold time ( $T_{\text{dhd}}$ ) beyond the SCLK rising edge. The less significant bit, or LSB, is the first to be shifted out of the digital ASIC and into the chip, followed by the remaining bits. The last of the 16 bits is the most significant bit or MSB. SDI will remain at the value presented with the last bit of data. The nCS line is then returned to a high state. The low to high transition of nCS loads the data into the internal L8229 input register where all the inputs are presented to their appropriate functions in a parallel mode.

In the event that there are less or more than 16 SCLK rising edges during nCS=0, the device will interpret the packet as invalid. This enables the SPI bus to be shared with others devices with similar packet skipping functionality (and with programming word length different from 16 bits), without the use of nCS.

The outputs of the serial input port shall not "glitch" during any operation.

The serial interface is cleared by nRESET signal applied to pin 14. When nRESET=0, output stages are in Hi-Z mode (all outputs off). Please note that neither TSD nor OCD reset the SPI.

Figure 8. SPI Operations



**Table 17. SPI Timing specifications**  
 ( $0^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$ ,  $V_S = 3.2\text{ V}$ , unless otherwise specified)

Name	Description	MIN	TYP	MAX	Units
Fclk	Serial clock frequency		8	12	MHz
Tclh	SCLK high width	30			ns
Tcll	SCLK low width	30			ns
Tcs-sclk	Delay nCS falling to first SCLK rising	10			ns
Tsclk-cs	Delay last SCLK rising edge to nCS rising	10			ns
Tdsu	Data valid to SCLK set up time	10			ns
Tdhd	Data hold time	10			ns
Tcs-cs	Delay required from (n-1)CS to nCS	10			ns
Trd	SDI rise time	0		20	ns
Tfd	SDI fall time	0		20	ns
Trfc	SCLK rise/fall time	0		20	ns

## 8.2 SPI Bit definition

### 8.2.1 Word Description

Each of the 3 words used to program the chip when in L8229\_0 or L8229\_1 mode has the 3 LSB used to address the word as follows:

**Table 18. Word Description**

BIT #	NAME	Value		DESCRIPTION
0	CHIP ADDRESS	0		This value addresses the word to chip #0 (if two L8229 are present on the same board and a single nCS line is used). Chip address is assigned by configuring the PROG bit according to <a href="#">Table 2</a> .
		1		This value addresses the word to chip #1 (if two L8229 are present on the same board and a single nCS line is used). Chip address is assigned by configuring the PROG bit according to <a href="#">Table 2</a> .
1 and 2	WORD ADDRESS 1, WORD ADDRESS 2	Bit 2	Bit 1	
		0	0	W0: OPERATIVE register
		0	1	W1: PARAMETERS register
		1	0	W2 : FUNCTIONAL register
		1	1	Not allowed

### 8.2.2 W0 (OPERATIVE: Bit 2=0, Bit 1=0)

This word is mainly used to fix the current level and direction in the bridge.

**Table 19. W0**

BIT #	NAME	RESET VALUE	DESCRIPTION
0	CHIP ADDRESS	0	This bit is used to select if the informations provided by bits 1 to 15 are referred to chip 0 or chip 1. This is useful in the case that two L8229 are present on the same board and a single nCS line is used.
1	WORD ADDRESS 1	0	This is the LSB of the two bits used to address the word
2	WORD ADDRESS 2	0	This is the MSB of the two bits used to address the word
3	DAC1 BIT 1 (LSB)	0	LSB for DAC intended to regulate the current of Bridge 1
4	DAC1 BIT 2	0	BIT2 for DAC intended to regulate the current of Bridge 1
5	DAC1 BIT 3	0	BIT3 for DAC intended to regulate the current of Bridge 1
6	DAC1 BIT 4	0	BIT4 for DAC intended to regulate the current of Bridge 1
7	DAC1 BIT 5 (MSB)	0	MSB for DAC intended to regulate the current of Bridge 1
8	PHASE 1	0	Controls the direction of current flow for Bridge1. A logic 0 level causes current flow from A (source) to B (sink).
9	DAC2 BIT1 (LSB)	0	LSB for DAC intended to regulate the current of Bridge 2



Table 19. W0 (continued)

BIT #	NAME	RESET VALUE	DESCRIPTION
10	DAC2 BIT 2	0	BIT2 for DAC intended to regulate the current of Bridge 2
11	DAC2 BIT 3	0	BIT3 for DAC intended to regulate the current of Bridge 2
12	DAC2 BIT 4	0	BIT4 for DAC intended to regulate the current of Bridge 2
13	DAC2 BIT 5 (MSB)	0	MSB for DAC intended to regulate the current of Bridge 2
14	PHASE 2	0	Controls the direction of current flow Bridge 2. A logic HIGH level causes current flow from A (source) to B (sink).
15	PARALLEL OUTPUT	0	This bit must be set to 1 when outputs are paralalled to drive a single DC motor

### 8.3 W1 (PARAMETERS: Bit 2=0, Bit 1=1)

This word is mainly used to set motor related parameters.

Table 20. W1

BIT #	NAME	RESET VALUE	DESCRIPTION
0	CHIP ADDRESS	0	This bit is used to select if the informations provided by bits 1 to 15 are referred to chip 0 or chip 1. This is useful in the case that two L8229 are present on the same board and a single nCS line is used.
1	WORD ADDRESS 1	0	This is the LSB of the two bits used to address the word.
2	WORD ADDRESS 2	0	This is the MSB of the two bits used to address the word.
3	NSLEEP	0	This bit is used to decide if the device should exit sleep mode.
4	OFF1	0	LSB for fixing the Toff time (see following <a href="#">Table 32</a> ).
5	OFF2	0	BIT 2 for fixing the Toff time (see following <a href="#">Table 32</a> ).
6	OFF3	0	BIT 3 for fixing the Toff time (see following <a href="#">Table 32</a> ).
7	OFF4	0	BIT 4 for fixing the Toff time (see following <a href="#">Table 32</a> ).
8	OFF5	0	MSB for fixing the Toff time (see following <a href="#">Table 32</a> ).
9	FASTDEC1	0	LSB for fixing the Fast Decay time (see following <a href="#">Table 31</a> ).
10	FASTDEC2	0	BIT 2 for fixing the Fast Decay time (see following <a href="#">Table 31</a> ).
11	FASTDEC3	0	BIT 3 for fixing the Fast Decay time (see following <a href="#">Table 31</a> ).
12	FASTDEC4	0	MSB for fixing the Fast Decay time (see following <a href="#">Table 31</a> ).
13	SYNCRECT1	0	LSB to decide the rectification mode (see following <a href="#">Table 35</a> ).
14	SYNCRECT2	0	MSB to decide the rectification mode (see following <a href="#">Table 35</a> ).
15	Brake	0	This bit is used to put outputs in brake mode

## 8.4 W2 (FUNCTIONAL: Bit 2=1, Bit 1=0)

This word is mainly used to set the functional mode

Table 21. W2

BIT #	NAME	RESET VALUE	DESCRIPTION
0	CHIP ADDRESS	0	This bit is used to select if the informations provided by bits 1 to 15 are referred to chip 0 or chip 1. This is useful in the case that two L8229 are present on the same board and a single nCS line is used.
1	WORD ADDRESS 1	0	This is the LSB of the two bits used to address the word.
2	WORD ADDRESS 2	0	This is the MSB of the two bits used to address the word.
3	MIX/SLOW 1 (St. mot)	0	This bit is to decide if Slow or Mixed Decay is applied to Bridge 1 (Stepping motor).
4	MIX/SLOW 2 (St. mot)	0	This bit is to decide if Slow or Mixed Decay is applied to Bridge 2 (Stepping motor).
5	REFERENCE INT/EXT	0	This bit is used to decide if the reference voltage will be internal (0) or external (1)
6	RANGE	0	This bit is to decide if the reference voltage will be divided by 10 (0) or by 5 (1).
7	BLANK LSB	0	This is the LSB bit used to fix the Blanking time (see following <a href="#">Table 30</a> ).
8	BLANK MSB	0	This is the MSB bit used to fix the Blanking time (see following <a href="#">Table 30</a> ).
9	OSC LSB	0	This is the LSB bit used to fix the Oscillator values (see following <a href="#">Table 29</a> ).
10	OSC MSB	0	This is the MSB bit used to fix the Oscillator values (see following <a href="#">Table 29</a> ).
11	TEST 1	0	This bit is used for trim mode.
12	TEST 2	0	This bit is used for trim mode.
13	TEST 3	0	This bit is used for trim mode.
14	STEP/DC	0	This bit is used to set the drive of a Stepping Motor (0) or a DC Motor (1).
15	SLOW/FAST (DC mot)	0	This bit is used to decide if Slow (0) or Fast (1) decay is applied to DC Motor configuration

### 8.4.1 Reading back SPI.

When W2 bit 11 to 13 are to 111, read back from SPI is enabled. This function is to check the actual data in W0 and W1; W2 can't be read back.

To read back the following procedure is requested:

1. Set PROG1=1, PROG2=0
2. Write W0 and W1 to SDI
3. Write W2 (with bits 11, 12, 13 set to 111) to SDI. This enables read back mode from SPI.
4. Write 0001 1111 1111 1111 to SDI (the first three bits mean that W0 is requested to be read out, the other bits have no sense just to fill the blank bits). This allows to check if the SDI output is W0 bit3~15.
5. Write W2 (with bits 11, 12, 13 set to 111) to SDI. This enables read back mode from SPI.
6. Write 0101 1111 1111 1111 to SDI (the first three bits mean that W1 is requested to be read out, the other bits have no sense just to fill the blank bits). This allows to check if the SDI output is W1 bit3~15.

If the data to be read out are the same as the data write in, it means write function of SPI is right.

## 9 SPI programming

On power up, the device is by default in sleep mode. Before coming out from sleep, the device needs to be programmed to drive either Stepping or DC motor. This is controlled by W2 bit 14. Default is stepping motor drive.

**Table 22. Motor mode selected by W2**

Bit 14	Mode
0	Stepping motor
1	DC motor

The device can be awoken from the sleep mode by means of the bit 3 of W1.

**Table 23. Nsleep mode selected by W1**

Bit 3	Mode
0	Sleep
1	Normal

The device can be set in brake mode ( both outputs are LL) by means of W1 bit 15. Please note that Brake mode overcomes Nsleep mode.

**Table 24. Brake mode selected by W1**

Bit 15	Mode
0	Normal
1	Brake

### 9.1 Current Control

Current level in the motor is set by means of a combination of Vref (ext or int), Rsense and DAC control bits.

The max current is set as follows:

$$I_{max} = V_{ref} / (Range \times R_{sense})$$

Vref can be set to be internal at 2V or externally applied to VREF1 and VREF2 pins. On power up, the default is the internal 2V.

**Table 25. Vref mode selected by W2**

Bit 5	Mode
0	Internal ref. 2V
1	External ref. (7.5V max)

Vref voltage is divided according to Range value that is defined by W2 bit 6 to be either 10 or 5.

**Table 26. Range mode selected by W2**

Bit 6	Mode
0	Range = 10
1	Range = 5

The direction of current is determined by W0 bits 8 and 14. During Ton, outputs will be according to following table:

**Table 27. Current direction selected by W0**

Bit 8 (14)	OUT A	OUT B
0	L	H
1	H	L

The 5 bit DACs for each Bridge enable an accurate resolution control defined by Current levels table below. The current level Iset is then defined as:

$$I_{set} = V_{dac} / (\text{Range} \times R_{sense})$$

where:

$$V_{dac} = (\text{DAC}/31) \times V_{ref}$$

where DAC is defined from 0 to 31, so the current level is fixed by W0 bits 7 (MSB) to 3 (LSB) (13 to 9) as in following table.

**Table 28. Current levels selected by W0 for DAC**

Bit 7 (13)	Bit 6 (12)	Bit 5 (11)	Bit 4 (10)	Bit 3 (9)	IPH_A (B)/I <sub>max</sub>
0	0	0	0	0	0
0	0	0	0	1	1/31
0	0	0	1	0	2/31
0	0	0	1	1	3/31
0	0	1	0	0	4/31
0	0	1	0	1	5/31
0	0	1	1	0	6/31
0	0	1	1	1	7/31
0	1	0	0	0	8/31
0	1	0	0	1	9/31
0	1	0	1	0	10/31
0	1	0	1	1	11/31
0	1	1	0	0	12/31
0	1	1	0	1	13/31
0	1	1	1	0	14/31
0	1	1	1	1	15/31
1	0	0	0	0	16/31

**Table 28. Current levels selected by W0 for DAC (continued)**

Bit 7 (13)	Bit 6 (12)	Bit 5 (11)	Bit 4 (10)	Bit 3 (9)	IPH_A (B)/Imax
1	0	0	0	1	17/31
1	0	0	1	0	18/31
1	0	0	1	1	19/31
1	0	1	0	0	20/31
1	0	1	0	1	21/31
1	0	1	1	0	22/31
1	0	1	1	1	23/31
1	1	0	0	0	24/31
1	1	0	0	1	25/31
1	1	0	1	0	26/31
1	1	0	1	1	27/31
1	1	1	0	0	28/31
1	1	1	0	1	29/31
1	1	1	1	0	30/31
1	1	1	1	1	31/31

## 9.2 Timings Control

All timings are controlled by a master oscillator that can be internal or externally provided. At power up, OSC will default to the internal 4MHz oscillator. Setting W2 bits 9 and 10 will select the external oscillator frequency or it's dividing by either 2 or 4.

**Table 29. Oscillator frequency selected by W2**

Bit 10	Bit 9	Freq
0	0	Internal (4MHz)
0	1	Ext
1	0	Ext/2
1	1	Ext/4

The switching blanking time for masking transient can be selected by W2 bits 7 and 8.

**Table 30. Blanking time selected by W2**

Bit 8	Bit 7	Time
0	0	2/fosc
0	1	4/fosc
1	0	8/fosc
1	1	12/fosc

Fast decay timing is set by W1 bits 9 (LSB) to 12 (MSB).

$$T_{fast} = (N+1) \times 8/Fosc$$

Where N = 0 to 15 and Fosc is either the internal 4 MHz or the external oscillator frequency with selected division.

Setting Toff to be smaller than Tfast will result in fast decay only.

**Table 31. Fast decay time selected by W1**

Bit 12	Bit 11	Bit10	Bit9	Fast decay
0	0	0	0	1x8/fosc
0	0	0	1	2x8/fosc
0	0	1	0	3x8/fosc
0	0	1	1	4x8/fosc
0	1	0	0	5x8/fosc
0	1	0	1	6x8/fosc
0	1	1	0	7x8/fosc
0	1	1	1	8x8/fosc
1	0	0	0	9x8/fosc
1	0	0	1	10x8/fosc
1	0	1	0	11x8/fosc
1	0	1	1	12x8/fosc
1	1	0	0	13x8/fosc
1	1	0	1	14x8/fosc
1	1	1	0	15x8/fosc
1	1	1	1	16x8/fosc

The Toff timing is controlled by bits 4 (LSB) to 8 (MSB) of W1 and is based on the oscillator frequency.

$$T_{off} = (N+1) \times 8/Fosc$$

Where N = 0 to 31 and Fosc is either the internal 4 MHz or the external oscillator frequency with selected division.

**Table 32. Toff time selected by W1**

Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Toff
0	0	0	0	0	1x8/fosc
0	0	0	0	1	2x8/fosc
0	0	0	1	0	3x8/fosc
0	0	0	1	1	4x8/fosc
0	0	1	0	0	5x8/fosc
0	0	1	0	1	6x8/fosc

Table 32. Toff time selected by W1 (continued)

Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Toff
0	0	1	1	0	7x8/fosc
0	0	1	1	1	8x8/fosc
0	1	0	0	0	9x8/fosc
0	1	0	0	1	10x8/fosc
0	1	0	1	0	11x8/fosc
0	1	0	1	1	12x8/fosc
0	1	1	0	0	13x8/fosc
0	1	1	0	1	14x8/fosc
0	1	1	1	0	15x8/fosc
0	1	1	1	1	16x8/fosc
1	0	0	0	0	17x8/fosc
1	0	0	0	1	18x8/fosc
1	0	0	1	0	19x8/fosc
1	0	0	1	1	20x8/fosc
1	0	1	0	0	21x8/fosc
1	0	1	0	1	22x8/fosc
1	0	1	1	0	23x8/fosc
1	0	1	1	1	24x8/fosc
1	1	0	0	0	25x8/fosc
1	1	0	0	1	26x8/fosc
1	1	0	1	0	27x8/fosc
1	1	0	1	1	28x8/fosc
1	1	1	0	0	29x8/fosc
1	1	1	0	1	30x8/fosc
1	1	1	1	0	31x8/fosc
1	1	1	1	1	32x8/fosc



### 9.3 Decay Modes and Synchronous Rectification

For stepping motor drive, the recirculation mode during Toff could be slow, fast or mixed (that is fast followed by slow decay): W2, by means of bit 3 (for Out1) and bit 4 (for Out2), allows to select MIXED or SLOW decay for bridge 1 and bridge 2 respectively; by selecting (with W1, bits 9 to 12) Tfast longer than Toff, it is possible to select FAST decay for all the Toff duration.

**Table 33. Stepping decay mode selected by W2**

Bit 3 (4)	Mode
0	Mixed decay
1	Slow decay

For DC motor drive, W2 bit 15 allows to choose slow or fast decay.

**Table 34. DC decay mode selected by W2**

Bit 15	Mode
0	Slow
1	Fast

During the decay, it is possible for the current to flow through the intrinsic body diodes of the LDMOS or through switched on LDMOS channel (in this case the current conduction will be reversed from Source to Drain). This switching on of the active device in parallel with the diode is called SYNCHRONOUS rectification and means that the recirculation path is not obtained only through the internal diodes but also by turning on the DMOS in parallel with the diode needed to recirculate current; because of the low RDSon of this LDMOS the dissipation is reduced.

For stepping motors only with W1, by means of bits 13 and 14, it is possible to choose several kinds of SYNCHRONOUS recirculation modes: ACTIVE recirculation, PASSIVE recirculation, SYNC OFF recirculation, and LOW SIDE recirculation.

**Table 35. Sync rectification selected by W1**

Bit 14	Bit 13	Mode
0	0	Active <sup>(1)</sup>
0	1	Passive
1	0	Off
1	1	Low side

1. Only for Mixed Decay mode.

ACTIVE means that the current is monitored to avoid reverse current in the load: this could happen because of FAST SYNC recirculation (that reverse the conduction of the bridge). When a reverse current is detected, synchronous rectification is turned off, so the outputs are placed in Hi-Z state until the end of Toff. Please note that Active Synchronous rectification can't be used when in Slow Decay mode.

PASSIVE means that the current is not monitored to avoid a reverse current in the load. In this case the current, during Toff, could be inverted and no action is taken until the current reaches the current limit selected by the user by means of Vref and Rsense. When this

value is reached, synchronous rectification is turned off, so the outputs are placed in Hi-Z state until the end of Toff. Please note that a typical 50mA reverse current could be present during Active Sync rectification.

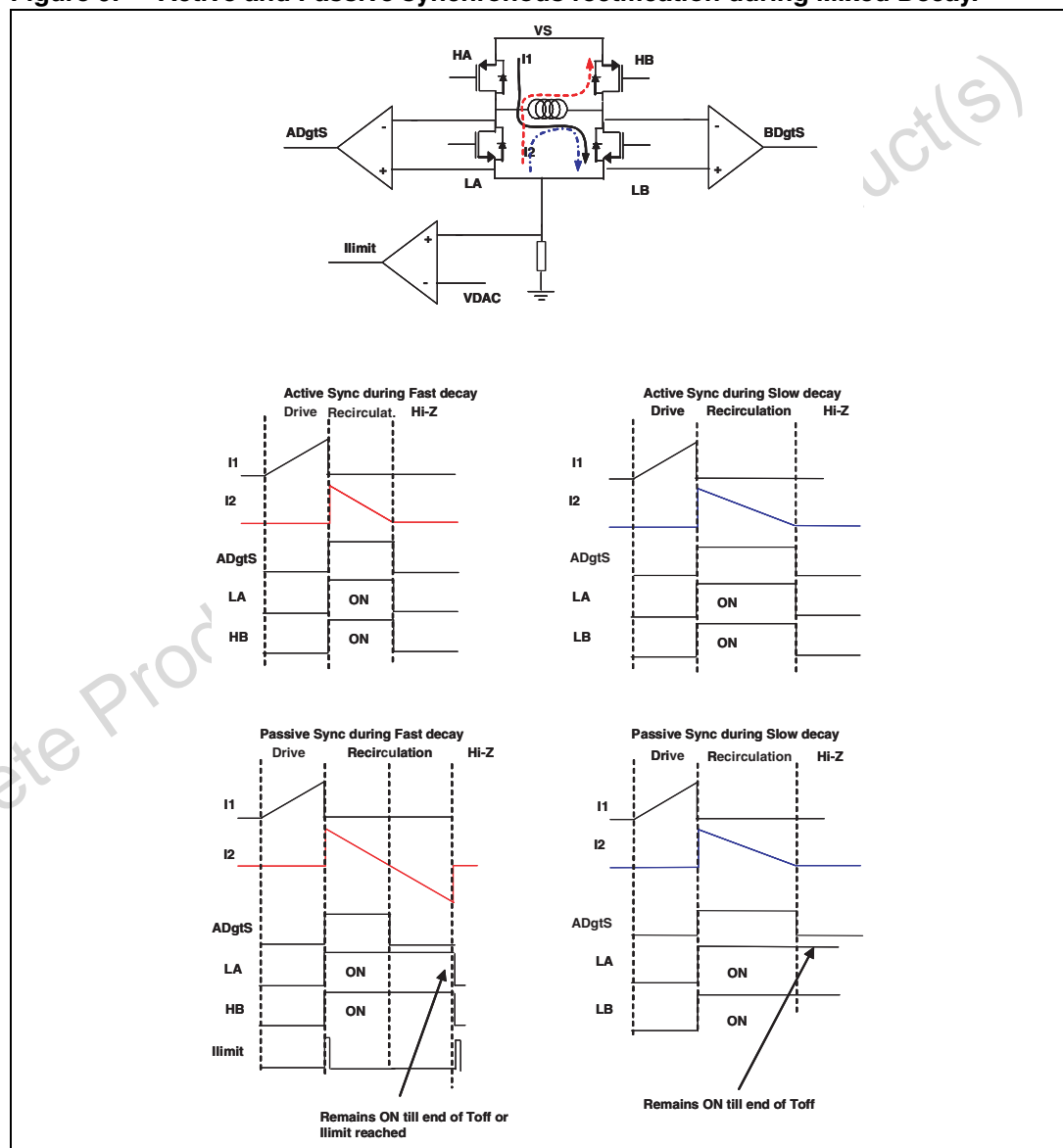
SYNC OFF means that the current will recirculate through the body diodes in parallel with power DMOS. This is intended to allow the user to use external Schottky diodes to save the internal dissipation.

LOW SIDE means that the synchronous recirculation is forced only through the low side power DMOS.

Please note that while the current reversal is always sensed, if required, the current level is sensed only by means of Rsense, so no current control is performed when current flows away from Rsense, as in SLOW recirculation.

Active and passive synchronous rectification modes are illustrated in the following drawing:

**Figure 9. Active and Passive synchronous rectification during Mixed Decay.**



The output states during these cases of recirculation could be summarized as below: (only OUTA to OUTB current flowing is described)

## 9.4 Mixed Decay

### 1) ACTIVE SYNC recirculation could be divided in following cases.

#### 1a) No reverse current detected during Toff

HA on	HB off	LA off	LB on	Current increasing in the load.
All off				Anticross state (fast recirculation through LA and HB body diodes).
HA off	HB on	LA on	LB off	FAST SYNC recirculation through DMOS till end of fast decay time.
HA off	HB off	LA on	LB off	Anticross state (fast recirculation through LA DMOS and HB body diode).
HA off	HB off	LA on	LB on	SLOW SYNC recirculation till end of Toff.
HA off	HB off	LA off	LB on	Anticross state (slow recirculation through LA body diode and LB DMOS).
HA on	HB off	LA off	LB on	Current increasing in the load.

#### 1b) Reverse current detected during Fast Recirculation of Toff

HA on	HB off	LA off	LB on	Current increasing in the load.
All off				Anticross state (fast recirculation through LA and HB body diodes).
HA off	HB on	LA on	LB off	FAST SYNC recirculation through DMOS till reverse current is detected.
All off				Hi-Z state till end of Toff.
HA on	HB off	LA off	LB on	Current increasing in the load.

#### 1c) Reverse current detected during Slow Recirculation of Toff

HA on	HB off	LA off	LB on	Current increasing in the load.
All off				Anticross state (fast recirculation through LA and HB body diodes).
HA off	HB on	LA on	LB off	FAST SYNC recirculation through DMOS till end of fast decay time.
HA off	HB off	LA on	LB off	Anticross state (fast recirculation through LA DMOS and HB body diode).
HA off	HB off	LA on	LB on	SLOW SYNC recirculation till reverse current is detected.
All off				Hi-Z state till end of Toff.
HA on	HB off	LA off	LB on	Current increasing in the load.

**2) - PASSIVE SYNC recirculation could be divided in following cases:**

**2a) The reverse current (if present) does not exceed the regulated value  
(Note: this case is identical to ACTIVE SYNC case 1a)**

HA on	HB off	LA off	LB on	Current increasing in the load.
All off				Anticross state (fast recirculation through LA and HB body diodes).
HA off	HB on	LA on	LB off	FAST SYNC recirculation through DMOS till end of fast decay time.
HA off	HB off	LA on	LB off	Anticross state (fast recirculation through LA DMOS and HB body diode).
HA off	HB off	LA on	LB on	SLOW SYNC recirculation till end of Toff.
HA off	HB off	LA off	LB on	Anticross state (slow recirculation through LA body diode and LB DMOS).
HA on	HB off	LA off	LB on	Current increasing in the load.

**2b) The reverse current exceeds the regulated value during FAST recirculation.  
(Note: if the current exceed the regulated value during SLOW recirculation, no action is taken and the behaviour will be that of case 2a)**

HA on	HB off	LA off	LB on	Current increasing in the load.
All off				Anticross state (fast recirculation through LA and HB body diodes).
HA off	HB on	LA on	LB off	FAST SYNC recirculation through DMOS till reverse current reaches the regulated value).
All off				Hi-Z state till end of Toff.
HA on	HB off	LA off	LB on	Current increasing in the load.

**3) - SYNC OFF recirculation has only one case:**

HA on	HB off	LA off	LB on	Current increasing in the load.
All off				Fast recirculation through LA and HB body diodes till end of fast decay time.
HA off	HB off	LA off	LB on	Slow recirculation through LA body diode and LB DMOS till end of Toff.
HA on	HB off	LA off	LB on	Current increasing in the load.

#### 4) LOW SIDE recirculation has only one case:

HA on	HB off	LA off	LB on	Current increasing in the load.
All off				Fast recirculation through LA and HB body diodes) till end of fast decay time.
HA off	HB off	LA on	LB on	SLOW SYNC recirculation till end of Toff.
HA off	HB off	LA off	LB on	Anticross state (slow recirculation through the LA body diode and LB DMOS).
HA on	HB off	LA off	LB on	Current increasing in the load.

## 9.5 Slow Decay

When in Slow Decay, Active Synchronous rectification can't be used since current is not expected to be reversed because of BEMF. Therefore only Passive, Off or Low side recirculation cases can be selected.

### 1) ACTIVE SYNC recirculation is not allowed.

### 2) PASSIVE SYNC recirculation

HA on	HB off	LA off	LB on	Current increasing in the load.
HA off	HB off	LA off	LB on	Anticross state (slow recirculation through LA body diode and LB DMOS).
HA off	HB off	LA on	LB on	SLOW SYNC recirculation till end of Toff.
HA off	HB off	LA off	LB on	Anticross state (slow recirculation through the LA body diode and LB DMOS).
HA on	HB off	LA off	LB on	Current increasing in the load.

### 3) SYNC OFF

HA on	HB off	LA off	LB on	Current increasing in the load.
HA off	HB off	LA off	LB on	Slow recirculation (through the LA body diode and LB DMOS) till end of Toff
HA on	HB off	LA off	LB on	Current increasing in the load.

### 4) LOW SIDE is identical to PASSIVE SYNC.

# 10 DC Motor Driver operation

When in L8229\_0 or L8229\_1 configuration, the device could be configured to drive two different DC motors. Each drive provides bi-directional drive to a DC motor via the serial control and the PWM pins. The W0 bits 8 and 14 in the register will control the direction of drive while the PWM input pin controls the switching of the drivers. According to above description, the motor drive will be in voltage mode only.

The device could also drive a single DC motor with increased current by paralleling the two bridges. If this is required, W0 bit 15 must be set to 1 and OUT1A must be shorted to OUT2A while OUT1B must be shorted to OUT2B. In this case of two bridges paralleled to drive a single DC motor, the W0 bit 14 (PHASE2) will not be used as well as pin 17 (PWM2). This means that the device will act as a single bridge with outputs OUTA (OUT1A in parallel with OUT2A), OUTB (OUT1B in parallel with OUT2B) and driven by PHASE1 (W0 bit 8) and PWM1 (pin 20).

The drives are powered by VS.

The crossover delay is controlled to provide sufficient time for cross-conduction suppression, so that at no time both the upper and lower output devices on the same side of the H bridge are allowed to conduct simultaneously.

A blanking period following a current turn-on event is included to prevent false current protection turnoffs due to the initial current spike resulting from circuit capacitance.

When OCD happens, outputs are placed in Hi\_Z until next PWM positive edge occurs.

During an over-temperature event, when the device junction temperature Tj is above Tj(shutdown), the internal thermal protection circuit disables the drive outputs by driving all outputs to the high impedance state until the device temperatures have dropped below the lower thermal threshold temperature.

**Table 36. DC Motor Drivers - DC Specifications**  
(0°C ≤ Tj ≤ 125°C, VS = 32 V, unless otherwise specified)

Name	Description	Conditions	Min	Typ	Max	Units
IDCMOTOR OCT	DC Motor Over Current Threshold (1)		1.5			A

1. The current limitation is applied to the bottom H bridge LDMOS only, therefore over current protection applies to motor current, but no short circuit protection exists against shorts from the DC motor outputs to ground or to VS.

**Table 37. DC Motor Drivers - AC/Transient Specifications**  
(0°C ≤ Tj ≤ 125°C, VS = 32 V, unless otherwise specified)

Name	Description	Conditions	Min	Typ	Max	Units
fPWM	PWM frequency		10		30	KHz
Tblank	Blanking time (for OCD)			1		µs

**Table 38. DC Motor Drivers Truth Table**

Therm. prot.	OCD	W2 bit 15 (SLOW /FAST)	W0 bit 8 or 14 (PHASE)	Pin 20 or 17 (PWM)	OUT A high side	OUT A low side	OUT B high side	OUT B low side	Out State
0	0	0	0	0	Off	On	Off	On	L-L
0	0	0	0	1	Off	On	On	Off	L-H

Table 38. DC Motor Drivers Truth Table (continued)

Therm. prot.	OCD	W2 bit 15 (SLOW /FAST)	W0 bit 8 or 14 (PHASE)	Pin 20 or 17 (PWM)	OUT A high side	OUT A low side	OUT B high side	OUT B low side	Out State
0	0	0	1	0	Off	On	Off	On	L-L
0	0	0	1	1	On	Off	Off	On	H-L
0	0	1	0	0	On	Off	Off	On	H-L
0	0	1	0	1	Off	On	On	Off	L-H
0	0	1	1	0	Off	On	On	Off	L-H
0	0	1	1	1	On	Off	Off	On	H-L
x	1	X	X	X	Off	Off	Off	Off	Hi. Z
1	x	X	X	X	Off	Off	Off	Off	Hi. Z

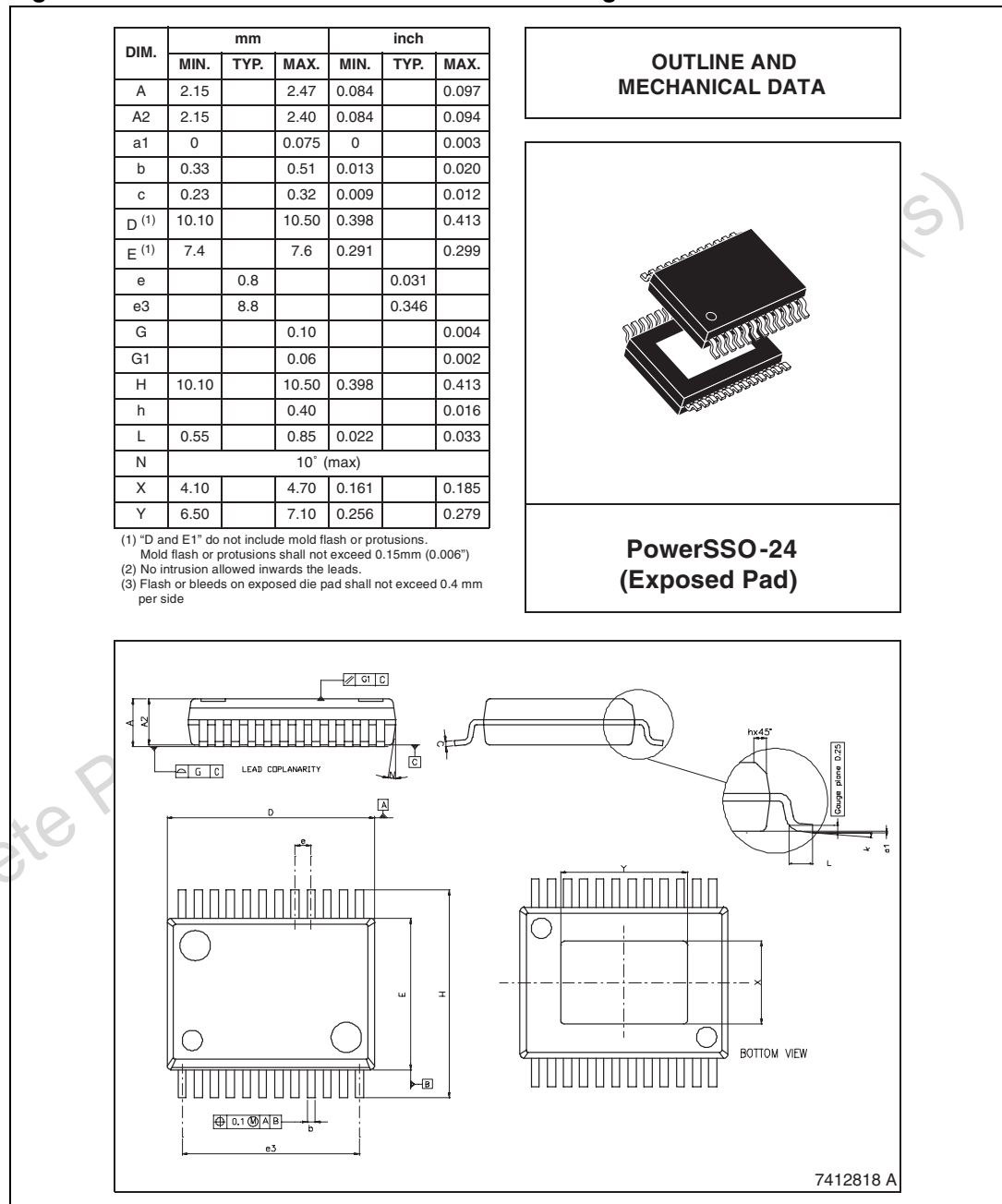
Obsolete Product(s) - Obsolete Product(s)

# 11 Package Information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

**Figure 10. PowerSSO24 Mechanical Data & Package Dimensions**





## 12 Revision history

**Table 39. Document revision history**

Date	Revision	Changes
17-Feb-2005	1	Initial release.
10-Aug-2005	2	Many modify of texts and table.
20-Feb- 2006	3	Corrected some errors/imprecisions in the whole document. Cancelled the L8229S part number, and all information about HSOP24 package.
30-May-2006	4	Added note at the table 2.
12-Sep- 2006	5	Applied new graphic design template. Modified the tables 2, 5, 6, 7, 8. 10, 13, 14, 15, 16, 17, 23 and 24.

Obsolete Product(s) - Obsolete Product(s)

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