Data Sheet
April 2000

microelectronics group

Lucent Technologies
Bell Labs Innovations

L8560 Low-Power SLIC with Ringing

Features

- Full-feature set for central office applications
- Also ideal for ISDN terminal adapters, pair gain, and cable telephony applications
- Auxiliary input for second battery, and internal switch to enable its use to save power in short telephone loops
- 5 V only operation or optional ±5 V operation for reduced power consumption
- Low active power (85 mW typical) and scan power (61 mW typical) with 5 V only operation
- Low active power (68 mW typical with auxiliary battery) and scan power (45 mW typical) with ±5 V operation
- Quiet tip/ring polarity reversal
- Per-line ringing available for short loops
- Reduced overhead and increased current limit during ring mode for lower-battery operation or increased ring loop length
- Supports meter pulse injection
- Distortion-free full duplex from 0 mA dc loop current on-hook transmission
- Convenient operating states:
  — Forward powerup
  — Polarity reversal powerup
  — Forward sleep
  — Ground start
  — Disconnect
- Adjustable supervision functions:
  — Off-hook detector with longitudinal rejection
  — Ground key detector with longitudinal rejection
  — Ring trip detector
- Independent, adjustable dc and ac parameters:
  — dc feed resistance (44-pin PLCC version)
  — Loop current limit
  — Termination impedance
- Thermal protection

Description

The L8560 full-feature, low-power subscriber line interface circuit (SLIC) is optimized for low power consumption while providing an extensive set of features. This part is ideal for ISDN terminal adapter applications and short-loop, power-sensitive applications such as pair gain and cable telephony. This part is also designed for PBX, DLC, or CO applications.

The SLIC includes an auxiliary battery input and a battery switch. In short-loop applications, SLICs can be used in high battery to present a high on-hook voltage, and then switched to low battery to reduce off-hook power.

To help minimize the required auxiliary battery voltage, the dc feed resistance and overhead voltage are set at 55 Ω and 6.7 V, respectively. This allows an undistorted on-hook transmission of a 3.14 dBm signal into a 900 Ω loop impedance.

The device offers the reverse battery function. Using the reverse battery, the device can provide a balanced power ring signal to tip and ring. In this mode of operation, the battery switch is used to apply a high-voltage battery during ringing and a lower-voltage battery during the talk and idle states. Also included in the L8560 is a dc current-limit switch, which increases the dc current limit during power ringing. In addition, dc overhead voltage is reduced during the ring state. With the battery and current-limit switches, and overhead reduction, the L8560 can provide sufficient power to ring a true North American 5 REN load of 1386 Ω + 40 µF.

The device offers ring trip and loop closure supervision with 0.3 V and 2 mA hysteresis, respectively. It also includes the ground start state and ring ground detection. A summing node for meter pulse injection to 2.2 Vrms is also included. The 44-pin PLCC version also has a spare uncommitted op amp, which may be used for ac gain setting or meter pulse filtering.

Table of Contents

Table of Contents (continued)

Figures

Tables

Description (continued)

The L8560 product family is graded by different features, specifications, and package options. The L8560Axx is the basic full-feature SLIC that operates with 5 V and a battery supply, and is available in the 32-pin PLCC (AAU) package and the 44-pin PLCC package (AP). This part is graded as the 54 dB longitudinal balance part. Additional features (spare op amp and overhead voltage programming) are available in the 44-pin PLCC package.

The L8560CAU is available only in the 32-pin PLCC package and has a feature set similar to the AAU version, except the CAU version requires +5 V, –5 V, and battery power supplies. With this option, power consumption is greatly reduced.

The L8560DAU and L8560EP are available in the 32-pin and 44-pin PLCC packages and have feature sets identical to the L8560AAU and L8560AP, respectively, with the following modifications. These parts are graded as high longitudinal balance (63 dB), and have an additional logic state (scan with low battery) which allows for low on-hook power dissipation.

The L8560FAU and L8560GP are available in the 32-pin and 44-pin PLCC packages and have feature sets identical to the L8560AAU and L8560AP, respectively, with the following modifications. These parts are graded for lower longitudinal balance (50 dB), and have an additional logic state (scan with battery) which allows for low on-hook power dissipation.

Table 1 below summarizes the features in the L8560 product family.

Table 1. L8560 Product Family Feature Summary

Feature	L8560						
	AAU	**AP**	**CAU**	**DAU**	**EP**	**FAU**	**GP**
32-Pin PLCC	X	NA	X	X	NA	X	NA
44-Pin PLCC	NA	X	NA	NA	X	NA	X
5 V Operation	X	X	NA	X	X	X	X
±5 V Operation (reduced power consumption)	NA	NA	X	NA	NA	NA	NA
Operational V_{BAT1} (V)	–70	–70	–70	–70	–70	–70	–70
Battery Switch	X	X	X	X	X	X	X
Balanced Ring Mode	X	X	X	X	X	X	X
Adjustable Overhead	NA	X	NA	NA	X	NA	X
Spare Op Amp	NA	X	NA	NA	X	NA	X
Reverse Battery	X	X	X	X	X	X	X
Scan Mode	X	X	X	X	X	X	X
Scan Mode with Low Battery	NA	NA	NA	X	X	X	X
Longitudinal Balance (dB)*	54	54	54	63	63	50	50
On-hook Transmission	X	X	X	X	X	X	X
Ground Start	X	X	X	X	X	X	X
Loop Start	X	X	X	X	X	X	X
Ring Trip Detector	X	X	X	X	X	X	X
Programmable Current Limit	X	X	X	X	X	X	X
Thermal Protection	X	X	X	X	X	X	X

* More information is provided in the Applications section of this document.

Description (continued)

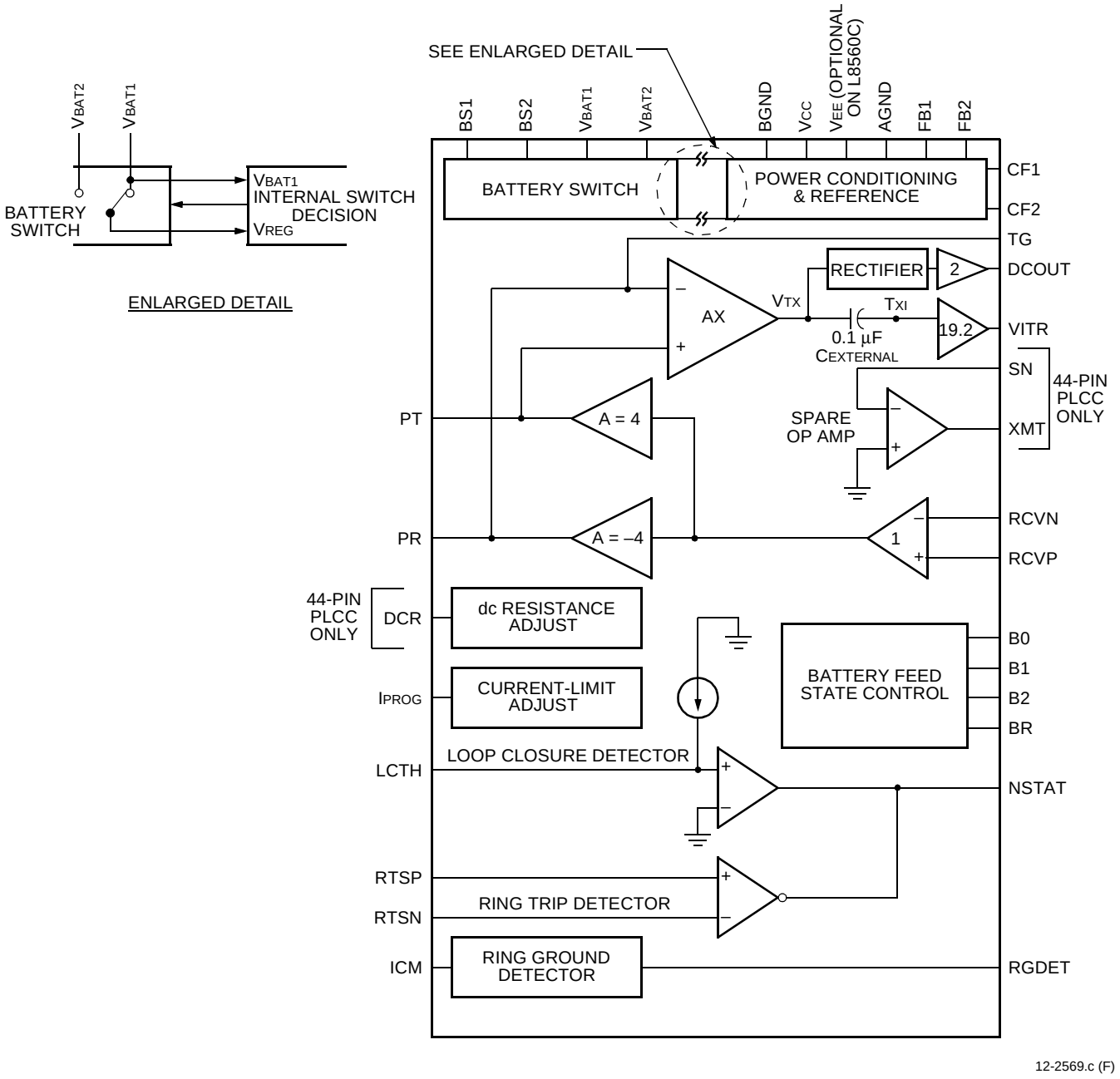
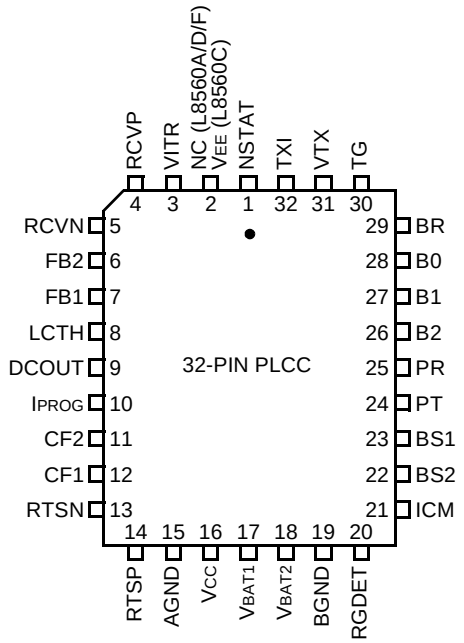


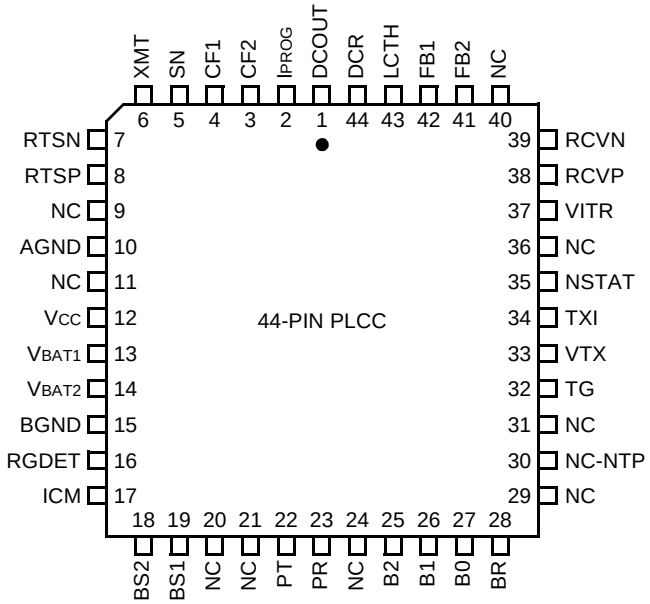
Figure 1. Functional Diagram

Pin Information



12-2548.L (F)

Figure 2. 32-Pin Diagram (PLCC Chip)



12-2548.f (F)

Figure 3. 44-Pin Diagram (PLCC Chip)

Pin Information (continued)

Table 2. Pin Descriptions

32-Pin	44-Pin	Symbol	Type	Description
9	1	DCOUT	O	**dc Output Voltage.** This output is a voltage that is directly proportional to the absolute value of the differential tip/ring current.
10	2	I_{PROG}	I	**Current-Limit Program Input.** A resistor to DCOUT sets the dc current limit of the device.
11	3	CF2	—	**Filter Capacitor 2.** Connect a 0.1 µF capacitor from this pin to AGND.
12	4	CF1	—	**Filter Capacitor 1.** Connect a 0.47 µF capacitor from this pin to pin CF2.
—	5	SN	I	**Summing Node.** The inverting input of the uncommitted operational amplifier. A resistor or network to XMT sets the gain (44-pin PLCC only).
—	6	XMT	O	**Transmit ac Output Voltage.** The output of the uncommitted operational amplifier (44-pin PLCC only).
13	7	RTSN	I	**Ring Trip Sense Negative.** Connect this pin to the ringing generator signal through a high-value resistor.
14	8	RTSP	I	**Ring Trip Sense Positive.** Connect this pin to the ring relay and the ringer series resistor through a high-value resistor.
—	9	NC	—	**No Connection.** May be used as a tie point.
15	10	AGND	—	**Analog Signal Ground.**
—	11	NC	—	**No Connection.** May be used as a tie point.
16	12	V_{CC}	—	**5 V Power Supply.**
17	13	V_{BAT1}	—	**Battery Supply.** Negative high-voltage battery, higher in magnitude than V_{BAT2}.
18	14	V_{BAT2}	—	**Auxiliary Battery Supply.** Negative high-voltage battery, lower in magnitude than V_{BAT1}, used to reduce power dissipation on short loops.
19	15	BGND	—	**Battery Ground.** Ground return for the battery supply.
20	16	RGDET	O	**Ring Ground Detect.** When high, this open-collector output indicates the presence of a ring ground. To use, connect a 100 kΩ resistor to V_{CC}.
21	17	ICM	I	**Common-Mode Current Sense.** To program ring ground sense threshold, connect a resistor to V_{CC} and connect a capacitor to AGND to filter 50/60 Hz. If unused, the pin should be connected to ground.
22	18	BS2	—	**Battery Switch Slowdown.** Connect a 0.22 µF capacitor to pin BS1.
23	19	BS1	—	**Battery Switch Slowdown.** Connect a 0.22 µF capacitor to pin BS2. Also, connect a 0.1 µF capacitor in series with a 100 Ω resistor from BS1 to V_{BAT1} for stability.
—	20	NC	—	**No Connection.** May be used as a tie point.
—	21	NC	—	**No Connection.** May be used as a tie point.
24	22	PT	I/O	**Protected Tip.** The output of the tip driver amplifier and input to loop sensing. Connect to loop through overvoltage protection.
25	23	PR	I/O	**Protected Ring.** The output of the ring driver amplifier and input to loop sensing circuitry. Connect to loop through overvoltage protection.

Pin Information (continued)

Table 2. Pin Descriptions (continued)

32-Pin	44-Pin	Symbol	Type	Description
—	24	NC	—	**No Connection.** May be used as a tie point.
26	25	B2	I	**State Control Input.** B0, B1, B2, and BR determine the state of the SLIC. See Table 3. Pin B2 has a 40 kΩ pull-up.
27	26	B1	I	**State Control Input.** B0, B1, B2, and BR determine the state of the SLIC. See Table 3. Pin B1 has a 40 kΩ pull-up.
28	27	B0	I	**State Control Input.** B0, B1, B2, and BR determine the state of the SLIC. See Table 3. Pin B0 has a 40 kΩ pull-up.
29	28	BR	I	**State Control Input.** B0, B1, B2, and BR determine the state of the SLIC. See Table 3. Pin BR has a 40 kΩ pull-up.
—	29	NC	—	**No Connection.** May be used as a tie point.
—	30	NC-NTP	—	**No Connection.** May **not** be used as a tie point.
—	31	NC	—	**No Connection.** May be used as a tie point.
30	32	TG	—	**Transmit Gain.** Connect a 4.32 kΩ resistor from this pin to VTX.
31	33	VTX	O	The voltage at this pin is directly proportional to the differential tip/ring current.
32	34	TXI	—	**ac/dc Separation.** Connect a 0.1 μF capacitor from this pin to VTX**.**
1	35	NSTAT	O	**Loop Detector Output/Ring Trip Detector Output.** This output is a wired-OR of the NLC/NRDET outputs. When low, this logic output indicates that an off-hook condition exists or that ringing has been tripped.
2	—	V_{EE}	—	**–5 V Power Supply L8560C.**
2	—	NC	—	**No Connection L8560A/D/F.** May be used as a tie point.
—	36	NC	—	**No Connection.** May be used as a tie point.
3	37	VITR	O	**ac Output Voltage.** This output is a voltage that is directly proportional to the differential ac tip/ring current.
4	38	RCVP	I	**Receive ac Signal Input (Noninverting).** This high-impedance input controls the ac differential voltage on tip and ring.
5	39	RCVN	I	**Receive ac Signal Input (Inverting).** This high-impedance input controls the ac differential voltage on tip and ring.
—	40	NC	—	**No Connection.** May be used as a tie point.
6	41	FB2	—	**Polarity Reversal Slowdown.** Connect a capacitor to ground.
7	42	FB1	—	**Polarity Reversal Slowdown.** Connect a capacitor to ground.
8	43	LCTH	I	**Loop Closure Threshold Input.** Connect a resistor to DCOUT to set off-hook threshold.
—	44	DCR	I	**dc Resistance.** Short to analog ground for dc feed resistance of 55 Ω. The dc feed resistance can be increased to a nominal 760 Ω by shorting DCR to DCOUT. Intermediate values can be set by a simple resistor divider from DCOUT to ground with the trip at DCR (44-pin PLCC only).

Functional Description

Table 3. Input State Coding

B0	B1	B2	BR	State/Definition
1	1	0	1	**Powerup, Forward Battery V_{BAT2}.** Pin PT is positive with respect to pin PR. V_{BAT2} is applied to the tip/ring drive amplifiers. On-hook transmission capability. All supervision active—an off-hook condition or a ring trip causes output NSTAT to go low.
1	0	0	1	**Powerup, Reverse Battery V_{BAT2}.** Pin PR is positive with respect to pin PT. V_{BAT2} is applied to the tip/ring drive amplifiers. On-hook transmission capability. All supervision active—an off-hook condition or a ring trip causes output NSTAT to go low.
1	1	1	1	**Powerup, Forward Battery V_{BAT1}.** Pin PT is positive with respect to pin PR. V_{BAT1} is applied to the tip/ring drive amplifiers. On-hook transmission capability. All supervision active—an off-hook condition or a ring trip causes output NSTAT to go low.
1	0	1	1	**Powerup, Reverse Battery V_{BAT1}.** Pin PR is positive with respect to pin PT. V_{BAT1} is applied to the tip/ring drive amplifiers. On-hook transmission capability. All supervision active—an off-hook condition or a ring trip causes output NSTAT to go low.
0	1	1	1	**Ground Start.** Tip drive amplifier is turned off. The device presents a high impedance (>100 kΩ) to pin PT and a current-limited battery (V_{BAT1}) to pin PR. Output pin RGDET indicates current flowing in the ring lead.
0	0	1	1	**Low-Power Scan.** Except for off-hook supervision, all circuits are shut down to conserve power. Only the off-hook detector affects output pin NSTAT. V_{BAT1} is applied to the tip/ring drive amplifiers. Pin PT is positive with respect to pin PR. On-hook transmission is disabled.
0	1	0	1	**Low-Power Scan (L8560D/E/F/G Only).** Except for off-hook supervision, all circuits are shut down to conserve power. Only the off-hook detector affects output pin NSTAT. V_{BAT2} is applied to the tip/ring drive amplifiers. Pin PT is positive with respect to pin PR. On-hook transmission is disabled.
0	0	0	1	**Forward Disconnect.** The tip and ring amplifiers are turned off and the SLIC goes into a high-impedance state (>100 kΩ). V_{BAT2} is applied to the SLIC.
1	1/0	1	0	**Ring State.** SLIC is powered up. V_{BAT1} is applied to the tip and ring amplifiers. Current limit is increased by a factor of 2.8. Overhead voltage is reduced to approximately 2.4 V. These conditions are necessary to supply sufficient power to drive a true North American 5 REN ringing load (1386 Ω + 40 μF). Loop closure detector is disabled—only the ring trip detector affects output pin NSTAT. To apply a balanced ring signal to pins PR and PT, apply a 0 V to 5 V square wave to input pin B1. Ringing frequency is the frequency of the input wave at B1. To shape the ring signal at pins PR and PT, connect a capacitor from pin FB1 to ground and from pin FB2 to ground.

Table 4. Supervision Coding

Pin NSTAT	Pin RGDET
0 = off-hook or ring trip	1 = ring ground
1 = on-hook and no ring trip	0 = no ring ground

Absolute Maximum Ratings (T_A = 25 °C)

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Value	Unit
5 V Power Supply	V_{CC}	7.0	V
–5 V Power Supply (L8560C)	V_{EE}	–7.0	V
Battery (talking) Supplies	V_{BAT1}, V_{BAT2}	–75	V
V_{BAT2} Magnitude	$\|V_{BAT2}\|$	$\|V_{BAT1}\|$ + 0.4	V
Logic Input Voltage	—	–0.5 to +7.0	V
Analog Input Voltage	—	–7.0 to +7.0	V
Maximum Junction Temperature	T_J	165	°C
Storage Temperature Range	T_{stg}	–40 to +125	°C
Relative Humidity Range	R_H	5 to 95	%
Ground Potential Difference (BGND to AGND)	—	±3	V
PT or PR Fault Voltage (dc)	V_{PT}, V_{PR}	(V_{BAT1} – 5) to +3	V
PT or PR Fault Voltage (10 x 1000 µs)	V_{PT}, V_{PR}	(V_{BAT1} – 15) to +15	V
Current into Ring Trip Inputs	I_{RTSP}, I_{RTSN}	±240	µA

Note: The IC can be damaged unless all ground connections are applied before, and removed after, all other connections. Furthermore, when powering the device, the user must guarantee that no external potential creates a voltage on any pin of the device that exceeds the device ratings. Some of the known examples of conditions that cause such potentials during powerup are 1) an inductor connected to tip and ring can force an overvoltage on V_{BAT} through the protection devices if the V_{BAT} connection chatters, and 2) inductance in the V_{BAT} lead could resonate with the V_{BAT} filter capacitor to cause a destructive overvoltage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Ambient Temperature	–40	—	85	°C
Loop Closure Threshold-detection Programming Range	5	10	I_{LIM}	mA
dc Loop Current-limit Programming Range	5	40	50	mA
On- and Off-hook 2-wire Signal Level (@ Z_{LOOP} = 200 Ω)	—	—	2.2	Vrms
ac Termination Impedance Programming Range	150	600	1300	Ω
V_{BAT1}	–24	–48	–70	V
V_{BAT2}	–16	—	V_{BAT1}	V
V_{CC}	4.5	5.0	5.5	V
V_{EE} (L8560C)	–4.75	–5.0	–5.5	V
dc Feed Resistance Programming Range (excl. RP)	55	55	760	Ω

Electrical Characteristics

Minimum and maximum values are testing requirements in the temperature range of 25 °C to 85 °C and battery range of –24 V to –70 V. These minimum and maximum values are guaranteed to –40 °C based on component simulations and design verification of samples, but devices are not tested to –40 °C in production. The test circuit shown in Figure 5 is used, unless otherwise noted. Positive currents flow into the device.

Typical values are characteristics of the device design at 25 °C based on engineering evaluations and are not part of the test requirements. Supply values used for typical characterization are V_{CC} = 5.0 V, V_{EE} = –5.0 V, V_{BAT1} = –48 V, V_{BAT2} = –25.5 V, unless otherwise noted.

Electrical Characteristics (continued)

Table 5. Power Supply

V_{CC} = 5.0 V, V_{EE} = –5.0 V, V_{BAT1} = –48 V, V_{BAT2} = –19 V, unless otherwise noted.

Parameter	Min	Typ	Max	Unit
Power Supply Rejection 500 Hz to 3 kHz (See Figures 6, 7, 14, and 15.)[1]:				
V_{CC} (1 kHz), V_{EE} (1 kHz)[2]	35	—	—	dB
V_{BAT1}, V_{BAT2} (500 Hz—3 kHz)	45	—	—	dB
Thermal Protection Shutdown (T_{jc})	—	165	—	°C
Thermal Resistance, Junction to Ambient (θ_{JA}), Still Air, 44-pin PLCC	—	47	—	°C/W
Thermal Resistance, Junction to Ambient (θ_{JA}), Still Air, 32-pin PLCC	—	60	—	°C/W
Power Supply—Powerup, No Loop Current, V_{BAT2} Applied L8560A/D/E/F/G:				
I_{CC}	—	6.0	7.2	mA
I_{BAT1}	—	120	200	µA
I_{BAT2}	—	2.6	3.2	mA
Power Supply—Powerup, No Loop Current, V_{BAT1} Applied:				
I_{CC} (L8560A/D/E/F/G)	—	6.0	7.2	mA
I_{BAT1} (L8560A)	—	2.8	3.3	mA
I_{BAT1} (L8560D/E/F/G)	—	1.65	2.0	mA
I_{BAT2} (L8560D/E/F/G)	—	1.0	1.3	mA
Power Supply—Scan Mode, Forward Battery, No Loop Current, V_{BAT1} Applied:				
I_{CC} (L8560A/D/E/F/G)	—	4.0	5.2	mA
I_{BAT1} (L8560A)	—	1.3	1.6	mA
I_{BAT1} (L8560D/E/F/G)	—	0.5	0.75	mA
I_{BAT2} (L8560D/E/F/G)	—	0.9	1.2	mA
Power Supply—Scan Mode, Forward Battery, No Loop Current, V_{BAT2} Applied:				
I_{CC}	—	4.1	—	mA
I_{BAT1} (V_{BAT1} = –65 V)	—	200	—	µA
I_{BAT2} (V_{BAT2} = –30 V)	—	1.2	—	mA
Power Supply—Powerup, No Loop Current, L8560C Only:				
I_{CC}	—	5.8	7.2	mA
I_{EE}	—	0.9	1.26	mA
I_{BAT1} (V_{BAT1} applied)	—	1.65	2.2	mA
I_{BAT2} (V_{BAT2} applied)	—	1.50	1.96	mA
I_{BAT1} (V_{BAT2} applied)	—	120	200	µA
Power Supply—Scan, Forward Battery, No Loop Current, V_{BAT1} Applied, L8560C Only:				
I_{CC}	—	4.1	5.5	mA
I_{EE}	—	0.81	1.1	mA
I_{BAT} (V_{BAT1} applied)	—	0.43	0.56	mA
Power Supply—Ring Mode, No Loop Current:				
I_{CC}	—	6.45	—	mA
I_{BAT1}	—	2.2	—	mA

1. This parameter is not tested in production. It is guaranteed by design and device characterization.
2. V_{EE} used for L8560C version only.

Electrical Characteristics (continued)

Table 6. 2-Wire Port

Parameter	Min	Typ	Max	Unit
Tip or Ring Drive Current = dc + Longitudinal + Signal Currents	65	—	—	mA
Signal Current	15	—	—	mArms
Longitudinal Current Capability per Wire[1]	8.5	15	—	mArms
dc Loop Current Limit[2]:				
Programmability Range[3]	5	—	50	mA
Accuracy (B0 = BR = 5 V, R_{LOOP} = 100 Ω, V_{BAT1} = –48 V or V_{BAT2} = –25.5 V active)	—	—	±5	%
Powerup Open Loop Voltage Levels:				
Differential Voltage – V_{BAT2} (V_{BAT2} = –25.5 V)	$\lvert V_{BAT2} + 6.9\rvert$	$\lvert V_{BAT2} + 6.5\rvert$	$\lvert V_{BAT2} + 6.1\rvert$	V
Differential Voltage – V_{BAT1} (V_{BAT1} = –48 V)[4]	$\lvert V_{BAT1} + 7.1\rvert$	$\lvert V_{BAT1} + 6.7\rvert$	$\lvert V_{BAT1} + 6.3\rvert$	V
Differential Voltage – V_{BAT1} (ring mode)	$\lvert V_{BAT1} + 5.5\rvert$	$\lvert V_{BAT1} + 2.4\rvert$	—	V
Ground Start State:				
PT Resistance	100	—	—	kΩ
dc Feed Resistance (for I_{LOOP} below current limit)	—	55	80	Ω
Loop Resistance Range (3.17 dBm overload into 600 Ω; not including protection):				
I_{LOOP} = 20 mA at V_{BAT1} = –48 V	1940	—	—	Ω
I_{LOOP} = 20 mA at V_{BAT2} = –24 V	760	—	—	Ω
Longitudinal to Metallic Balance—*IEEE*[5] Std. 455 (See Figure 8.)[6, 7]:				
L8560A/C:				
200 Hz to 2999 Hz Forward/Reverse Battery	54	59	—	dB
3000 Hz to 3400 Hz Forward/Reverse Battery	49	54	—	dB
L8560D/E:				
200 Hz to 2999 Hz Forward Battery	63	68	—	dB
3000 Hz to 3400 Hz Forward Battery	58	63	—	dB
200 Hz to 2999 Hz Reverse Battery	58	63	—	dB
3000 Hz to 3400 Hz Reverse Battery	54	59	—	dB
L8560F/G:				
200 Hz to 2999 Hz Forward/Reverse Battery	50	55	—	dB
3000 Hz to 3400 Hz Forward/Reverse Battery	45	50	—	dB
Metallic to Longitudinal Balance:				
200 Hz to 4 kHz	46	—	—	dB
RFI Rejection (See Figure 9.)[3]:				
0.5 Vrms, 50 Ω Source, 30% AM Mod. 1 kHz	—	–55	–45	dBV
500 kHz to 100 MHz				

1. The longitudinal current is independent of dc loop current.
2. Current-limit I_{LIM} is programmed by a resistor, R_{PROG}, from pin IPROG to DCOUT. I_{LIM} is specified at the loop resistance where current limiting begins (see Figure 22). Select R_{PROG} (kΩ) = 0.616 x I_{LIM} (mA) – onset of current limit with input BR high. When input BR is low, the current will be increased by a factor of 2.8.
3. This parameter is not tested in production. It is guaranteed by design and device characterization.
4. Specification is reduced to $\lvert V_{BAT1} + 10.5\ V\rvert$ minimum when V_{BAT1} = –70 V at 85 °C.
5. *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.
6. Longitudinal balance of circuit card will depend on loop series protection resistor matching and magnitude.
7. Tested at 1000 Hz only. Full frequency specifications guaranteed by design and device characterization.

Electrical Characteristics (continued)

Table 7. Analog Pin Characteristics

Parameter	Min	Typ	Max	Unit
Differential PT/PR Current Sense (DCOUT):				
Gain (PT/PR to DCOUT)	—	–41.7	—	V/A
Offset Voltage @ I_{LOOP} = 0	–200	—	200	mV
Loop Closure Detector Threshold[1]:				
Programming Accuracy at 10 mA	—	—	±20	%
Ring Ground Detector Threshold[2]:				
R_{ICM} = 83 kΩ	3	6	10	kΩ
Programming Accuracy	—	—	±25	%
Ring Trip Comparator:				
Input Offset Voltage[3]	—	±10	—	mV
Internal Voltage Source (L8560A/D/E/F)	–8.6	–8.2	–7.6	V
Internal Voltage Source (L8560C)	–6.1	–5.7	–5.1	V
Current at Input RTSP[4]	I_N – 0.5	I_N	I_N + 0.5	µA
RCVN, RCVP:				
Input Bias Current	—	–0.2	–1	µA
Loop Closure Detector Hysteresis	—	2	—	mA
Variation	—	15	—	%
THD[3] at $V_{PT/PR}$ = 2.2 Vrms, V_{OH} = 12 V, Z_T = 200 Ω	—	—	–35	dB
VITR Output Impedance	—	5	—	Ω
VITR Output Offset Voltage	—	20	—	mV
Average/dc Current to FB1 and FB2 Tested as: (|FB1 (FB) (–5 V)| + |FB1 (FB) (–63 V)| + 2|FB1 (FB) (–35 V)| + |FB2 (FB) (–5 V)| + |FB2 (FB) (–63 V)| + 2|FB2 (FB) (–35 V)| + |FB1 (RB) (–5 V)| + |FB1 (RB) (–63 V)| + 2|FB1 (RB) (–35 V)| + |FB2 (RB) (–5 V)| + |FB2 (RB) (–63 V)| + 2|FB2 (RB) (–35 V)|)/16	—	29	—	µA
Accuracy	—	—	±8	%

1. Loop closure threshold is programmed by resistor R_{LCTH} from pin LCTH to pin DCOUT.
2. Ring ground threshold is programmed by resistor R_{ICM2} from pin ICM to V_{CC}.
3. This parameter is not tested in production. It is guaranteed by design and device characterization.
4. I_N is the sourcing current at RTSN. Guaranteed if I_N is within 5 µA to 30 µA.

Table 8. Uncommitted Op Amp Characteristics (44-Pin PLCC Only)

Parameter	Min	Typ	Max	Unit
Input Offset Voltage	—	±5	—	mV
Input Offset Current	—	±10	—	nA
Input Bias Current	—	200	—	nA
Differential Input Resistance	—	1.5	—	MΩ
Output Voltage Swing (R_L = 10 kΩ)	—	±3.5	—	Vpk
Output Resistance (A_{VCL} = 1)	—	2.0	—	Ω
Small-signal GBW	—	700	—	kHz

Electrical Characteristics (continued)

Table 9. ac Feed Characteristics

Parameter	Min	Typ	Max	Unit
ac Termination Impedance[1]	150	—	1300	Ω
Longitudinal Impedance	—	0	—	Ω
Total Harmonic Distortion—200 Hz to 4 kHz[2]:				
Off-hook	—	—	0.3	%
On-hook	—	—	1.0	%
Transmit Gain, f = 1 kHz (PT/PR to VITR; see Figure 11.)	–392	–400	–408	V/A
Receive + Gain, f = 1 kHz (RCVP to PT/PR)	7.76	8.00	8.24	—
Receive – Gain, f = 1 kHz (RCVN to PT/PR)	–7.76	–8.00	–8.24	—
Group Delay[2]:				
Transmit, Powerup	—	1	—	µs
Receive	—	0.5	—	µs
Gain vs. Frequency (transmit and receive) (600 Ω termination; reference 1 kHz, 1 Vrms)[2]:				
200 Hz to 300 Hz	–1.00	0.0	0.05	dB
300 Hz to 3.4 kHz	–0.3	0.0	0.05	dB
3.4 kHz to 16 kHz	–3.0	–0.1	0.3	dB
16 kHz to 266 kHz	—	—	2.5	dB
Gain vs. Level (transmit and receive)(reference 0 dBV)[2]:				
–55 dB to +3 dB	–0.05	0	0.05	dB
Return Loss[2, 3]:				
200 Hz to 500 Hz	—	30	—	dB
500 Hz to 3400 Hz	—	36	—	dB
2-wire Idle-channel Noise (600 Ω termination):				
Psophometric[2]	—	–87	–77	dBmp
C-message	—	2	12	dBrnC
3 kHz Flat[2]	—	10	20	dBrn
4-wire Idle-channel Noise:				
Psophometric[2]	—	–82	–77	dBmp
C-message	—	7	12	dBrnC
3 kHz Flat[2]	—	15	20	dBrn
Transhybrid Loss[3]:				
200 Hz to 500 Hz	—	30	—	dB
500 Hz to 3400 Hz	—	36	—	dB

1. Set by external components. Any complex impedance R1 + R2 || C between 150 Ω and 1300 Ω can be synthesized.
2. This parameter is not tested in production. It is guaranteed by design and device characterization.
3. Return loss and transhybrid loss are functions of device gain accuracies and the external hybrid circuit. Guaranteed performance assumes 1% tolerance external components. Not tested in production.

Electrical Characteristics (continued)

Table 10. Logic Inputs and Outputs

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltages:					
Low Level (permissible range)	V_{IL}	–0.5	0.4	0.7	V
High Level (permissible range)	V_{IH}	2.0	2.4	V_{CC}	V
Input Currents:					
Low Level (V_{CC} = 5.25 V, V_I = 0.4 V)	I_{IL}	–75	–115	–300	µA
High Level (V_{CC} = 5.25 V, V_I = 2.4 V)	I_{IH}	–40	–60	–100	µA
Output Voltages (open collector with internal pull-up resistor):					
Low Level (V_{CC} = 4.75 V, I_{OL} = 360 µA)	V_{OL}	0	0.2	0.4	V
High Level (V_{CC} = 4.75 V, I_{OH} = –20 µA)	V_{OH}	2.4	—	V_{CC}	V

Ring Trip Requirements

- Ringing signal:
  — Voltage, minimum 35 Vrms, maximum 100 Vrms.
  — Frequency, 17 Hz to 23 Hz.
  — Crest factor, 1.4 to 2.
- Ringing trip:
  — ≤100 ms (typical), ≤250 ms (V_{BAT} = –33 V, loop length = 530 Ω).
- Pretrip:
  — The circuits in Figure 4 will not cause ringing trip.

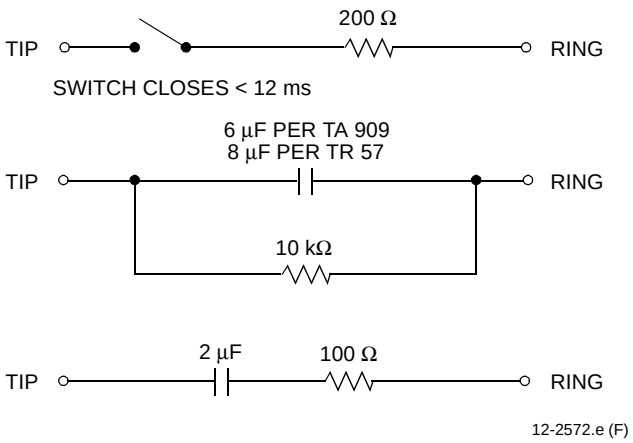


Figure 4. Ring Trip Circuits

Test Configurations

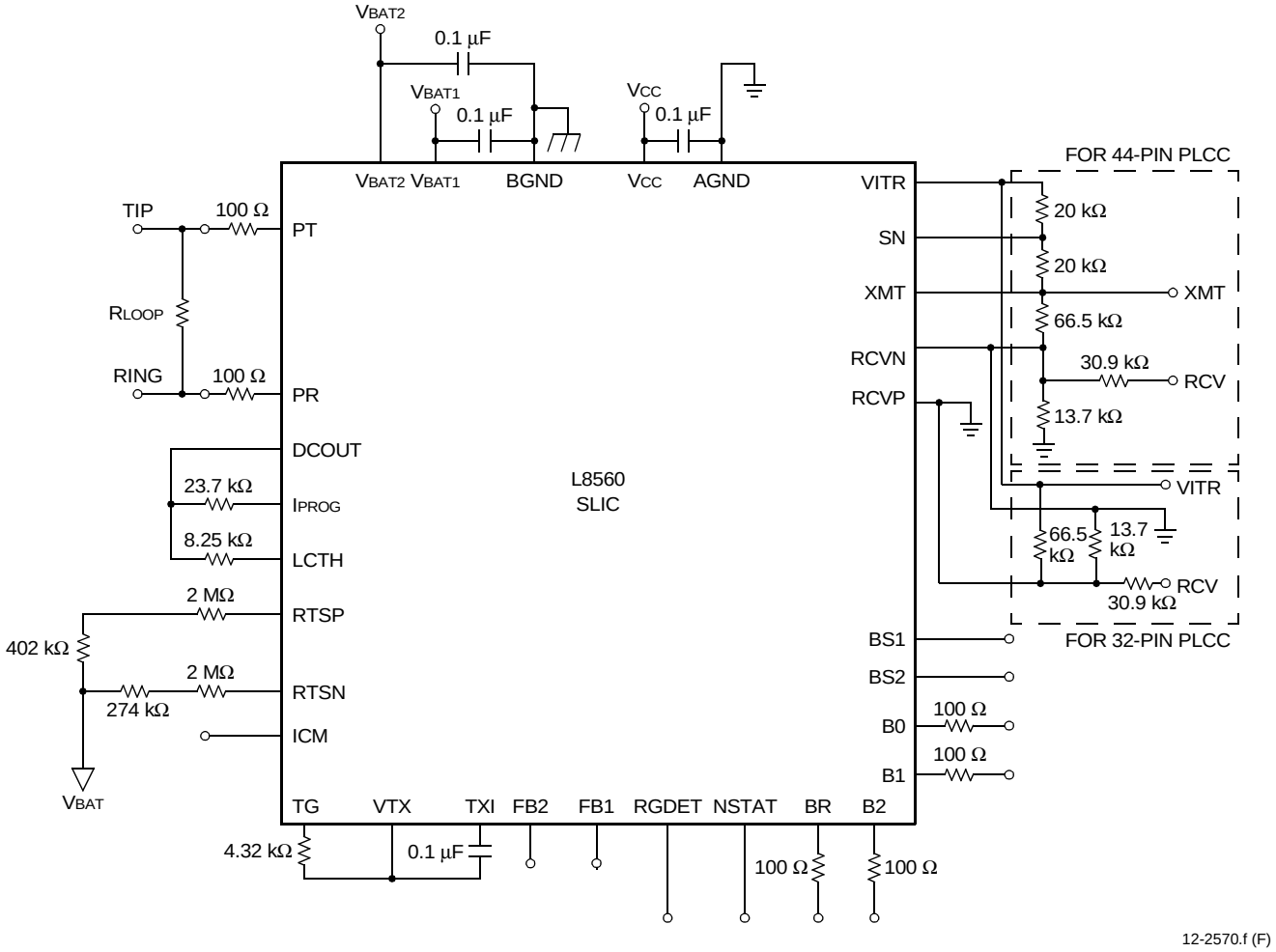


Figure 5. Basic Test Circuit

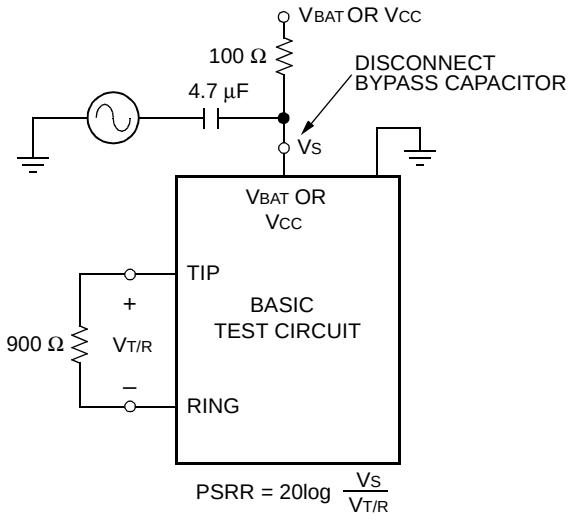


Figure 6. Metallic PSRR

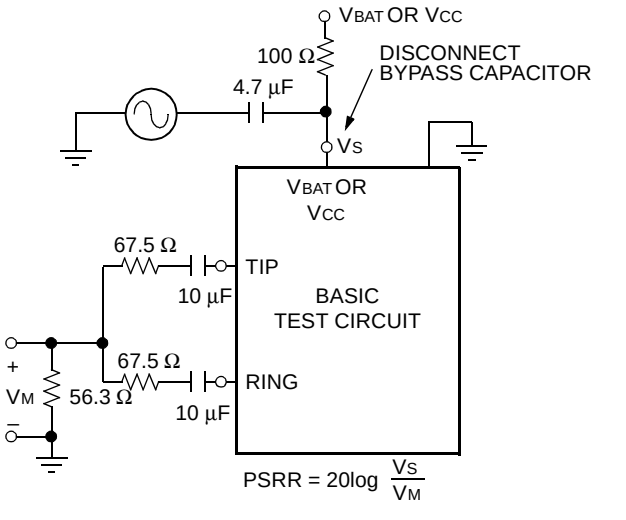
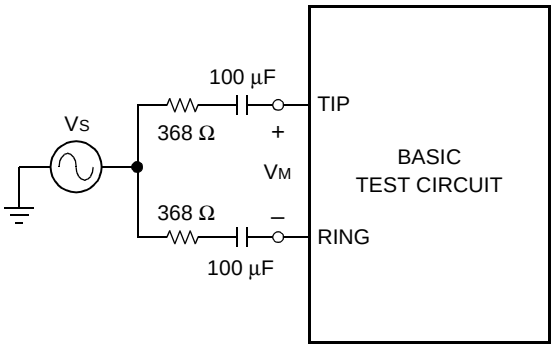


Figure 7. Longitudinal PSRR

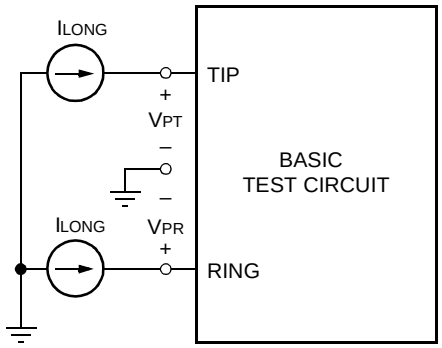
Test Configurations (continued)



$$\text{LONGITUDINAL BALANCE} = 20 \log \frac{V_S}{V_M}$$

12-2584.c (F)

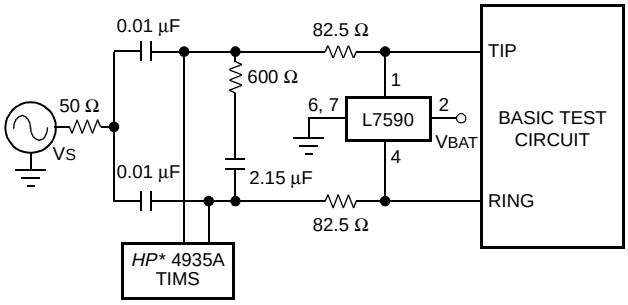
Figure 8. Longitudinal Balance



$$Z_{LONG} = \frac{\Delta V_{PT}}{\Delta I_{LONG}} \text{ OR } \frac{\Delta V_{PR}}{\Delta I_{LONG}}$$

12-2585.a (F)

Figure 10. Longitudinal Impedance



5-6756.a (F)

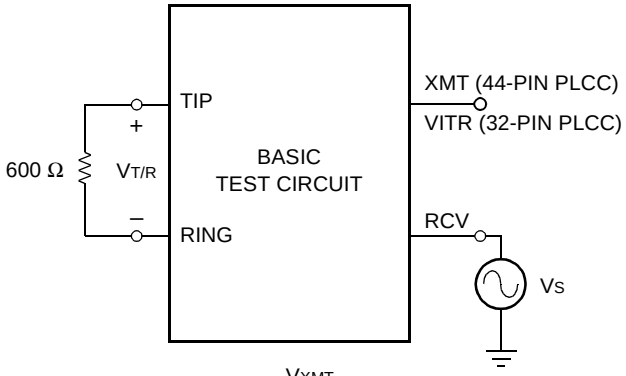
* *HP* is a registered trademark of Hewlett-Packard Company.

Notes:
V_S = 0.5 Vrms 30% AM 1 kHz modulation.

f = 500 kHz—1 MHz.

Device in powerup mode 600 Ω termination.

Figure 9. RFI Rejection



$$G_{XMT} = \frac{V_{XMT}}{V_{T/R}}$$

$$G_{RCV} = \frac{V_{T/R}}{V_{RCV}}$$

12-2587.d (F)

Figure 11. ac Gains

Applications

Characteristic Curves

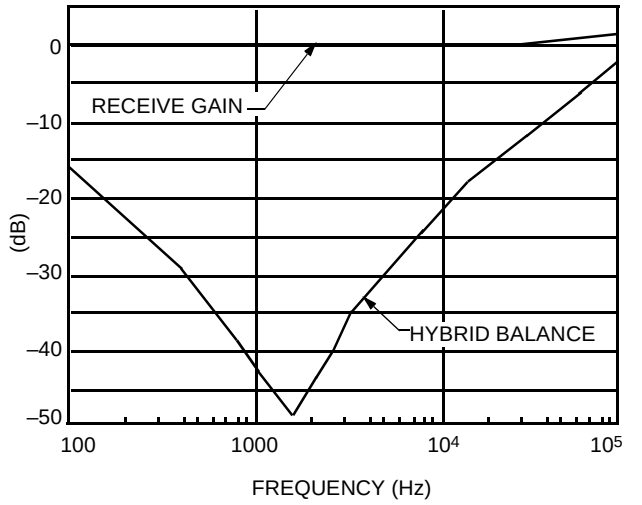


Figure 12. L8560 Receive Gain and Hybrid Balance vs. Frequency

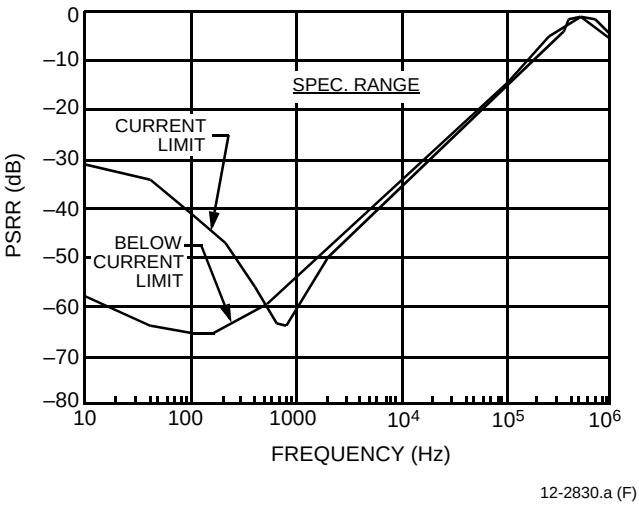


Figure 14. L8560 Typical V_{CC} Power Supply Rejection

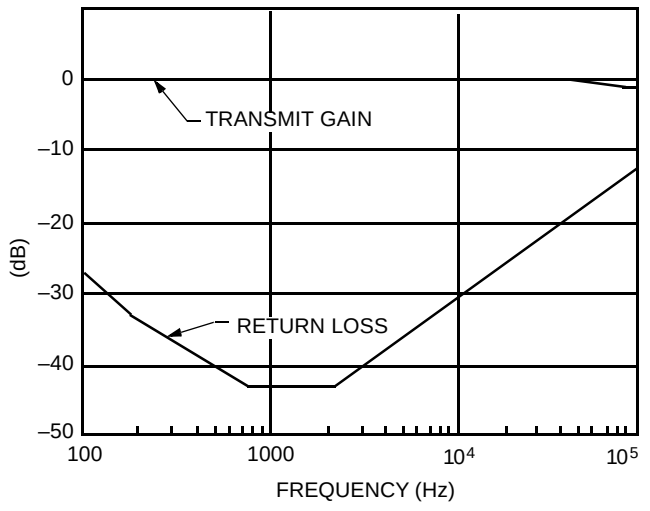


Figure 13. L8560 Transmit Gain and Return Loss vs. Frequency

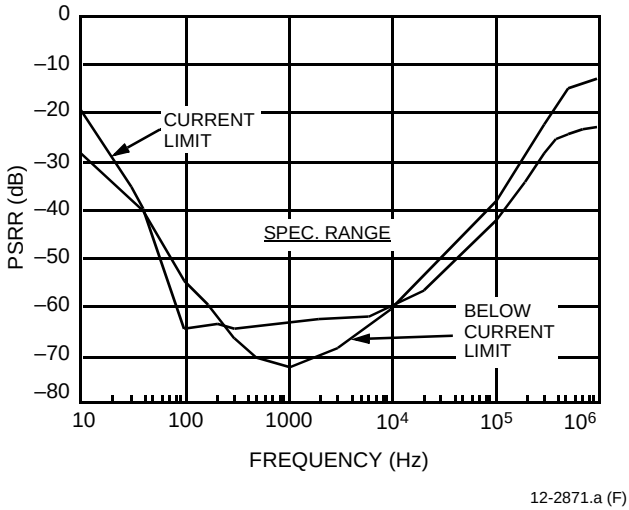
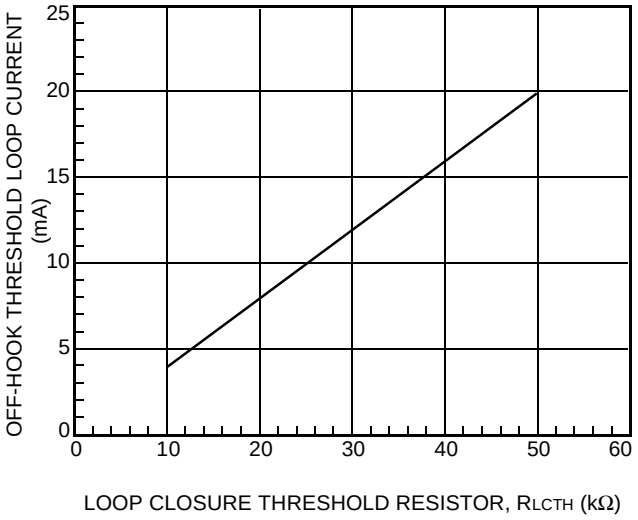


Figure 15. L8560 Typical V_{BAT} Power Supply Rejection

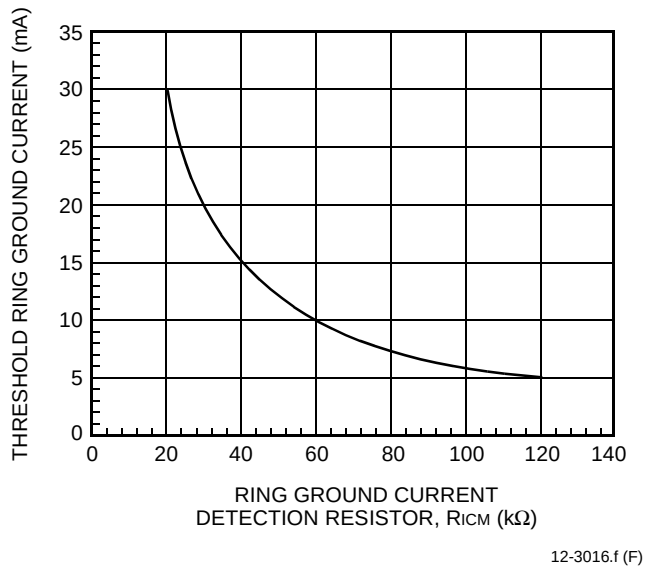
Applications (continued)

Characteristic Curves (continued)



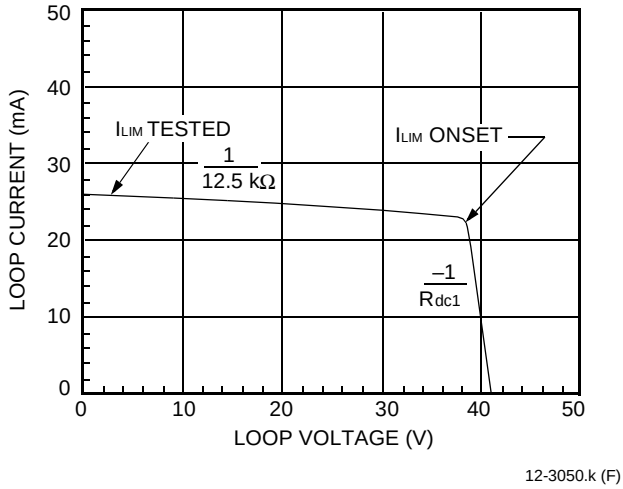
Note: V_{BAT1} = –48 V, I_{TR} = 1.2 x 10^{-3} R_{LCTH} (kΩ).

Figure 16. Loop Closure Program Resistor Selection



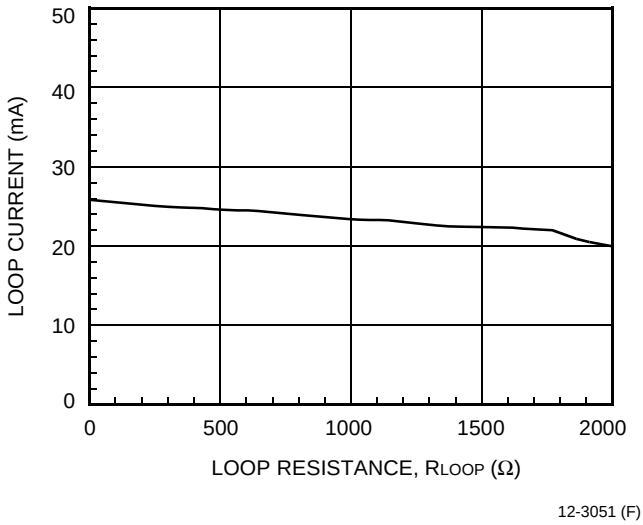
Note: Tip lead is open; V_{BAT1} = –48 V.

Figure 17. Ring Ground Detection Programming



Note: V_{BAT1} = –48 V; I_{LIM} = 22 mA; R_{dc1} = 55 Ω.

Figure 18. Loop Current vs. Loop Voltage

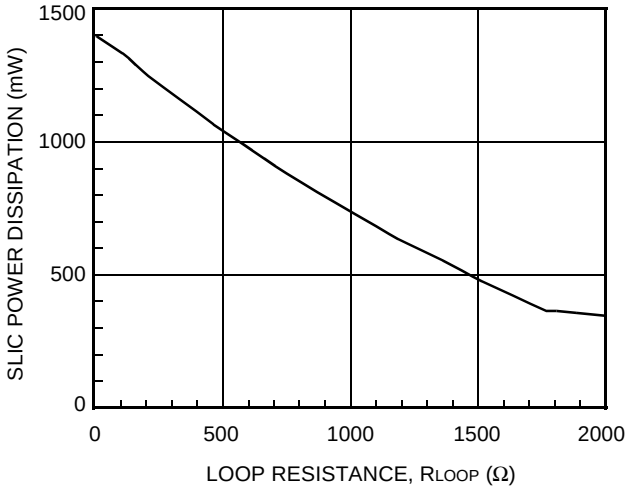


Note: V_{BAT1} = –48 V; I_{LIM} = 22 mA; R_{dc1} = 55 Ω.

Figure 19. Loop Current vs. Loop Resistance

Applications (continued)

Characteristic Curves (continued)



Note: V_{BAT1} = –48 V; I_{LIM} = 22 mA; R_{dc1} = 55 Ω.

Figure 20. L8560 Typical SLIC Power Dissipation vs. Loop Resistance

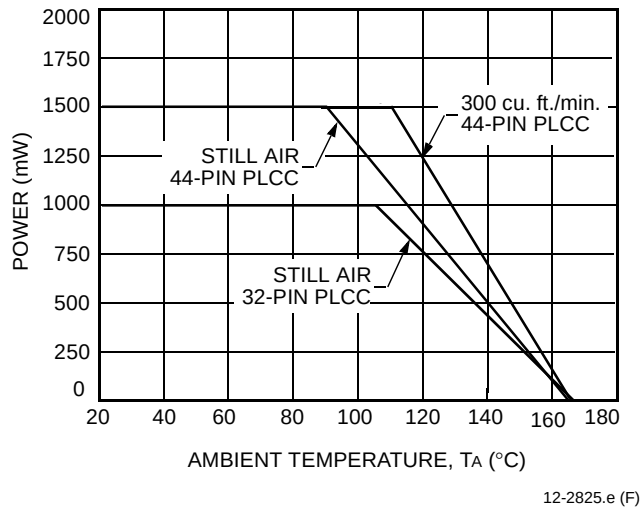


Figure 21. Power Derating

dc Applications

Battery Feed

The dc feed characteristic can be described by:

$$V_{T/R} = \frac{(|V_{BAT}| - V_{OH}) \times R_L}{R_L + 2R_P + R_{dc}}$$

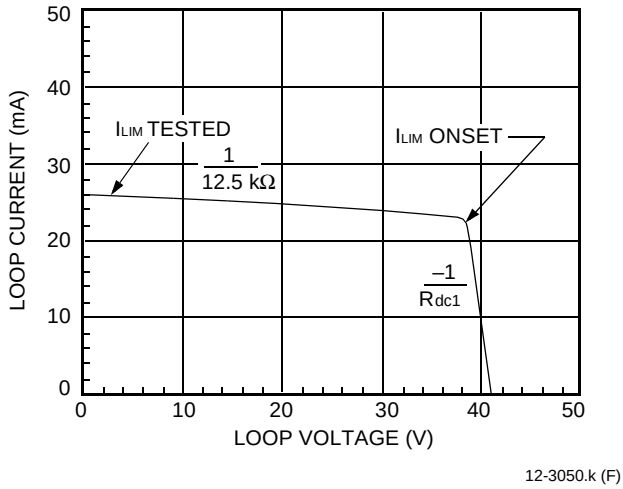
$$I_L = \frac{|V_{BAT}| - V_{OH}}{R_L + 2R_P + R_{dc}}$$

where:
I_L = dc loop current.
$V_{T/R}$ = dc loop voltage.
$|V_{BAT}|$ = battery voltage magnitude.

Note: The L8560 has a battery switch circuit that allows use of a primary battery, V_{BAT1}, or an auxiliary battery, V_{BAT2}. $|V_{BAT}|$ is the battery, V_{BAT1} or V_{BAT2}, that is active. See the Battery Switch section for more information.

V_{OH} = overhead voltage. This is the difference between the battery voltage and the open loop tip/ring voltage.
R_L = loop resistance, not including protection resistors.
R_P = protection resistor value.
R_{dc} = SLIC internal dc feed resistance.

The design begins by drawing the desired dc template. An example is shown in Figure 22.



Note: V_{BAT1} = –48 V; I_{LIM} = 22 mA; R_{dc1} = 55 Ω.

Figure 22. Loop Current vs. Loop Voltage

Applications (continued)

dc Applications (continued)

Starting from the on-hook condition and going through to a short circuit, the curve passes through two regions:

Region 1: On-hook and low loop currents. In this region, the slope corresponds to the dc resistance of the SLIC, R_{dc1} (default is 55 Ω typical). The open circuit voltage is the battery voltage less the overhead voltage of the device, V_{OH} (default is 6.7 V typical). These values are suitable for most applications but can be adjusted if needed. For more information, see the sections titled Adjusting dc Feed Resistance or Adjusting Overhead Voltage.

Region 2: Current limit. The dc current is limited to a starting value determined by external resistor R_{PROG}, an internal current source, and the gain from tip/ring to pin DCOUT. Current limit is set by the equation:

$I_{PROG} \times R_{PROG} = I_{LIM} \times B_{DCOUT}$

Where:

I_{PROG} = the current from an internal current source

R_{PROG} = the external resistor used to set the current limit

B_{DCOUT} = the transconductance from tip/ring to DCOUT, which is nominally 41.67 V/A

During nonringing modes, the internal current source is set at 75 µA, thus:

$I_{PROG} \times R_{PROG} = I_{LIM} \times B_{DCOUT}$

$R_{PROG} = I_{LIM} \times B_{DCOUT}/I_{PROG}$

R_{PROG} (K) = I_{LIM} (mA) x 0.04167 (V/mA)/75e–3 (mA)

R_{PROG} (K) = 0.556 x I_{LIM} (mA)

Testing data shows that:

R_{PROG} (K) = 0.616 x I_{LIM} (mA)

This equation is a first-order estimation of the loop current at current-limit range.

For more precise loop current at current-limit range, the loop current is also determined by loop length, protection resistance, and battery voltage. It can be shown through calculations as follows:

Current-limit onset (I_{Lonset}):

$$I_{Lonset}\,(mA) = \frac{R_{PROG}\ (K)}{0.616}$$

Loop resistance where current-limit onsets (R_{Lonset}):

$$R_{Lonset}\,(\Omega) = \frac{(|V_{BAT}| - V_{OH})(V)}{I_{Lonset}(mA)} \times 1000 - 2R_P - Rdc$$

Tip/ring voltage where current-limit onsets ($V_{T/Ronset}$):

$$V_{T/Ronset} = \frac{(|V_{BAT}| - V_{OH}) \times R_{Lonset}}{R_{Lonset} + 2R_P + Rdc}$$

Tip/ring voltage when loop resistance is R_{loop} ($V_{T/Rloop}$):

$V_{T/Rloop}$ (V) = I_{loop} (mA) x R_{LOOP} (Ω)/1000

Loop current is now given by:

I_{loop} (mA) = I_{Lonset} (mA) + ($V_{T/Ronset}$ – $V_{T/Rloop}$) (V)/12.5 (kΩ)

or

$$I_{loop}\,(mA) = \frac{I_{Lonset}(mA) + V_{T/Ronset}(V)/12.5(k\Omega)}{1 + R_{loop}\,(\Omega)/12500(k\Omega)}$$

Current limit is not sensitive to temperature variation.

Overhead Voltage

In order to drive an on-hook ac signal, the SLIC must set up the tip and ring voltage to a value less than the battery voltage. The amount that the open loop voltage is decreased relative to the battery is referred to as the overhead voltage and is expressed as:

$$V_{OH} = |V_{BAT}| - (V_{PT} - V_{PR})$$

Without this buffer voltage, amplifier saturation will occur and the signal will be clipped. The L8560 is automatically set at the factory to allow undistorted on-hook transmission of a 3.17 dBm signal into a 900 Ω loop impedance.

The drive amplifiers are capable of 4 Vrms minimum (V_{AMP}). So, the maximum signal the device can guarantee is:

$$V_{T/R} = 4\ V\left(\frac{|Z_{T/R}|}{|Z_{T/R}| + 2R_P}\right)$$

For applications where higher signal levels are needed, e.g., periodic pulse metering, the 2-wire port of the SLIC can be programmed with pin DCR (pin DCR is not available in the 32-pin PLCC package). The first step is to determine the amount of overhead voltage needed. The peak voltage at output of tip and ring amplifiers is related to the peak signal voltage by:

$$\hat{V}_{AMP} = \hat{V}_{T/R}\left(1 + \frac{2R_P}{|Z_{T/R}|}\right)$$

Applications (continued)

dc Applications (continued)

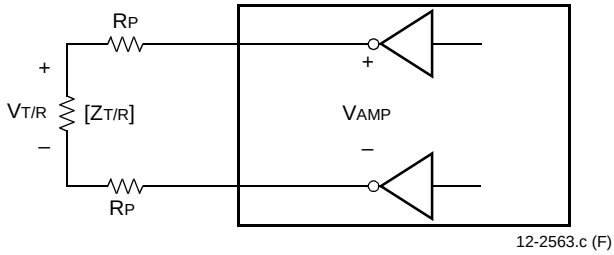


Figure 23. SLIC 2-Wire Output Stage

In addition to the required peak signal level, the SLIC needs about 2 V from each power supply to bias the amplifier circuitry. It can be thought of as an internal saturation voltage. Combining the saturation voltage and the peak signal level, the required overhead can be expressed as:

$$V_{OH} = V_{SAT} + \left(1 + \frac{2R_P}{|Z_{T/R}|}\right)\Lambda V_{T/R}$$

$$= V_{SAT} + \left(1 + \frac{2R_P}{|Z_{T/R}|}\right)\sqrt{\frac{2|Z_{T/R}|}{1000}} \times 10^{dBm/20}$$

where V_{SAT} is the combined internal saturation voltage between the tip/ring amplifiers and V_{BAT} (4.0 V typ.). R_P (Ω) is the protection resistor value. $Z_{T/R}$ (Ω) is the ac loop impedance.

Example 1, On-Hook Transmission of a Meter Pulse:

Signal level: 2.2 Vrms into 200 Ω
35 Ω protection resistors
I_{LOOP} = 0 (on-hook transmission of the metering signal)

$$V_{OH} = 4.0 + \left(1 + \frac{2 \times 35}{200}\right)\sqrt{2}\,(2.2)$$

$$= 8.2 \text{ V}$$

Accounting for V_{SAT} tolerance of 0.5 V, a nominal overhead of 8.7 V would ensure transmission of an undistorted 2.2 V metering signal.

Adjusting Overhead Voltage

To adjust the open loop 2-wire voltage, pin DCR (44-pin PLCC only) is programmed at the midpoint of a resistive divider from ground to either –5 V or V_{BAT}. In the case of –5 V, the overhead voltage will be independent of the battery voltage. Figure 24 shows the equivalent input circuit to adjust the overhead.

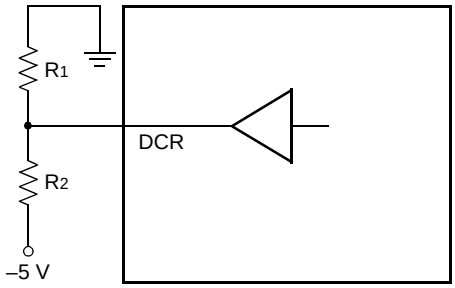


Figure 24. Equivalent Circuit for Adjusting the Overhead Voltage

The overhead voltage is programmed by using the following equation:

$$V_{OH} = 7.1 - 18.18\ V_{DCR}$$

$$= 7.1 - 18.18\left(-5 \times \left(\frac{R_1}{R_2 + R_1}\right)\right)$$

Adjusting dc Feed Resistance

The dc feed resistance may be adjusted with the help of Figure 25.

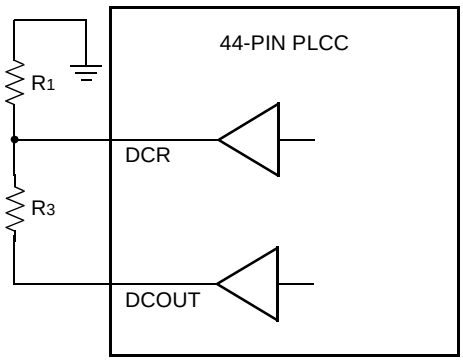


Figure 25. Equivalent Circuit for Adjusting the dc Feed Resistance

$$R_{dc} = 55\ \Omega + 705\ \Omega \frac{\Delta V_{DCR}}{\Delta V_{DCOUT}}$$

$$= 55\ \Omega + 705\ \Omega \left(\frac{R_1}{R_3 + R_1}\right)$$

Applications (continued)

dc Applications (continued)

Adjusting Overhead Voltage and dc Feed Resistance Simultaneously

The above paragraphs describe the independent setting of the overhead voltage and the dc feed resistance. If both need to be set to customized values, combine the two circuits as shown in Figure 26.

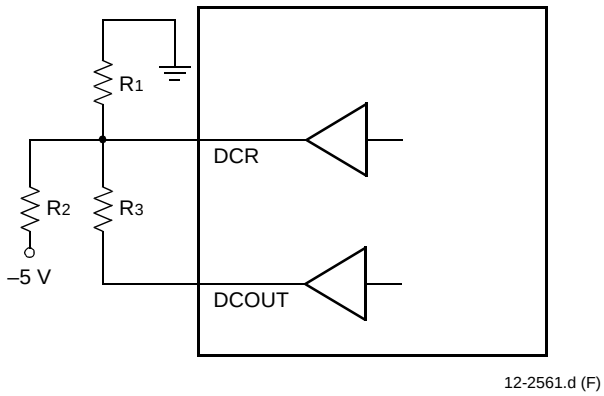


Figure 26. Adjusting Both Overhead Voltage and dc Feed Resistance

This is an equivalent circuit for adjusting both the dc feed resistance and overhead voltage together.

The adjustments can be made by simple superposition of the overhead and dc feed equations:

$$V_{OH} = 7.1 + 40\left(\frac{R_1 \| R_3}{R_2 + R_1 \| R_3}\right)$$

$$R_{dc} = 55\ k\Omega + 705\ \Omega\left(\frac{R_1}{R_2 + R_1}\right)$$

Lower-value resistors can be used; the only disadvantage is the power consumption of the external resistors.

Loop Range

The equation below can be rearranged to provide the loop range for a required loop current:

$$R_L = \frac{|V_{BAT}| - V_{OH}}{I_L} - 2R_P - R_{dc}$$

Off-Hook Detection

The loop closure comparator has built-in longitudinal rejection, eliminating the need for an external 60 Hz filter. This applies in both powerup and low-power scan states. The loop closure detection threshold is set by resistor R_{LCTH}. Referring to Figure 27, NLC is high in an on-hook condition (I_{TR} = 0, V_{DCOUT} = 0) and V_{LCTH} = 0.05 mA x R_{LCTH}. The off-hook comparator goes low when V_{LCTH} crosses zero and then goes negative:

$$V_{LCTH} = 0.05\ mA \times R_{LCTH} + V_{DCOUT}$$
$$= 0.05 \times R_{LCTH} – 0.04167\ V/mA \times I_{TR}$$
$$R_{LTCH}\ (k\Omega) = 0.833\ I_{TR}\ (mA)$$

Testing data shows that:

$$R_{LTCH}\ (k\Omega) = 0.899\ I_{TR}\ (mA)$$

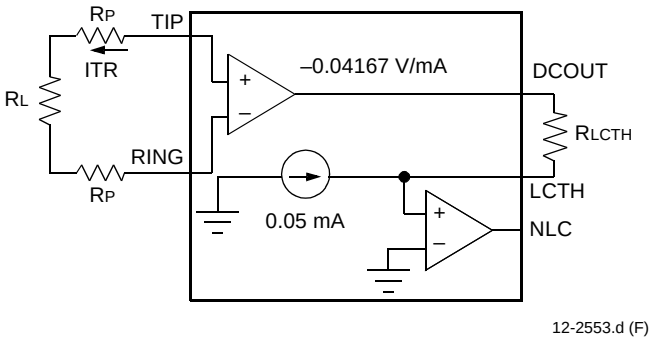


Figure 27. Off-Hook Detection Circuit

Note that NLC is internally wired-OR with the output of the ring trip detector (NRDET). The wired-OR, NSTAT, is a package output pin.

Note that if NSTAT is used to directly control logic input B2, connect a 0.01 µF capacitor from node LCTH to ground for filtering purposes. In this mode of operation, the L8560 will automatically switch to the lower-voltage battery under off-hook conditions.

Also note that NSTAT will toggle low with a ring ground in the ground start application. Under a ring ground, one-half of the current appears as differential. This total ring ground current is approximately two times the current limit; thus, the differential current is approximately equal to the current limit, which typically exceeds the loop closure threshold. Thus, in the ground start application, if RGDET trips, NSTAT will also trip. Under this condition, via software, ignore the NSTAT transition.

Applications (continued)

dc Applications (continued)

Ring Ground Detection

Pin ICM sinks a current proportional to the longitudinal loop current. It is also connected to an internal comparator whose output is pin RGDET. In a ground start application where tip is open, the ring ground current is half differential and half common mode. In this case, to set the ring ground current threshold, connect a resistor R_{ICM} from pin ICM to V_{CC}. Select the resistor according to the following relation:

$$R_{ICM}\,(k\Omega) = \frac{V_{CC} \times 120}{I_{RG}\,(mA)}$$

The above equation is shown graphically in Figure 17. It applies for the case of tip open. The more general equation can be used in ground key applications to detect a common-mode current ICM:

$$R_{ICM}\,(k\Omega) = \frac{V_{CC} \times 60}{ICM\,(mA)}$$

Longitudinal Balance

The SLICs are graded with different codes to represent different longitudinal balance specifications. The numbers are guaranteed by testing (Figures 5 and 8). However, for specific applications, the longitudinal balance may also be determined by termination impedance, protection resistance, and especially by the mismatch between protection resistors at tip and ring. This can be illustrated by:

$$LB = 20 \times \log \frac{(368 + RP) \times (368 + ZT - RP)}{368 \times (2 \times [ZT - 2 \times RP] \times \Delta + \varepsilon)}$$

where:

LB: longitudinal balance
RP: protection resistor value in Ω
ZT: magnitude of the termination impedance in Ω
ε: protection resistor mismatch in Ω
Δ: SLIC internal tip/ring sensing mismatch

The Δ can be calculated using the above equation with these exceptions: $\varepsilon = 0$, ZT = 600 Ω, RP = 100 Ω, and the longitudinal balance specification on a specific code.

Now with Δ available, the equation will predict the actual longitudinal balance for RP, ZT, and ε.

Be aware that ZT may vary with frequency for complex impedance applications.

Power Derating

Thermal considerations can affect the choice of a 32-pin PLCC or a 44-pin PLCC package. Operating temperature range, maximum current limit, maximum battery voltage, minimum dc loop, and protection resistor values will influence the overall thermal performance. This section shows the relevant design equations and considerations in evaluating the SLIC thermal performance.

First, consider the L8560 SLIC in a 44-pin PLCC package. The still-air thermal resistance is 47 °C/W; however, this number implies zero airflow as if the L8560 were totally enclosed in a box. A more realistic number would be 43 °C/W. This is an experimental number that represents a thermal impedance with no forced airflow (i.e., from a muffin fan) but from the natural airflow as seen in a typical switch cabinet.

The SLIC will enter the thermal shutdown state at typically 165 °C. The thermal shutdown design should ensure that the SLIC temperature does not reach 165 °C under normal operating conditions.

Assume a maximum ambient operating temperature of 85 °C, a maximum current limit of 45 mA, and a maximum battery of –52 V. Further, assume a (worst case) minimum dc loop of 100 Ω and that 100 Ω protection resistors are used at both tip and ring.

1. $T_{TSD} - T_{AMBIENT(max)}$ = allowed thermal rise.
   165 °C – 85 °C = 80 °C
2. Allowed thermal rise = package thermal impedance • SLIC power dissipation.
   80 °C = 43 °C/W • SLIC power dissipation
   SLIC power dissipation (P_D) = 1.9 W

Thus, if the total power dissipated in the SLIC is less than 1.9 W, it will not enter the thermal shutdown state. Total SLIC power is calculated as:

Total P_D = maximum battery • maximum current limit + SLIC quiescent power.

For the L8560, SLIC quiescent power (P_Q) is approximated at 0.167 W. Thus,

Total P_D = (–52 V • 45 mA) + 0.167 W
Total P_D = 2.34 W + 0.167 W
Total P_D = 2.507 W

Applications (continued)

Power Derating (continued)

The power dissipated in the SLIC is the total power dissipation less the power that is dissipated in the loop.

SLIC P_D = Total power – Loop power
Loop power = $(I_{LIM})^2 \bullet (R_{LOOP(dc)}$ min + $2R_P)$
Loop power = $(45\ mA)^2 \bullet (100\ \Omega + 200\ \Omega)$
Loop power = 0.61 W
SLIC power = 2.507 W – 0.61 W
SLIC power = 1.897 W < 1.9 W

Thus, in this example, the thermal design ensures that the SLIC will not enter the thermal shutdown state.

The next example uses the 32-pin PLCC package and demonstrates the technique used to determine the maximum allowed current.

In this example, assume a 0 °C to 70 °C operating range. Thus,

$T_{TSD} - T_{AMBIENT\ (max)}$ = allowed thermal rise
165 °C – 70 °C = 95 °C

To estimate the open-air thermal impedance, use the 43 °C/W parameter from the 44-pin PLCC and ratio the lead count.

Thermal impedance (32-pin PLCC) = 48 °C/W $\bullet \left[\frac{44}{32}\right]$ = 59 °C/W

Again:

Allowed thermal rise = thermal impedance • SLIC power dissipation
95 °C = 59 °C/W • SLIC power dissipation
SLIC P_D = 1.6 W

In this example, again assume the dc loop + 2 • protection resistors = 300 Ω, then:

$(I_{LIM})(V_{BAT}$ max) + $P_Q - (I_{LIM})^2 (R_{dc} + 2\ R_P) = 1.6$ W
$I \bullet 52 + 0.167 - I^2\ 300 = 1.6$ W
$300\ I^2 - 52\ I + 1.433 = 0$

This is a quadratic equation whose solution is in the form:

$$X = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

$$I_{LIM} = \frac{52 \pm \sqrt{52^2 - (4)(300)(1.433)}}{2(300)}$$

$$I_{LIM} = \frac{52 \pm 31.4}{600}$$

Ignore the "+" term:

$$I_{LIM} = \frac{52 - 31.4}{600} = 34\ mA$$

Thus, 34 mA is the maximum allowable current limit in the 32-pin PLCC package under the conditions given in this example.

This type of analysis should be performed under the conditions of the user's particular application to ensure adequate thermal design.

Battery Switch

The L8560 SLIC provides an input for an auxiliary battery. Called V_{BAT2}, this power supply should be lower in magnitude than the primary battery V_{BAT1}. Under an acceptable loop condition, V_{BAT2} can be switched to provide the loop power through the amplifiers of the SLIC. The dc template, described in previous sections, is determined by the battery that is active—either V_{BAT1} or V_{BAT2}.

There are several important applications where use of a lower-voltage battery in the off-hook state is desired to provide dc current to the loop, yet a higher-voltage battery is desired in on-hook or ringing modes. These applications are typically short-loop applications, such as an ISDN terminal adapter, fiber-in-the-loop applications, or a cable telephony interface.

Typically, in these applications, the maximum dc loop resistance (which includes the off-hook telephone handset plus twisted-cable pair) is relatively low. For example, Bellcore TA-909, *Generic Requirements and Objectives for Fiber in the Loop Systems*, specifies that in the off-hook state, 20 mA must be provided into a 430 Ω dc loop. To meet these requirements, a lower battery in the off-hook condition is important to minimize off-hook power consumption. Power conservation is important from a cost of energy point of view and is vital in remotely powered POTS interface applications.

While use of a low-voltage battery in off-hook short dc loops is important, certain on-hook applications, such as providing a balanced power ring signal or maintaining compatibility with certain CPE such as answering machines, may require a higher magnitude battery.

With the logic-controlled battery switch, the L8560 is able to provide a higher-voltage battery to meet on-hook battery voltage requirements. At the same time, the L8560 can accept a lower-voltage auxiliary battery during short-loop, off-hook applications. If a dc/dc converter with two fixed voltage outputs is used, tie the battery voltage that is higher in magnitude to V_{BAT1} and the voltage that is lower in magnitude to V_{BAT2}. If it is

Applications (continued)

Battery Switch (continued)

desired to use a single battery supply or a dc/dc converter with a single programmable voltage output, tie V_{BAT1} to V_{BAT2} and connect the battery to this node. Note that V_{BAT1} is forced during the balanced ringing state.

VCC/VEE Supplies

The L8560A/D/E/F SLICs are designed to operate using battery and only a 5 V power supply. In this mode of operation, power for the tip/ring drive amplifiers, dc feedback loop, internal amplifiers, logic, ac, and reference circuits is drawn from the negative battery (and 5 V supply).

While the L8560A/D/E/F type devices offer very low power dissipation in both the sleep and active states, further reduction in power dissipation is possible by use of battery and +5 V and –5 V power supplies. The L8560C operates using battery, +5 V, and –5 V power supplies. When the –5 V is used, the internal amplifiers, logic, ac, and reference circuits draw power from the negative –5 V supply, not the negative battery. Since the magnitude of the –5 V supply is less than the battery, power consumption is reduced. With the L8560C, the tip/ring drive amplifiers and dc feedback loop still draw power from the battery.

Power Ringing

The L8560 ringing SLIC is designed with the capability of generating balanced power ring signal to tip and ring. Because the SLIC itself generates the power ringing signal, no ring relay is needed in this mode of operation. Alternatively, the L8560 SLIC can also be used in the more standard battery-backed, unbalanced ringing application. In this case, the ring signal is generated by a central ring generator and is bused to individual tip/ring pairs. A ringing relay is used during ringing to disconnect the SLIC from, and apply the ring generator to, the tip and ring pair.

This section discusses in detail the use of the L8560 ringing SLIC in either mode of application.

Ringing SLIC Balanced Ring Signal Generation

The internal dc current source drives current into or pulls current out from C_{FB1} and C_{FB2} depending on whether the SLIC is operating at battery forward or at battery reversal. The voltage at PT then will be positive with respect to PR or vice versa. If a square wave signal is added to B1, the SLIC will be operating consecutively at battery forward, and then battery reversal. The differential output at PT and PR can be a balanced power ringing signal. Its frequency is equal to that of the square wave at B1. Its slew rate is determined by the size of the capacitors C_{FB1} and C_{FB2}.

If a sinusoidally modulated pulse-width-modulation (PWM) signal is applied to B1, the differential output at PT and PR will be sinusoidal. Theoretically, it provides power ringing in a sinusoidal format. For more information, please refer to the *L8560 Sinusoidal Ringing Generation Using a PWM Input to B1* Application Note.

POTS for ISDN Terminal Adapters

The L8560 ringing SLIC is designed to provide a balanced power ring signal to tip and ring. This mode of operation is suited for short-loop, plain old telephone service (POTS) applications, such as ISDN terminal adapters (TA).

When ISDN was first visualized, it was thought that we would all exchange our existing telephones for new, full-feature ISDN phones. Digital technology would drive these sets to very low costs. While this may happen in the future, the current demand is for the ISDN TA to service a standard analog telephone. The challenges of this application are discussed here along with a suggested solution.

Until recently, POTS has been the exclusive domain of the service provider. Over its 100-year history, any architectural change was always required to be compatible with the existing installed local loop plant and all telephone sets.

If this is the expectation of the TA, it would be capable of being connected into the residence phone wiring to drive every phone in the house. It would also be designed with enough backup battery to provide uninterrupted service during electrical power interruptions. In this case, adherence to a standard, such as Bellcore's TA-909, is recommended.

For the case where a TA is only going to provide limited service, the design can be made less costly by limiting the scope of the device. An example of this limited scope would be the provision of analog jacks for a FAX/modem and a phone set near the TA in a home office environment. A block diagram of a POTS design is outlined in Figure 28.

Applications (continued)

Power Ringing (continued)

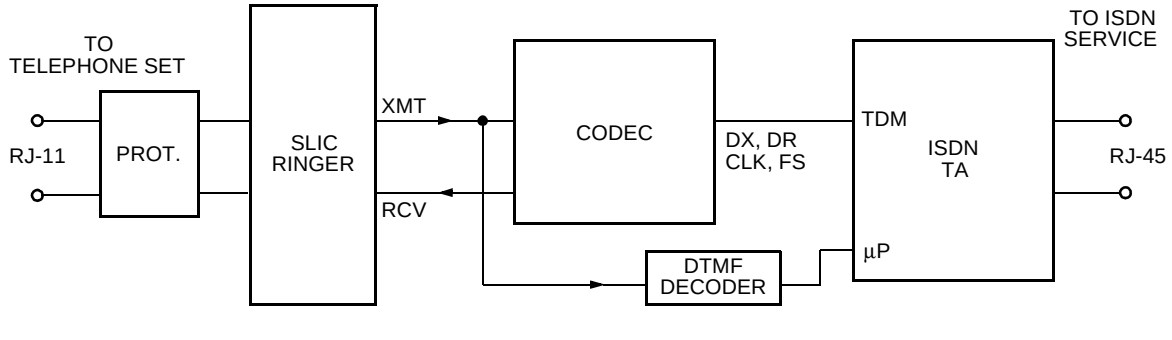


Figure 28. POTS Controlled from an ISDN Terminal Adapter

Power Ringing Load

Bellcore TA-909 specifies that a minimum 40 Vrms must be delivered to a 5 REN ringing load of 1380 Ω + 40 µF. During the ringing state, V_{BAT1} is automatically applied to the tip/ring power amplifiers. For 5 REN load, it is recommended that V_{BAT1} be set to –65 Vdc. Also during the power ring state, the dc current limit is automatically boosted by a factor of 2.8 over the current limit set by resistor R_{PROG}. Both of these factors are necessary to ensure delivery of 40 Vrms to the North American 5 REN ringing load of 1380 Ω + 40 µF.

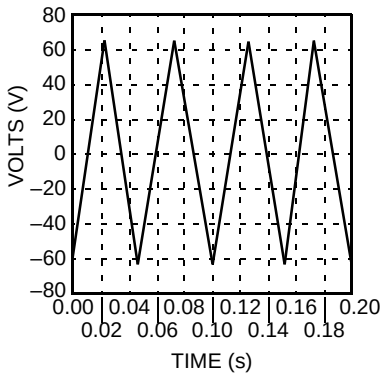
Crest Factor

The balanced trapezoidal ring signal is generated by simply toggling the SLIC between the powerup state forward and powerup reverse battery states. The state change is done by applying a square wave (whose frequency is the desired ring frequency) to logic input B1. Capacitors FB1 and FB2 are used to control or ramp the speed of the transition of the battery reverse, thus shaping the balanced ring signal. Waveforms of crest factors 1.6 and 1.2 are shown in Figure 29 and Figure 30.

In a real application, the ringing trapezoidal waveform crest factor can be estimated by:

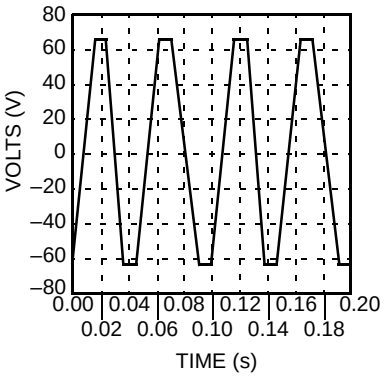
$$\text{Crest factor} = \frac{1}{\sqrt{1 - \frac{4 \times f \times C_{FB} \times (|V_{BAT}| - V_{OH})}{3 \times I_{CS}}}}$$

Where: f = ringing frequency; $C_{FB} = (C_{FB1} + C_{FB2})/2$; I_{CS} = 29 µA @ ±8% accuracy over temperature; V_{OH} = SLIC overhead during ring.



Note: Slew rate = 5.65 V/ms; trise = tfall = 23 ms; pwidth = 2 ms; period = 50 ms.

Figure 29. Ringing Waveform Crest Factor = 1.6



Note: Slew rate = 10.83 V/ms; trise = tfall = 12 ms; pwidth = 13 ms; period = 50 ms.

Figure 30. Ringing Waveform Crest Factor = 1.2

Applications (continued)

Power Ringing (continued)

Current-Limit Switch

During nonringing modes, the internal current source is set at 75 µA. During the ring mode, the current limit is automatically increased by a factor of 2.8. This is done to provide sufficient ring to a true North American 5 REN load. This is done internally by increasing the value of I_{PROG} from 75 µA to 210 µA, thus:

$I_{PROG} \bullet R_{PROG} = I_{LIM} \bullet B_{DCOUT}$
$R_{PROG} = I_{LIM} \bullet B_{DCOUT}/I_{PROG}$
$R_{PROG}(K) = I_{LIM}$ (mA) • 0.04167 (V/mA)/210e–3 (mA)
$R_{PROG}(K) = 0.198 \bullet I_{LIM}$ (mA)

In the current-limit region, the dc template has a high resistance (12.5 kΩ).

Ring Trip

Ring trip is accomplished by filtering the voltage seen at node DCOUT and applying it to the integrated ring trip comparator. DCOUT is a voltage proportional to the tip/ring current, and under short dc loop conditions, on-hook ringing current and off-hook current provide sufficient voltage differential at DCOUT to distinguish that a ring trip condition has occurred. The ring trip comparator threshold is set via a resistor between the ring trip comparator and ground.

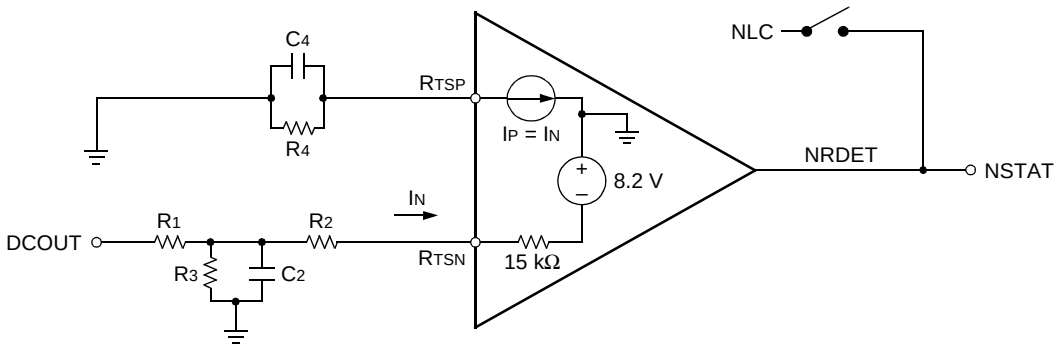
Output NSTAT is automatically set to detect ring trip during the balanced ring mode. During quiet intervals of ringing, output NSTAT is automatically determined by the loop closure detector.

The equivalent ring trip circuit for the balanced ringing SLIC application is shown in Figure 31.

The equations governing ring trip are derived below.

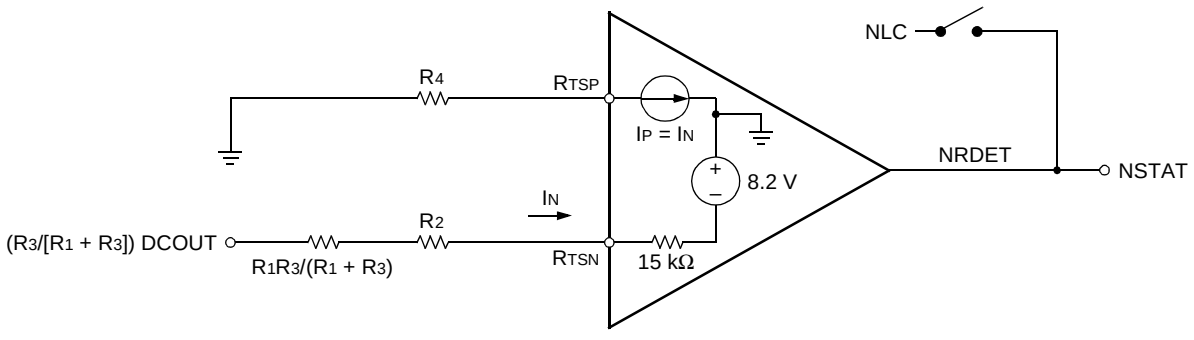
Capacitors C_2 and C_4, in conjunction with resistors R_2 and R_4, form a double-pole, low-pass filter that smooths the voltage seen at DCOUT. The poles of the filters are determined by C_2 and C_4. Where these poles are set will influence both the ripple seen at DCOUT and the speed of the transition of the voltage at DCOUT from the pretrip to the tripped level. For the derivation of the ring trip threshold equations, capacitors C_2 and C_4 can be ignored.

Redrawing the circuit, ignoring the capacitors, and taking the Thevenin equivalent circuit of the network at RTSN gives the results shown below in Figure 32.



12-3349.b (F)

Figure 31. Equivalent Ring Trip Circuit for Balanced Ringing SLIC



12-3348.b (F)

Figure 32. Thevenin Equivalent Ring Trip Circuit for Balanced Ringing SLIC

Applications (continued)

Power Ringing (continued)

$$I_{RTSN} = \frac{\left(\frac{R3}{R3 + R1} V_{DCOUT}\right) - (-8.2\ V)}{\frac{R1R3}{R1 + R3} + R2 + 15\ k\Omega}$$

At the trip point, the internal current repeater will force I_{RTSP} to be equal to I_{RTSN} and V_{RTSP} will be equal to V_{RTSN}, which is –8.2 V. Thus, at the trip point:

$$I_{RTSN} = I_{RTSP} = \frac{0 - (-8.2)}{R4}$$

Thus:

$$\frac{\left(\frac{R3}{R3 + R1}\right) V_{DCOUT} + 8.2\ V}{\frac{R1R3}{R1 + R3} + R2 + 15\ k\Omega} = \frac{8.2\ V}{R4}$$

Solving for V_{DCOUT}, the voltage at DCOUT at the ring trip point is given by:

$$V_{DCOUT\ (TRIP)} = 8.2(R3 + R1)\left[\frac{R1}{R1R4 + R3R4} + \frac{R2}{R3R4} + \frac{15\ k\Omega}{R3R4} - \frac{1}{R3}\right]$$

The loop current at ring trip is given by:

$$I_{LOOP(TRIP)} = (V_{DCOUT})/(\beta_{DCOUT})$$

For the L8560, the gain (β) at pin DCOUT is 41.67 V/A.

Capacitors C_2 and C_4, along with resistors R_2 and R_4, respectively, form low-pass filters to filter the ac voltage seen at DCOUT before it is applied to the ring trip comparator input. The lower the pole of the filter, the less the ripple, but also the slower the state transition at NSTAT. Poles in the neighborhood of 2.5 Hz—3 Hz are suggested, as given by:

$$f_{LP} = \frac{1}{2\pi R_2 C_2}$$

$$f_{LP} = \frac{1}{2\pi R_4 C_4}$$

In the reference designs discussed in the next section, the ring trip threshold is set for 50 mA with:

R_1 = 210 kΩ
R_2 = 124 kΩ
C_2 = 0.1 μF
R_3 = 562 kΩ
R_4 = 351 kΩ
C_4 = 0.1 μF

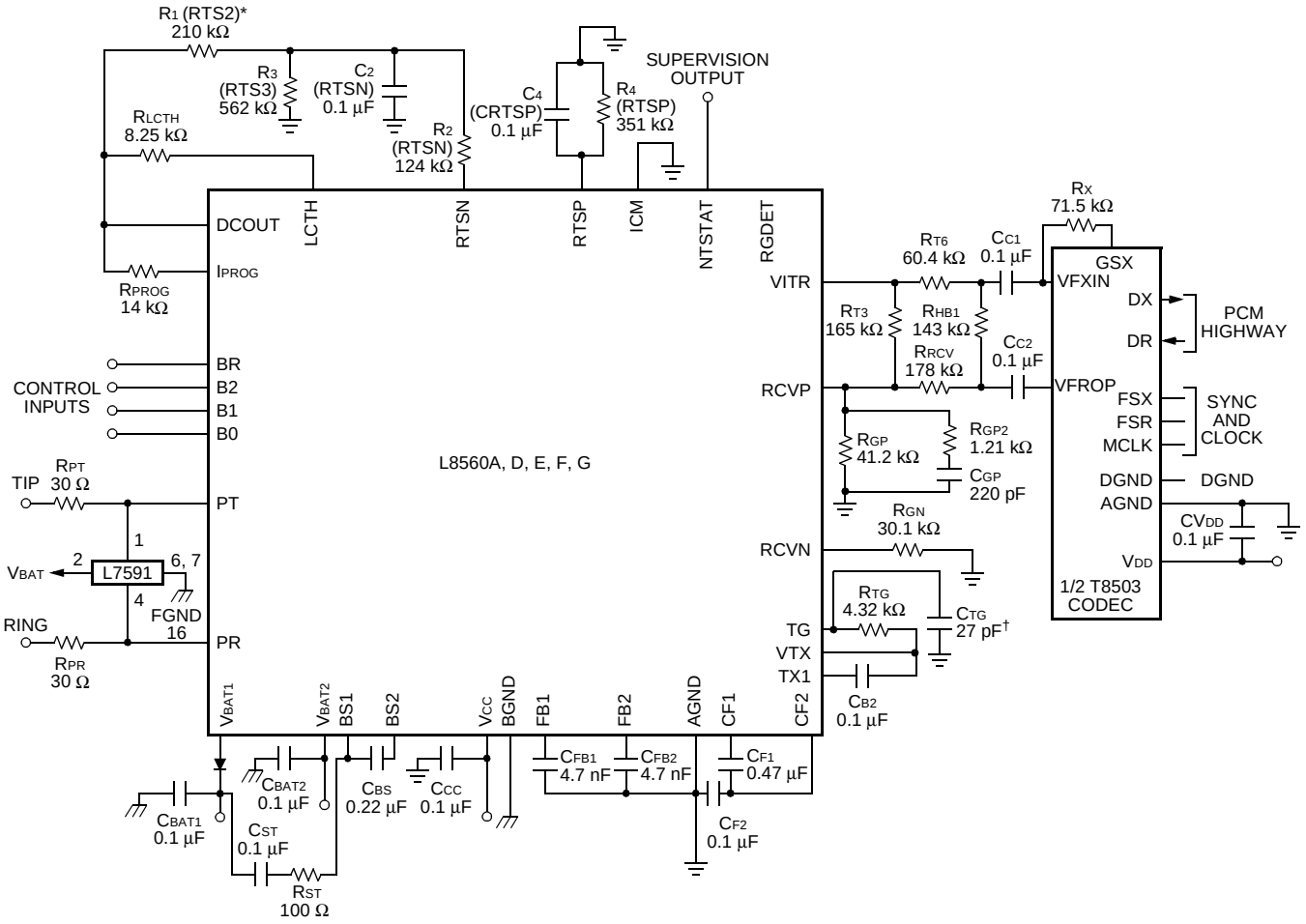
Except for L8560CAU, the internal voltage for L8560CAU is –5.7 V. 133 kΩ should be used for R_1.

Applications (continued)

Power Ringing (continued)

Reference Designs for ISDN TA Applications

A POTS circuit for reference design is shown in Figure 33. In Figure 33, the L8560 SLIC and T8503 codec are used. The ac circuit is designed per Bellcore TA-909 with a 600 Ω resistive termination and hybrid circuit, with the transmit gain set for –2 dB and the receive gain set for –4 dB. The T8503 codec is compatible with the T7237 U-interface transceiver and the T7256 SCNT1 interface.



12-3345.R (F)

* R1 = 133 kΩ for L8560C.
† Required only for L8560A/C versions.

Notes:
TX = –2 dB.
RX = –4 dB.
Termination = 600 Ω.
Hybrid balance = 600 Ω.

Figure 33. POTS Interface with Balanced Ringing Using L8560 SLIC and T8503 Codec

Applications (continued)

Power Ringing (continued)

Table 11. Parts List for Balanced Ringing Using T8503 Codec

Name	Value	Function
Integrated Circuits		
SLIC	L8560	Subscriber line interface circuit (SLIC).
Protector	L7591	Secondary protection.
Codec	T8503	First-generation codec.
Fault Protection		
R_{PT}	30 Ω fusible	Overcurrent protection.
R_{PR}	30 Ω fusible	Overcurrent protection.
Power Supply		
C_{BAT1}	0.1 µF, 20%, 100 V	V_{BAT} filter capacitor.
C_{BAT2}	0.1 µF, 20%, 100 V	V_{BAT} filter capacitor.
C_{CC}	0.1 µF, 20%, 10 V	V_{CC} filter capacitor.
C_{F1}	0.47 µF, 20%, 100 V	With C_{F2}, improves idle-channel noise.
C_{F2}	0.1 µF, 20%, 100 V	With C_{F1}, improves idle-channel noise.
C_{BS}	0.22 µF, 20%, 100 V	Slows battery switch transition.
C_{ST}	0.1 µF, 20%, 10 V	Loop stability.
R_{ST}	100 Ω, 1%, 1/8 W	Loop stability.
dc Profile/Ringing		
C_{FB1}	4.7 nF, 20%, 100 V	With C_{FB2}, slows rate of forward/reverse battery transition. Sets crest factor of balanced power ring signal.
C_{FB2}	4.7 nF, 20%, 100 V	With C_{FB1}, slows rate of forward/reverse battery transition. Sets crest factor of balanced power ring signal.
R_{PROG}	14 kΩ, 1%, 1/8 W	Sets dc loop current.
ac Characteristics		
R_{TG}	4.32 kΩ, 1%, 1/8 W	Sets internal transmit path gain to 19.2.
C_{B2}	0.1 µF, 20%, 10 V	ac/dc separation capacitor.
C_{C1}	0.1 µF, 20%, 10 V	dc blocking capacitor.
C_{C2}	0.1 µF, 20%, 10 V	dc blocking capacitor.
R_{T3}	165 kΩ, 1%, 1/8 W	With R_{GP} and R_{RCV}, sets ac termination impedance.
R_{RCV}	178 kΩ, 1%, 1/8 W	With R_{GP} and R_{T3}, sets receive gain.
R_{GP}	41.2 kΩ, 1%, 1/8 W	With R_{T3} and R_{RCV}, sets ac termination impedance and receive gain.
C_{GP}	220 pF, 20%, 10 V	Loop stability.
C_{TG}*	27 pF, 20%, 10 V	Loop stability.
R_{GP2}	1.21 kΩ, 1%, 1/8 W	Loop stability.
R_{GN}	30.1 kΩ, 1%, 1/8 W	Compensates for input bias offset at RCVN/RCVP.
R_{T6}	60.4 kΩ, 1%, 1/8 W	With R_X, sets transmit gain in codec.
R_X	71.5 kΩ, 1%, 1/8 W	With R_{T6}, sets transmit gain in codec.
R_{HB1}	143 kΩ, 1%, 1/8 W	Sets hybrid balance.
Supervision		
R_{LCTH}	8.25 kΩ, 1%, 1/8 W	Sets loop closure (off-hook) threshold.
R_1 (RTS2)†	210 kΩ, 1%, 1/8 W	With R_2, R_3, and R_4, sets ring trip threshold.
R_2 (RTSN)	124 kΩ, 1%, 1/8 W	With R_1, R_3, and R_4, sets ring trip threshold.
C_2 (CRTSN)	0.1 µF, 20%, 50 V	With R_2, sets pole of low-pass ring trip sense filter.
R_3 (RTS3)	562 kΩ, 1%, 1/8 W	With R_1, R_2, and R_4, sets ring trip threshold.
R_4 (RTSP)	351 kΩ, 1%, 1/8 W	With R_1, R_2, and R_3, sets ring trip threshold.
C_4 (CRTSP)	0.1 µF, 20%, 10 V	With R_4, sets pole of low-pass ring trip sense filter.

* Required for L8560A/L8560C version only.
† Use 133 kΩ for L8560C.

Applications (continued)

Design Considerations

Unbalanced Bused Ring Signal Application

The L8560 SLIC can also be used in the standard battery-backed, unbalanced ringing application. In this case, the ring signal is generated by a central ring generator and is bused to individual tip/ring pairs. A ringing relay is used during ringing to disconnect the SLIC from, and apply the ring generator to, the tip and ring pair.

Ring Trip Detection

The ring trip circuit is a comparator that has a special input section optimized for this application. The equivalent circuit is shown in Figure 34, along with its use in an application using unbalanced, battery-backed ringing.

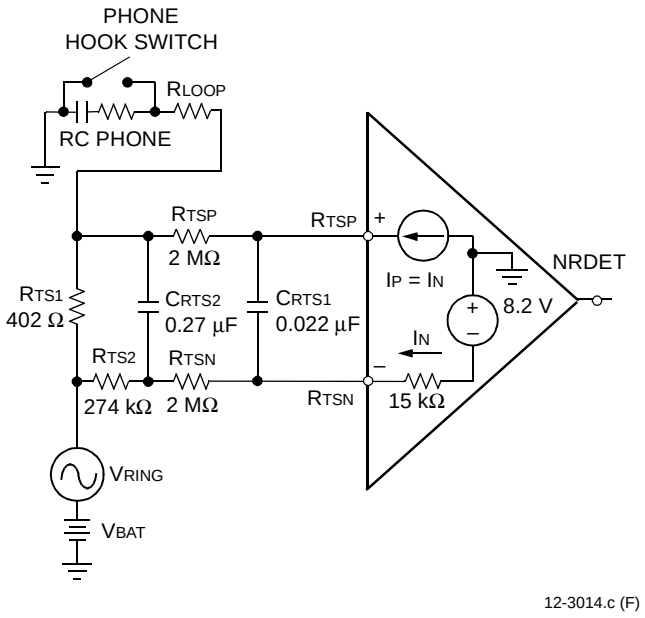


Figure 34. Ring Trip Equivalent Circuit and Equivalent Application

The comparator input voltage compliance is V_{CC} to V_{BAT}, and the maximum current is 240 µA in either direction. Its application is straightforward. A resistance (R_{TSN} + R_{TS2}) in series with the R_{TSN} input establishes a current that is repeated in the R_{TSP} input. A slightly lower resistance (R_{TSP}) is placed in series with the R_{TSP} input. When ringing is being injected, no dc current flows through R_{TS1}, so the R_{TSP} input is at a lower potential than R_{TSN}. When enough dc loop current flows, the R_{TSP} input voltage increases to trip the comparator. In Figure 34, a low-pass filter with a double pole at 2 Hz was implemented to prevent false ring trip.

The following example illustrates how the detection circuit in Figure 34 will trip at a 12.5 mA dc loop current using a –48 V battery.

$$I_N = \frac{-8.2\ V - (-48)}{2.289\ M\Omega}$$

$$= 17.4\ \mu A$$

The current I_N is repeated as I_P in the positive comparator input. The voltage at comparator input R_{TSP} is:

$$V_{RTSP} = V_{BAT} + I_{LOOP(dc)} \times R_{TS1} + I_P \times R_{TSP}$$

Using this equation and the values in the example, the voltage at input R_{TSP} is –13.2 V during ringing injection ($I_{LOOP(dc)}$ = 0). Input R_{TSP} is therefore at a level of 5 V below R_{TSN}. When enough dc loop current flows through R_{TS1} to raise its dc drop to 5 V, the comparator will trip.

In this example:

$$I_{LOOP(dc)} = \frac{5\ V}{402\ \Omega}$$

$$= 12.5\ mA$$

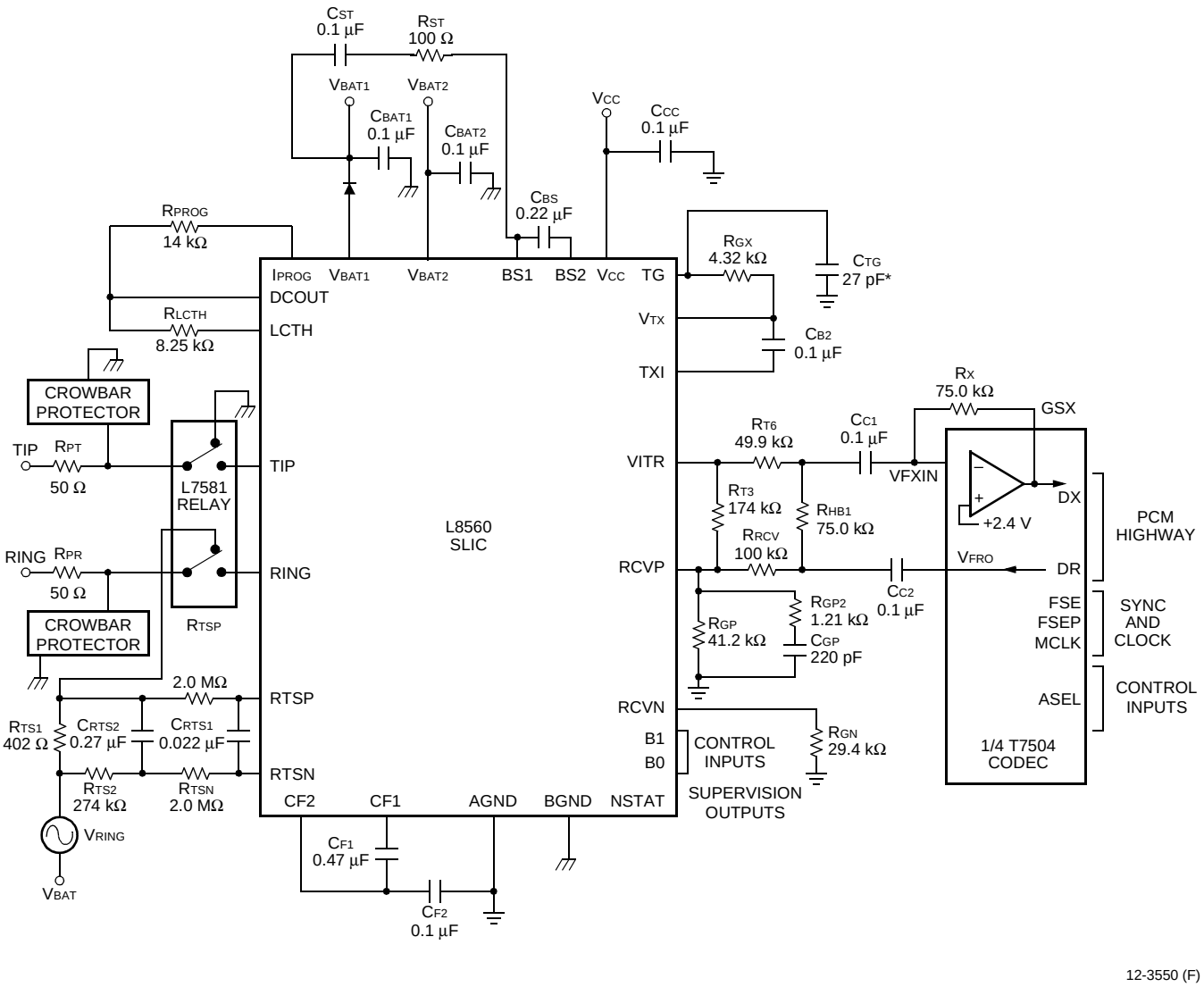
Except for L8560CAU, the internal voltage for L8560CAU is –5.7 V.

Note that during ringing in this mode of operation, both the NLC and NRDET circuits are active. During the actual ringing, NRDET is connected and NLC is isolated from tip and ring by the ring relay; thus, NSTAT reflects the status at NRDET. During quiet intervals of ringing, NLC is connected and NRDET is isolated from tip and ring by the ring relay; thus, NSTAT reflects the status at NLC. Thus, during ring cadence, the logic input that drives the ring relay can be used as an indication as to whether NRDET or NLC appears at output NSTAT.

A basic loop start reference circuit, using bused ringing with the L8560 SLIC and T7504 first-generation codec, is shown in Figure 35. This circuit is designed for a 600 Ω resistive termination impedance and hybrid balance. Transmit and receive gains are both set at 0 dB.

Applications (continued)

Design Considerations (continued)



12-3550 (F)

* Required for L8560A/L8560C version only.

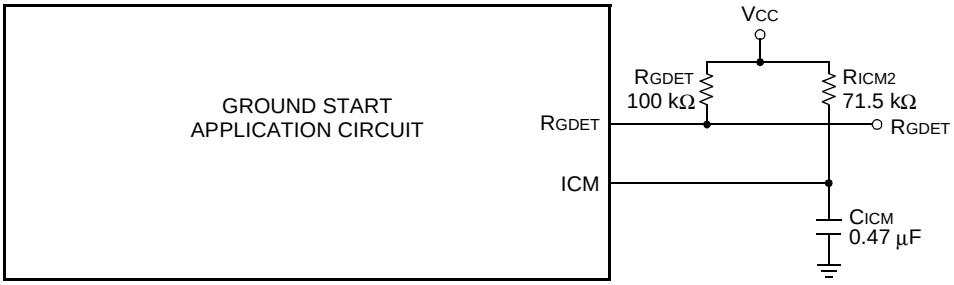
Notes:
Tx = 0 dB.
Rx = 0 dB.
Termination = 600 Ω.
Hybrid balance = 600 Ω.

Figure 35. Basic Loop Start Application Circuit Using T7504 Codec and Bused Ringing

Applications (continued)

Design Considerations (continued)

Figure 36 shows the ground start application.



12-3547.a.c (F)

Figure 36. Ground Start Application Circuit

Table 12. Parts List for Loop Start with Bused Ringing and Ground Start Applications

Name	Value	Function
Integrated Circuits		
SLIC	—	Subscriber line interface circuit (SLIC).
Protector	Crowbar protector*	Secondary protection.
Ringing Relay	L7581	Switches ringing signals.
Codec	T7504	First-generation codec.
Fault Protection		
R_{PT}	50 Ω PTC or fusible	Protection resistor.
R_{PR}	50 Ω PTC or fusible	Protection resistor.
Power Supply		
C_{BAT1}	0.1 µF, 20%, 100 V	V_{BAT} filter capacitor.
C_{BAT2}	0.1 µF, 20%, 100 V	V_{BAT} filter capacitor.
C_{CC}	0.1 µF, 20%, 10 V	V_{CC} filter.
C_{F1}	0.47 µF, 20%, 100 V	With C_{F2}, improves idle-channel noise.
C_{F2}	0.1 µF, 20%, 100 V	With C_{F1}, improves idle-channel noise.
C_{BS}	0.22 µF, 20%, 100 V	Slows battery switch transition.
C_{ST}	0.1 µF, 20%, 10 V	Loop stability.
R_{ST}	100 Ω, 1%, 1/8 W	Loop stability.
C_{TG}†	27 pF, 20%, 10 V	Loop stability.
dc Profile		
R_{PROG}	14 kΩ, 1%, 1/8 W	Sets dc loop current.

* Contact your Lucent Technologies account representative for protector recommendations. Choice of this (and all) component(s) should be evaluated and confirmed by the customer prior to use in any field or laboratory system. Lucent does not recommend use of this part in the field without performance verification by the customer. This device is suggested by Lucent for customer evaluation. The decision to use a component should be based solely on customer evaluation.
† Required for L8560A/L8560C version only.

Applications (continued)

Design Considerations (continued)

Table 12. Parts List for Loop Start with Bused Ringing and Ground Start Applications (continued)

Name	Value	Function
ac Characteristics		
R_{GX}	4.32 kΩ, 1%, 1/8 W	Sets internal transmit path gain of 9.6.
C_{B2}	0.1 μF, 20%, 10 V	ac/dc separation capacitor.
R_{T3}	174 kΩ, 1%, 1/8 W	With R_{GP} and R_{RCV}, sets ac termination impedance.
R_{RCV}	100 kΩ, 1%, 1/8 W	With R_{GP} and R_{T3}, sets receive gain.
R_{GP}	41.2 kΩ, 1%, 1/8 W	With R_{T3} and R_{RCV}, sets ac termination impedance and receive gain.
C_{GP}	220 pF, 20%, 10 V	Loop stability.
R_{GP2}	1.21 kΩ, 1%, 1/8 W	Loop stability.
R_{GN}	29.4 kΩ, 1%, 1/8 W	Compensates for input bias offset at RCVN/RCVP.
C_{C1}	0.1 μF, 20%, 10 V	dc blocking capacitor.
C_{C2}	0.1 μF, 20%, 10 V	dc blocking capacitor.
R_{T6}	49.9 kΩ, 1%, 1/8 W	With R_X, sets transmit gain in codec.
R_X	75.0 kΩ, 1%, 1/8 W	With R_{T6}, sets transmit gain in codec.
R_{HB1}	75.0 kΩ, 1%, 1/8 W	Sets hybrid balance.
Supervision		
R_{LCTH}	8.25 kΩ, 1%, 1/8 W	Sets loop closure (off-hook) threshold.
R_{TS1}	402 Ω, 5%, 2 W	Ringing source series resistor.
R_{TS2}	274 kΩ, 1%, 1/8 W	With C_{RTS2}, forms first pole of a double pole, 2 Hz ring trip sense filter.
C_{RTS1}	0.022 μF, 20%, 5 V	With R_{TSN} and R_{TSP}, forms second 2 Hz filter pole.
C_{RTS2}	0.27 μF, 20%, 100 V	With R_{TS2}, forms first 2 Hz filter pole.
R_{TSN}	2 MΩ, 1%, 1/8 W	With C_{RTS1} and R_{TSP}, forms second 2 Hz filter pole.
R_{TSP}	2 MΩ, 1%, 1/8 W	With C_{RTS1} and R_{TSN}, forms second 2 Hz filter pole.
Ground Start		
C_{ICM}	0.47 μF, 20%, 10 V	Provides 60 Hz filtering for ring ground detection.
R_{GDET}	100 kΩ, 20%, 1/8 W	Digital output pull-up resistor.
R_{ICM2}	71.5 kΩ, 1%, 1/8 W	Sets ring ground detection threshold.

Applications (continued)

Design Considerations (continued)

Table 13 shows the design parameters of the application circuit shown in Figure 35. Components that are adjusted to program these values are also shown.

Table 13. 600 Ω Design Parameters

Design Parameter	Parameter Value	Components Adjusted
Loop Closure Threshold	10 mA	R_{LCTH}
dc Loop Current Limit	25 mA	R_{PROG}
dc Feed Resistance	55 Ω	—
2-wire Signal Overload Level	3.14 dBm	—
ac Termination Impedance	600 Ω	R_{T3}, R_{GP}, R_{RCV}
Hybrid Balance Line Impedance	600 Ω	R_{HB1}
Transmit Gain	0 dB	R_{T6}, R_X
Receive Gain	0 dB	R_{RCV}, R_{GP}, R_{T3}

ac Design

There are four key ac design parameters. **Termination impedance** is the impedance looking into the 2-wire port of the line card. It is set to match the impedance of the telephone loop in order to minimize echo return to the telephone set. **Transmit gain** is measured from the 2-wire port to the PCM highway, while **receive gain** is done from the PCM highway to the transmit port. Finally, the **hybrid balance** network cancels the unwanted amount of the receive signal that appears at the transmit port.

At this point in the design, the codec needs to be selected. The discrete network between the SLIC and the codec can then be designed. Below is a brief codec feature and selection summary.

First-Generation Codecs

These perform the basic filtering, A/D (transmit), D/A (receive), and μ-law/A-law companding. They all have an op amp in front of the A/D converter for transmit gain setting and hybrid balance (cancellation at the summing node). Depending on the type, some have differential analog input stages, differential analog output stages, and μ-law/A-law selectability. This generation of codec has the lowest cost. It is most suitable for applications with fixed gains, termination impedance, and hybrid balance.

Second-Generation Codecs

This class of devices includes a microprocessor interface for software control of the gains and hybrid balance. The hybrid balance is included in the device. ac programmability adds application flexibility and saves several passive components. It also adds several I/O latches that are needed in the application. It does not have the transmit op amp, since the transmit gain and hybrid balance are set internally.

Third-Generation Codecs

This class of devices includes the gains, termination impedance, and hybrid balance—all under microprocessor control. Depending on the device, it may or may not include latches.

In the codec selection, increasing software control and flexibility are traded for device cost. To help decide, it may be useful to consider the following: Will the application require only one value for each gain and impedance? Will the board be used in different countries with different requirements? Will several versions of the board be built? If so, will one version of the board be most of the production volume? Does the application need only real termination impedance? Does the hybrid balance need to be adjusted in the field?

Applications (continued)

ac Design (continued)

ac equivalent circuits using a T7504 codec (V_{CC} only) are shown in Figures 37 and 38. Use the following two equations for Figure 37 below:

$R_{STP} = 1\ k\Omega \times \{[R_{GP}\ (k\Omega) \parallel R_{RCV}\ (k\Omega)]/24\ (k\Omega)\}$
$C_{STP} = 270\ pF/\{[R_{GP}\ (k\Omega) \parallel R_{RCV}\ (k\Omega)]/24\ (k\Omega)\}$

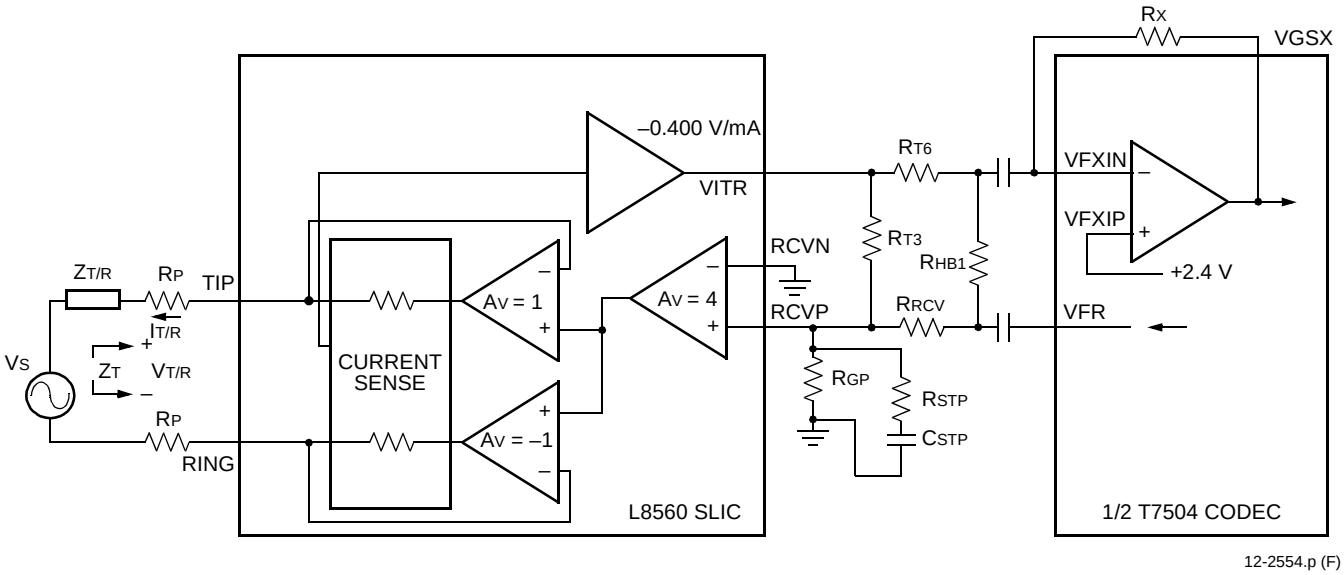


Figure 37. ac Equivalent Circuit Not Including Spare Op Amp

Use the following two equations for Figure 38 below:

$R_{STN} = 1\ k\Omega \times \{[R_{GN}\ (k\Omega) \parallel R_{RCV}\ (k\Omega)]/24\ (k\Omega)\}$
$C_{STN} = 270\ pF/\{[R_{GN}\ (k\Omega) \parallel R_{RCV}\ (k\Omega)]/24\ (k\Omega)\}$

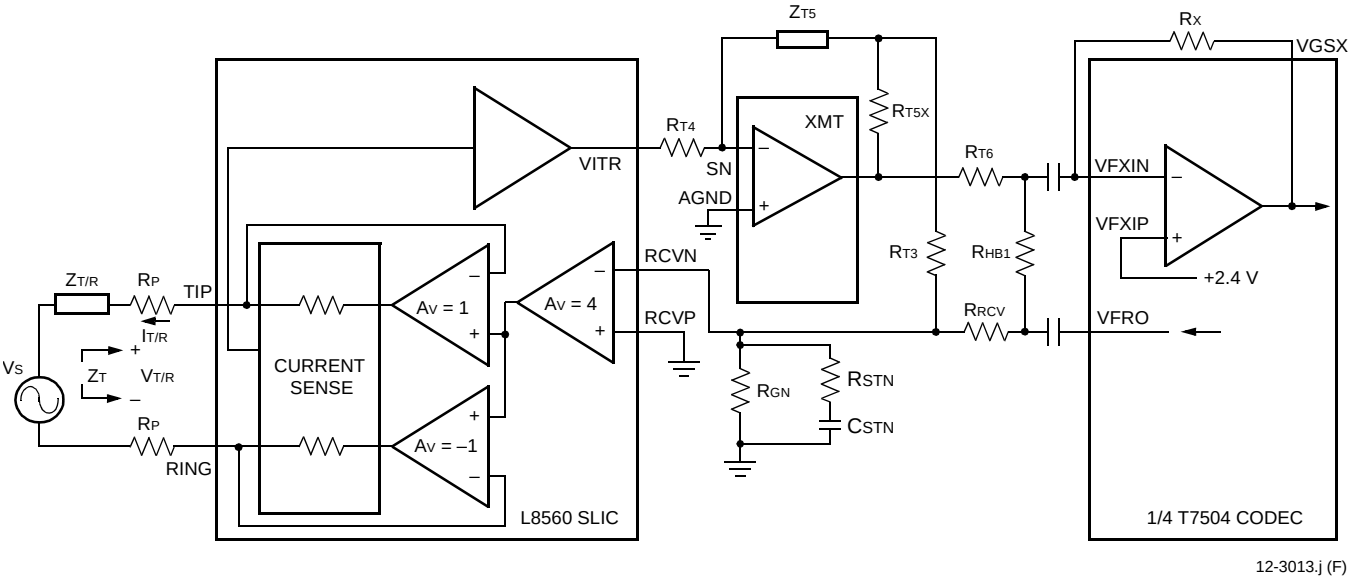


Figure 38. ac Equivalent Circuit Including Spare Op Amp

Applications (continued)

Design Examples

In the preceding examples, use of a first-generation codec is shown. The equations for second- and third-generation codecs are simply subsets of these. There are two examples below. The first shows the simplest circuit, which uses a minimum number of discrete components to synthesize a real termination impedance. The second example shows the use of the uncommitted op amp to synthesize a complex termination. The design has been automated in a DOS-based program, available on request.

Example 1, Real Termination

The following design equations refer to the circuit in Figure 37. Use these to synthesize real termination impedance.

Termination impedance:

$$z_T = \frac{V_{T/R}}{-I_{T/R}}$$

$$z_T = 2R_P + \frac{3200}{1 + \frac{R_{T3}}{R_{GP}} + \frac{R_{T3}}{R_{RCV}}}$$

Receive gain:

$$g_{rcv} = \frac{V_{T/R}}{V_{FR}}$$

$$g_{rcv} = \frac{8}{\left(1 + \frac{R_{RCV}}{R_{T3}} + \frac{R_{RCV}}{R_{GP}}\right)\left(1 + \frac{z_T}{Z_{T/R}}\right)}$$

Transmit gain:

$$g_{tx} = \frac{V_{GSX}}{V_{T/R}}$$

$$g_{tx} = \frac{-R_X}{R_{T6}} \times \frac{400}{Z_{T/R}}$$

Hybrid balance:

$$h_{bal} = 20\log\left(\frac{R_X}{R_{HB1}} - g_{tx} \times g_{rcv}\right)$$

$$h_{bal} = 20\log\left(\frac{V_{GSX}}{V_{FR}}\right)$$

To optimize the hybrid balance, the sum of the currents at the VFX input of the codec op amp should be set to 0. The expression for ZHB becomes:

$$R_{HB1}(k\Omega) = \frac{R_X}{g_{tx} \times g_{rcv}}$$

Example 2, Complex Termination

For complex termination, the spare op amp may be used (see Figure 38).

$$z_T = 2R_P + \frac{3200}{1 + \frac{R_{T3}}{R_{GN}} + \frac{R_{T3}}{R_{RCV}}}\left(\frac{Z_{T5}}{R_{T4}}\right)$$

$$= 2R_P + k(Z_{T5})$$

$$g_{rcv} = \frac{8}{\left(1 + \frac{R_{RCV}}{R_{T3}} + \frac{R_{RCV}}{R_{GN}}\right)\left(1 + \frac{z_T}{Z_{T/R}}\right)}$$

$$g_{tx} = \frac{R_X}{R_{T6}} \times \frac{400}{Z_{T/R}} \times \frac{Z_{T5}}{R_{T4}}\left(1 + \frac{R_{T5X}}{Z_{T5}} + \frac{R_{T5X}}{R_{T3} + R_{GN} \,||\, R_{RCV}}\right)$$

The hybrid balance equation is the same as in Example 1.

Example 3, Complex Termination Without Spare Op Amp

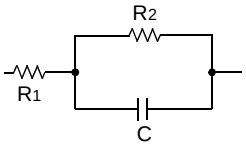
The gain shaping necessary for a complex termination impedance may be done without using the spare op amp by shaping across the Ax amplifier at nodes TG and VTX. This is a recommended approach.

Applications (continued)

Design Examples (continued)

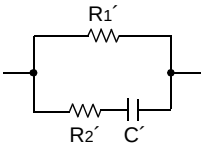
Complex Termination Impedance Design Example Using L8560 Without Spare Op Amp

Complex termination is specified in the form:



5-6396(F)

To work with this application, convert termination to the form:



5-6398(F)

where:

$R_1' = R_1 + R_2$

$R_2' = \frac{R_1}{R_2}(R_1 + R_2)$

$C' = \left(\frac{R_2}{R_1 + R_2}\right)^2 C$

ac Interface Using First-Generation Codec

$R_{TGP}/R_{TGS}/C_{GS}$ (Z_{TG}): These components give gain shaping to get good gain flatness. These components are a scaled version of the specified complex termination impedance.

Note for pure (600 Ω) resistive terminations, components R_{TGS} and C_{GS} are not used. Resistor R_{TGP} is used and is still 4.32 kΩ.

R_X/R_{T6}: With other components set, the transmit gain (for complex and resistive terminations) R_X and R_{T6} are varied to give specified transmit gain.

$R_{T3}/R_{RCV}/R_{GP}$: For both complex and resistive terminations, the ratio of these resistors set the receive gain. For resistive terminations, the ratio of these resistors set the return loss characteristic. For complex terminations, the ratio of these resistors set the low-frequency return loss characteristic.

$C_N/R_{N1}/R_{N2}$: For complex terminations, these components provide high-frequency compensation to the return loss characteristic.

For resistive terminations, these components are not used and R_{CVN} is connected to ground via a resistor.

R_{HB}: Sets hybrid balance for all terminations.

Set Z_{TG}—gain shaping:

$Z_{TG} = R_{TGP} \,||\, R_{TGS} + C_{GS}$ which is a scaled version of $Z_{T/R}$ (the specified termination resistance) in the $R_1' \,||\, R_2' + C'$ form.

R_{TGP} must be 4.32 kΩ to set SLIC transconductance to 400 V/A

$R_{TGP} = 4.32\ k\Omega$

At dc, C_{TGS} and C´ are open.

$R_{TGP} = M \times R1'$

where M is the scale factor.

$M = \frac{4320}{R_1'}$

It can be shown:

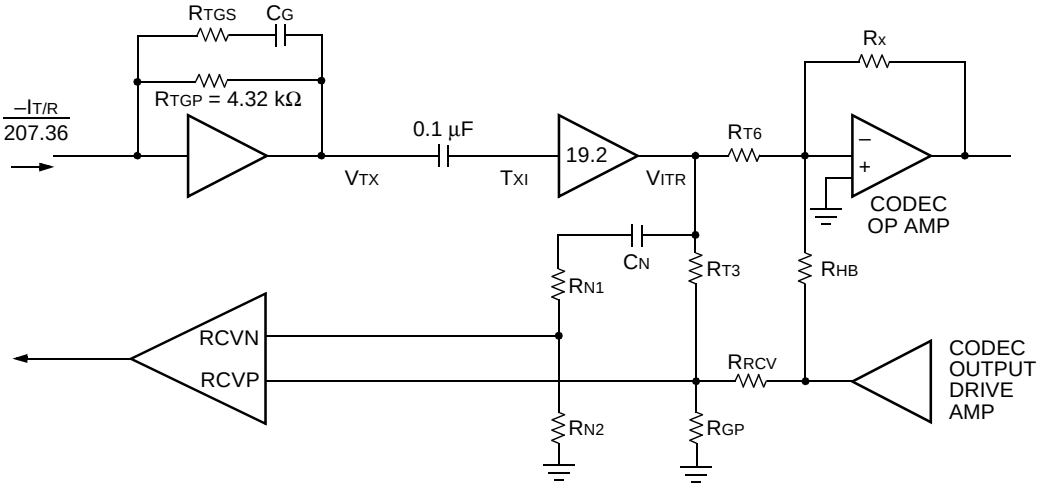
$R_{TGS} = M \times R2'$

and

$C_{TGS} = \frac{C'}{M}$

Applications (continued)

Design Examples (continued)



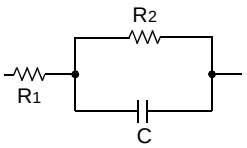
5-6400.b (F)

Figure 39. Interface Circuit Using First-Generation Codec (Blocking Capacitors Not Shown)

Transmit Gain

Transmit gain will be specified as a gain from T/R to PCM, T_X (dB). Since PCM is referenced to 600 Ω and assumed to be 0 dB, and in the case of T/R being referenced to some complex impedance other than 600 Ω resistive, the effects of the impedance transformation must be taken into account.

Again, specified complex termination impedance at T/R is of the form:



5-6396(F)

First, calculate the equivalent resistance of this network at the midband frequency of 1000 Hz.

$$R_{EQ} = \sqrt{\left(\frac{(2\pi f)^2 C_1^2 R_1 R_2^2 + R_1 + R_2}{1 + (2\pi f)^2 R_2^2 C_1^2}\right)^2 + \left(\frac{2\pi f R_2^2 C_1}{1 + (2\pi f)^2 R_2^2 C_1^2}\right)^2}$$

Using R_{EQ}, calculate the desired transmit gain, taking into account the impedance transformation:

$$T_X \text{ (dB)} = T_{X\,(\text{specified[dB]})} + 20 \log \sqrt{\frac{600}{R_{EQ}}}$$

$T_{X\,(\text{specified[dB]})}$ is the specified transmit gain. 600 Ω is the impedance at the PCM and R_{EQ} is the impedance at Tip and ring. $20 \log \sqrt{\frac{600}{R_{EQ}}}$ represents the power loss/gain due to the impedance transformation.

Note in the case of a 600 Ω pure resistive termination at T/R $20 \log \sqrt{\frac{600}{R_{EQ}}} = 20 \log \sqrt{\frac{600}{600}} = 0$.

Thus, there is no power loss/gain due to impedance transformation and T_X (dB) = $T_{X\,(\text{specified[dB]})}$.

Finally, convert T_X (dB) to a ratio, g_{TX}:

T_X (dB) = $20 \log g_{TX}$

The ratio of R_X/R_{T6} is used to set the transmit gain:

$$\frac{R_X}{R_{T6}} = g_{TX} \bullet \frac{207.36}{19.2} \bullet \frac{1}{M}$$

with a quad Lucent codec such as T7504:

$R_X < 200$ kΩ

Applications (continued)

Design Examples (continued)

Receive Gain

Ratios of R_{RCV}, R_{T3}, R_{GP} will set both the low-frequency termination and receive gain for the complex case. In the complex case, additional high-frequency compensation, via C_N, R_{N1}, and R_{N2}, is needed for the return loss characteristic. For resistive termination, C_N, R_{N1}, and R_{N2} are not used and R_{CVN} is tied to ground via a resistor.

Determine the receive gain, g_{RCV}, taking into account the impedance transformation in a manner similar to transmit gain.

$$R_X\ (dB) = R_{X\ (specified[dB])} + 20 \log \sqrt{\frac{R_{EQ}}{600}}$$

$$R_X\ (dB) = 20 \log g_{RCV}$$

Then:

$$g_{RCV} = \frac{4}{1 + \frac{R_{RCV}}{R_{T3}} + \frac{R_{RCV}}{R_{GP}}}$$

and low-frequency termination

$$Z_{TER(low)} = \frac{3200}{1 + \frac{R_{T3}}{R_{GP}} + \frac{R_{T3}}{R_{RCV}}} + 2R_P$$

$Z_{TER(low)}$ is the specified termination impedance assuming low frequency (C or C´ is open).

R_P is the series protection resistor.

These two equations are best solved using a computer spreadsheet.

Next, solve for the high-frequency return loss compensation circuit, C_N, R_{N1}, and R_{N2}:

$$C_N R_{N2} = \frac{2R_P}{3200}\ C_G\ R_{TGP}$$

$$R_{N1} = R_{N2} \left[\frac{3200}{2R_P} \left(\frac{R_{TGS}}{R_{TGP}} \right) - 1 \right]$$

There is an input offset voltage associated with nodes R_{CVN} and R_{CVP}. To minimize the effect of mismatch of this voltage at T/R, the equivalent resistance to ac ground at R_{CVN} should be approximately equal to that at R_{CVP}. Refer to Figure 40 on page 43 (with dc blocking capacitors). To meet this requirement, $R_{N2} = R_{GP} \parallel R_{T3}$.

Hybrid Balance

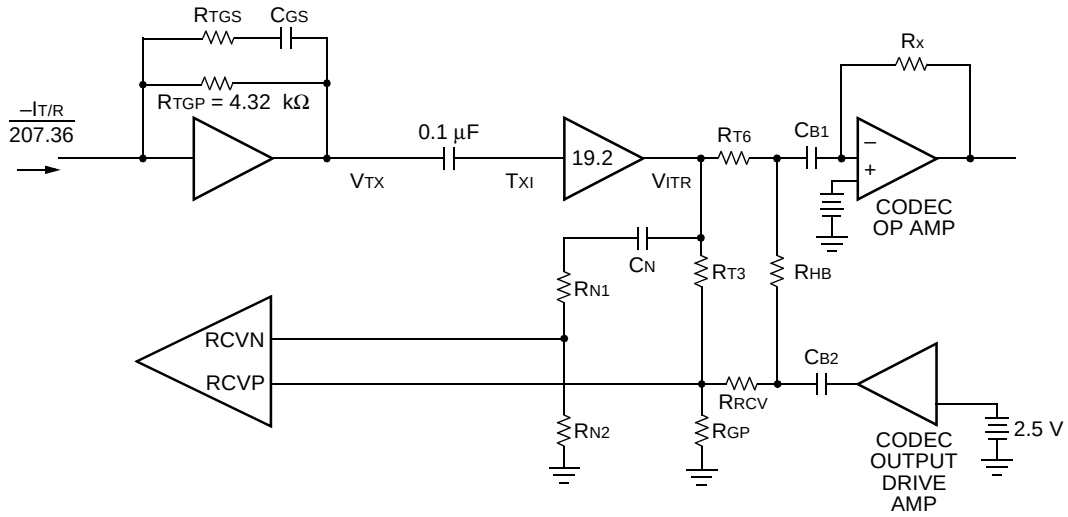
Set the hybrid cancellation via R_{HB}.

$$R_{HB} = \frac{R_X}{g_{RCV} \times g_{TX}}$$

Applications (continued)

Design Examples (continued)

Blocking Capacitors



5-6401b(F)

Figure 40. ac Interface Using First-Generation Codec (Including Blocking Capacitors) for Complex Termination Impedance

If a 5 V only codec such as the Lucent T7504 is used, dc blocking capacitors must be added as shown in Figure 40. This is because the codec is referenced to 2.5 V and the SLIC to ground—with the ac coupling, a dc bias at T/R is eliminated and power associated with this bias is not consumed.

Typically, values of 0.1 µF to 0.47 µF capacitors are used for dc blocking. The addition of blocking capacitors will cause a shift in the return loss and hybrid balance frequency response toward higher frequencies, degrading the lower-frequency response. The lower the value of the blocking capacitor, the more pronounced the effect is, but the cost of the capacitor is lower. It may be necessary to scale resistor values higher to compensate for the low-frequency response. This effect is best evaluated via simulation. A *PSPICE** model for the L8560 is available.

Design equation calculations seldom yield standard component values. Conversion from the calculated value to standard value may have an effect on the ac parameters. This effect should be evaluated and optimized via simulation.

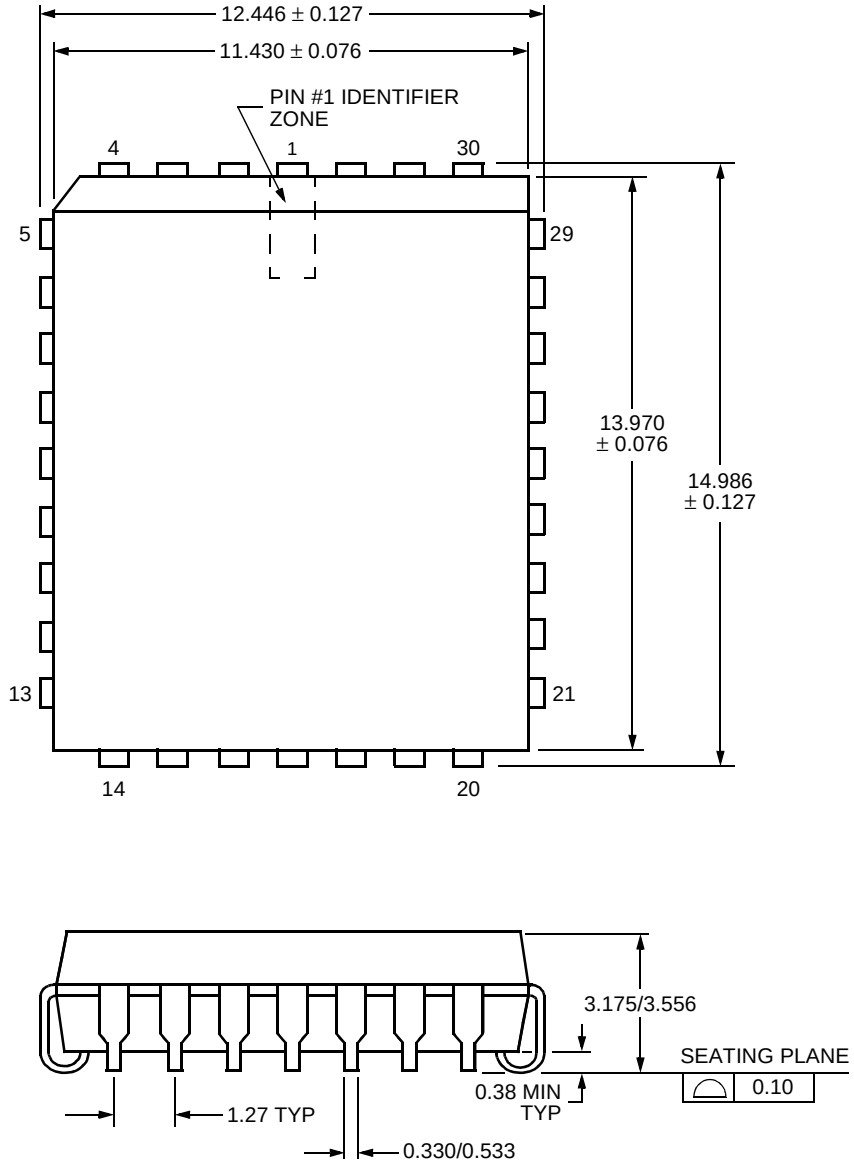
* *PSPICE* is a registered trademark of MicroSim Corporation.

Outline Diagrams

32-Pin PLCC

Dimensions are in millimeters.

Note: The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Lucent Technologies Sales Representative.



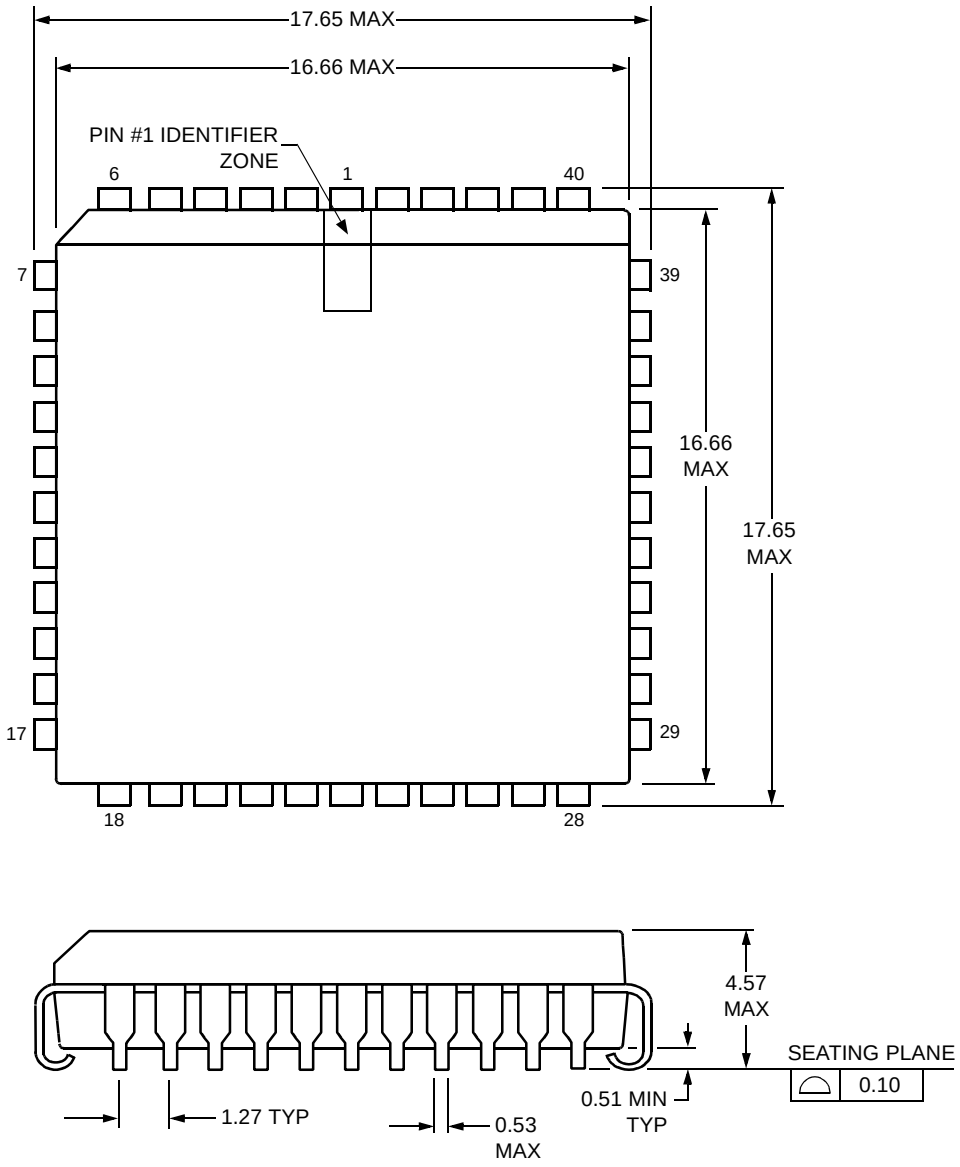
5-3813r2 (F)

Outline Diagrams (continued)

44-Pin PLCC

Dimensions are in millimeters.

Note: The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Lucent Technologies Sales Representative.



5-2506r.8(F)

Ordering Information

Device Code	Description	Package	Comcode
LUCL8560AAU-D	Low-power SLIC (Dry-bagged)	32-Pin PLCC	107957375
LUCL8560AAU-DT	Low-power SLIC (Tape and Reel, Dry-bagged)	32-Pin PLCC	107957383
LUCL8560AP-D	Low-power SLIC (Dry-bagged)	44-Pin PLCC	107891111
LUCL8560AP-DT	Low-power SLIC (Tape and Reel, Dry-bagged)	44-Pin PLCC	107891129
LUCL8560CAU-D	Low-power SLIC (Dry-bagged)	32-Pin PLCC	107953390
LUCL8560CAU-DT	Low-power SLIC (Tape and Reel, Dry-bagged)	32-Pin PLCC	107953408
LUCL8560DAU-D	Low-power SLIC (Dry-bagged)	32-Pin PLCC	108130576
LUCL8560DAU-DT	Low-power SLIC (Tape and Reel, Dry-bagged)	32-Pin PLCC	108130584
LUCL8560EP-D	Low-power SLIC (Dry-bagged)	44-Pin PLCC	108133000
LUCL8560EP-DT	Low-power SLIC (Tape and Reel, Dry-bagged)	44-Pin PLCC	108133018
LUCL8560FAU-D	Low-power SLIC (Dry-bagged)	32-Pin PLCC	108190885
LUCL8560FAU-DT	Low-power SLIC (Tape and Reel, Dry-bagged)	32-Pin PLCC	108190893
LUCL8560GP-D	Low-power SLIC (Dry-bagged)	44-Pin PLCC	108190935
LUCL8560GP-DT	Low-power SLIC (Tape and Reel, Dry-bagged)	44-Pin PLCC	108190943

For additional information, contact your Microelectronics Group Account Manager or the following:
INTERNET: **http://www.lucent.com/micro**
E-MAIL: **docmaster@micro.lucent.com**
N. AMERICA: Microelectronics Group, Lucent Technologies Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18103
1-800-372-2447, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106)
ASIA PACIFIC: Microelectronics Group, Lucent Technologies Singapore Pte. Ltd., 77 Science Park Drive, #03-18 Cintech III, Singapore 118256
Tel. (65) 778 8833, FAX (65) 777 7495
CHINA: Microelectronics Group, Lucent Technologies (China) Co., Ltd., A-F2, 23/F, Zao Fong Universe Building, 1800 Zhong Shan Xi Road, Shanghai 200233 P. R. China **Tel. (86) 21 6440 0468**, **ext. 316**, FAX (86) 21 6440 0652
JAPAN: Microelectronics Group, Lucent Technologies Japan Ltd., 7-18, Higashi-Gotanda 2-chome, Shinagawa-ku, Tokyo 141, Japan
Tel. (81) 3 5421 1600, FAX (81) 3 5421 1700
EUROPE: Data Requests: MICROELECTRONICS GROUP DATALINE: **Tel. (44) 7000 582 368**, FAX (44) 1189 328 148
Technical Inquiries: GERMANY: **(49) 89 95086 0** (Munich), UNITED KINGDOM: **(44) 1344 865 900** (Ascot),
FRANCE: **(33) 1 40 83 68 00** (Paris), SWEDEN: **(46) 8 594 607 00** (Stockholm), FINLAND: **(358) 9 4354 2800** (Helsinki),
ITALY: **(39) 02 6608131** (Milan), SPAIN: **(34) 1 807 1441** (Madrid)

April 2000
DS00-172ALC (Replaces DS99-124ALC)

microelectronics group

Lucent Technologies
Bell Labs Innovations