Shenzhen LIZE Electronic Technology Co., Ltd

SPECIFICATION

L93C56/66

Version 1.0

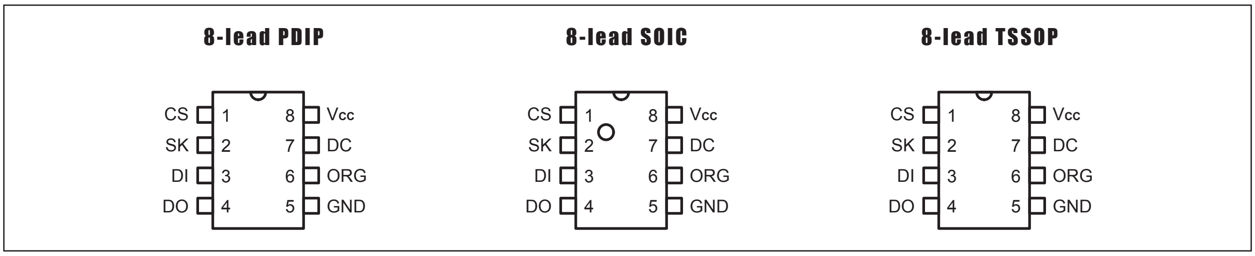
■ Features

- ➤Low-voltage Operation
  - - 1.8 (VCC = 1.8V to 5.5V)
- ➤Three-wire Serial Interface
- ➤Sequential Read Operation
- ➤2 MHz Clock Rate(5V) Compatibility
- ➤Self-timed Write Cycle (5 ms max)
- ➤High-reliability
  - - Endurance: 1 Million Write Cycles
  - - Data Retention: 100 Years
- ➤8-lead PDIP, 8-lead JEDEC SOIC and 8-lead TSSOP Packages

■ General Description

The L93C56/66 provides 2048/4096 bits of serial electrically erasable programmable read only memory (EEPROM) organized as 128/256 words of 16 bits each, when the ORG pin is connected to VCC and 256/512 words of 8 bits each when it is tied to ground. The L93C56/66 is available in space-saving 8-lead PDIP, 8-lead TSSOP and 8-lead JEDEC SOIC packages. The L93C56/66 is enabled through the Chip Select pin (CS), and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a Read instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The WRITE cycle is completely self-timed and no separate erase cycle is required before write. The Write cycle is only enabled when it is in the Erase/Write Enable state. When CS is brought "high" following the initiation of a write cycle, the DO pin outputs the Ready/Busy status.

■ Pin Configuration

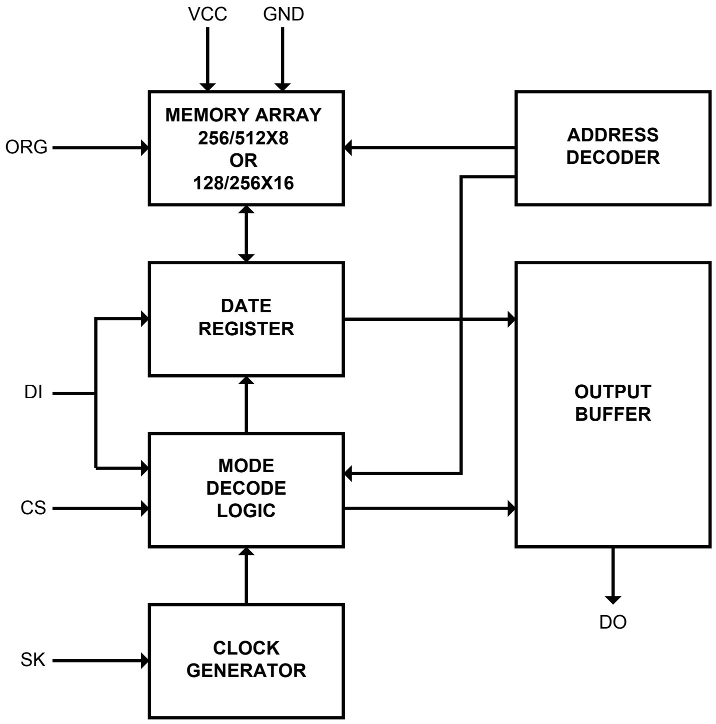


■ Pin Descriptions

➤Table 1: Pin Configuration

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply
ORG	Internal Organization
DC	Don't Connect

■ Figure 1: Block Diagram



Notes: When the ORG pin is connected to VCC, the “x 16” organization is selected. When it is connected to ground, the “x 8” organization is selected. If the ORG pin is left unconnected and the application does not load the input beyond the capability of the internal 1 Meg ohm pullup, then the “x 16” organization is selected.

Electrical Characteristics

➤Absolute Maximum Ratings*

DC Supply Voltage . . . .-0.3V to +6.5V

Input / Output Voltage . . . . GND-0.3V to Vcc+0.3V

Operating Ambient Temperature . . . . . -40°C to +85°C

Storage Temperature . . . . -65°C to +150°C

➤*NOTICE:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 2.Pin Capacitance (1)

➤Applicable over recommended operating range from TA = 25°C, f = 1.0 MHz, VCC = +1.8V (unless otherwise noted)

Symbol	Test Conditions	Max	Unit	Conditions
COUT	Output Capacitance (DO)	5	pF	VOUT = 0V
CIN	Input Capacitance (CS, SK, DI)	5	pF	VIN = 0V

Table 3 . DC Characteristics

➤Applicable over recommended operating range from: TA = −40°C to +85°C, VCC = +1.8V to +5.5V, (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage	-	1.8	-	5.5	V
V_{CC2}	Supply Voltage	-	2.7	-	5.5	V
V_{CC3}	Supply Voltage	-	4.5	-	5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0V Read at 1.0 MHz	-	0.2	2.0	mA
		Write at 1.0 MHz	-	0.9	3.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.8V CS = 0V	-	-	1.0	μA
I_{SB2}	Standby Current	V_{CC} = 2.7V CS = 0V	-	-	1.0	μA
I_{SB3}	Standby Current	V_{CC} = 5.0V CS = 0V	-	-	1.0	μA
$I_{IL(1)}$	Input Leakage	V_{IN} = 0V to V_{CC}	-	0.1	1.0	μA
$I_{IL(2)}$	Input Leakage	V_{IN} = 0V to V_{CC}	-	2.0	3.0	μA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}	-	0.1	1.0	μA
$V_{IL1(3)}$	Input Low Voltage	2.7V ≤ V_{CC} ≤ 5.5V	-0.3	-	0.8	
$V_{IH1(3)}$	Input High Voltage		2.0	-	V_{CC} + 0.3	V
$V_{IL2(3)}$	Input Low Voltage	1.8V ≤ V_{CC} ≤ 2.7V	-0.5	-	V_{CC} + 0.3	
$V_{IH2(3)}$	Input High Voltage		V_{CC} x 0.7	-	V_{CC} + 0.3	V
V_{OL1}	Output Low Voltage	2.7V ≤ V_{CC} ≤ 5.5V IOL = 2.1mA	-	-	0.4	V
V_{OH1}	Output High Voltage	IOH = -0.4mA	2.4	-		V
V_{OL2}	Output Low Voltage	1.8V ≤ V_{CC} ≤ 2.7V IOL = 0.15mA	-	-	0.2	V
V_{OH2}	Output High Voltage	IOH = -100μA	V_{CC}-0.2	-	-	V

Notes:
1. DI、CS、SK input pin
2. ORG input pin
3. VIL min and VIH max are reference only and are not tested.

■ Table 4. AC Characteristics

➤Applicable over recommended operating range from TA = −40°C to + 85°C, VCC = +1.8V to + 5.5V,
CL = 1 TTL Gate and 100pF (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
t_{SK}	SK Clock Frequency	4.5V ≤ VCC ≤ ≤5.5V		0	-	2	MHz
		2.7V ≤ VCC ≤ ≤5.5V		0		1	
		1.8V ≤ VCC ≤ 5.5V		0		0.25	
t_{SKH}	SK High Time	4.5V ≤ VCC ≤ ≤5.5V		250	-	-	ns
		2.7V ≤ VCC ≤ ≤5.5V		250			
		1.8V ≤ VCC ≤ 5.5V		1000			
t_{SKL}	SK Low Time	4.5V ≤ VCC ≤ ≤5.5V		250	-	-	ns
		2.7V ≤ VCC ≤ ≤5.5V		250			
		1.8V ≤ VCC ≤ 5.5V		1000			
t_{CS}	Minimum CS Low Time	4.5V ≤ VCC ≤ ≤5.5V		250	-	-	ns
		2.7V ≤ VCC ≤ ≤5.5V		250			
		1.8V ≤ VCC ≤ 5.5V		1000			
t_{CSS}	CS Setup Time	Relative to SK	4.5V ≤ VCC ≤ ≤5.5V	50	-	-	ns
			2.7V ≤ VCC ≤ ≤5.5V	50			
			1.8V ≤ VCC ≤ 5.5V	200			
t_{DIS}	DI Setup Time	Relative to SK	4.5V ≤ VCC ≤ ≤5.5V	100	-	-	ns
			2.7V ≤ VCC ≤ ≤5.5V	100			
			1.8V ≤ VCC ≤ 5.5V	400			
t_{CSH}	CS Hold Time	Relative to SK		0	-	-	ns
t_{DIH}	DI Hold Time	Relative to SK	4.5V ≤ VCC ≤ ≤5.5V	100	-	-	ns
			2.7V ≤ VCC ≤ ≤5.5V	100			
			1.8V ≤ VCC ≤ 5.5V	400			
t_{PD1}	Output Delay to “1”	AC Test	4.5V ≤ VCC ≤ ≤5.5V	-	-	250	ns
			2.7V ≤ VCC ≤ ≤5.5V			250	
			1.8V ≤ VCC ≤ 5.5V			1000	
t_{PD0}	Output Delay to “0”	AC Test	4.5V ≤ VCC ≤ ≤5.5V	-	-	250	ns
			2.7V ≤ VCC ≤ ≤5.5V			250	
			1.8V ≤ VCC ≤ 5.5V			1000	
t_{SV}	CS to Status Valid	AC Test	4.5V ≤ VCC ≤ ≤5.5V	-	-	250	ns
			2.7V ≤ VCC ≤ ≤5.5V			250	
			1.8V ≤ VCC ≤ 5.5V			1000	
t_{DF}	CS to DO in High Impedance	AC Test CS = VIL	4.5V ≤ VCC ≤ ≤5.5V	-	-	100	ns
			2.7V ≤ VCC ≤ ≤5.5V			100	
			1.8V ≤ VCC ≤ 5.5V			400	
t_{WP}	Write Cycle Time	-	-	-	1.5	5	ms
Endurance(1)	5.0V, 25°C	-		1M	-	-	Write Cycle

Notes: 1. This parameter is characterized and is not 100% tested.

Functional Description

The L93C56/66 is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. A valid instruction starts with a rising edge of CS and consists of a start bit (logic“1”) followed by the appropriate op code and the desired memory address location.

Table5.Instruction Set for the L93C56/66

Instruction	SB	OP Code	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A_8 - A_0	A_7 - A_0			Reads data stored in memory, at specified address
EWEN	1	00	11XXXXXXX	11XXXXXX			Write enable must precede all programming modes
ERASE	1	11	A_8 - A_0	A_7 - A_0			Erase memory location An - A0
WRITE	1	01	A_8 - A_0	A_7 - A_0	D_7 - D_0	D_{15} - D_0	Writes memory location An - A0
ERAL	1	00	10XXXXXXX	10XXXXXX			Erases all memory locations. Valid only at VCC = 4.5V to 5.5V
WRAL	1	00	01XXXXXXX	01XXXXXX	D_7 - D_0	D_{15} - D_0	Writes all memory locations. Valid only at VCC = 4.5V to 5.5V
EWDS	1	00	00XXXXXXX	00XXXXXX			Disables all programming instructions

Notes: The X’s in the address field represent don’t care values and must be clocked.

READ (READ): The Read (READ) instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that a dummy bit (logic “0”) precedes the 8- or 16-bit data output string.The K93C56/66 supports sequential read operations.The device will automatically increment the internal address pointer and clock out the next memory location as long as Chip Select (CS) is held high .In this case ,the dummy bit (logic “0”)will not be clocked out between memory locations,thus allowing for a continuous steam of data to be read.

ERASE/WRITE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable(EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the EWEN state, programming remains enabled until an EWDS instruction is executed or VCC power is removed from the part.

ERASE (ERASE): The Erase (ERASE) instruction programs all bits in the specified memory location to the logical “1” state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (TCS). A logic “1” at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

WRITE (WRITE): The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle, tWP, starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (TCS). A logic “0” at DO indicates that programming is still in progress. A logic “1” indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. A Ready/Busy status cannot be obtained if the CS is brought high after the end of the selftimed programming cycle, TWP.

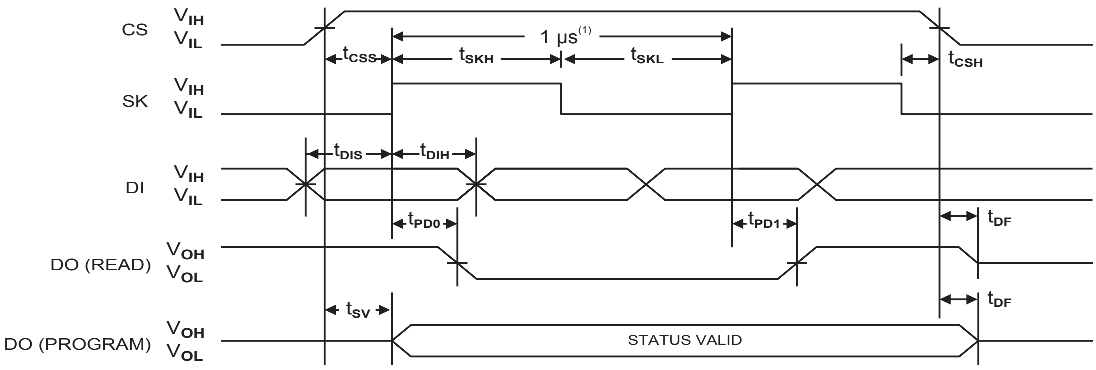
ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the logic “1” state and is primarily used for testing purposes. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (TCS). The ERAL instruction is valid only at VCC = 5.0V ± 10%.

WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (TCS). The WRAL instruction is valid only at VCC = 5.0V ± 10%.

ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the Read instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

■ Timing Diagrams

➤Figure 2: Synchronous Data Timing



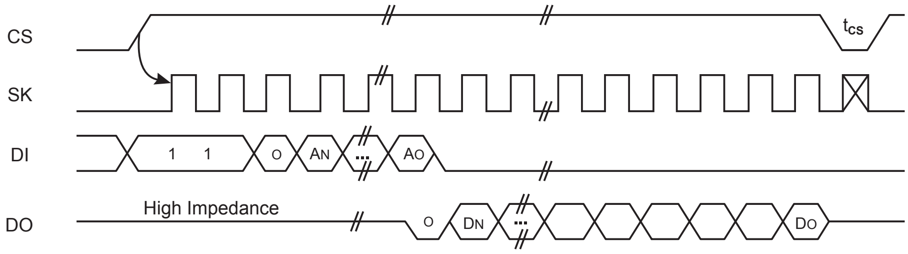
Note: 1. This is the minimum SK period.

■ Table 6. Organization Key for Timing Diagrams

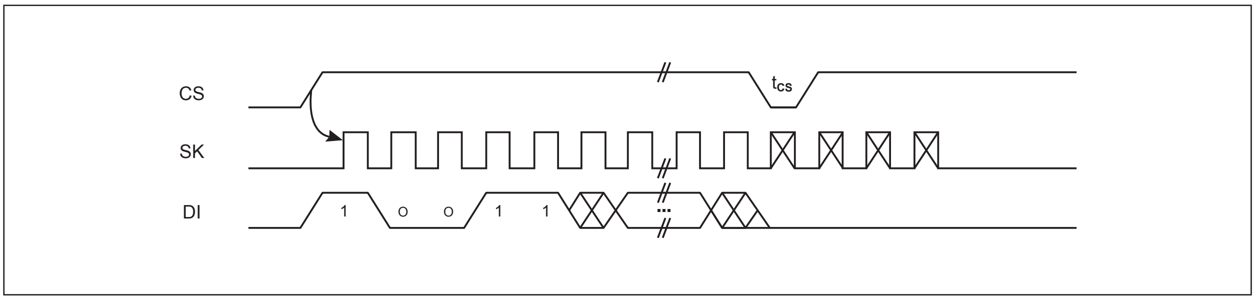
I/O	K93C56(2K)		K93C66(4K)	
	X 8	X 16	X 8	X 16
AN	A8(1)	A7(2)	A8	A7
DN	D7	D15	D7	D15

Note : 1. A8 is a DON'T CARE value ,but the extra clock is required.
2. A7 is a DON'T CARE value ,but the extra clock is required.

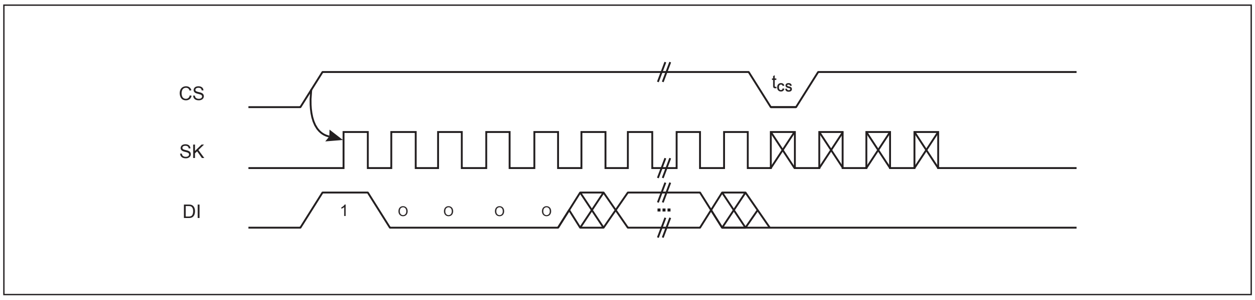
➤Figure 3: READ Timing



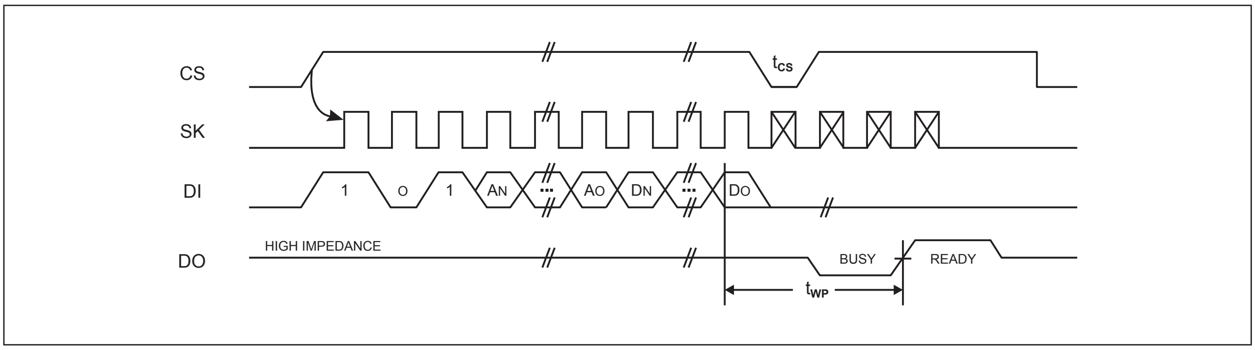
➤Figure 4：EWEN Timing



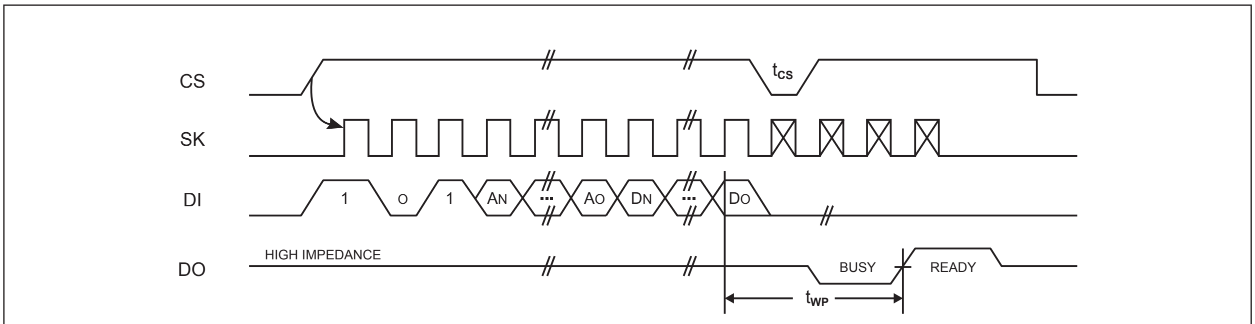
➤Figure 5：EWDS Timing



➤Figure 6：WRITE Timing

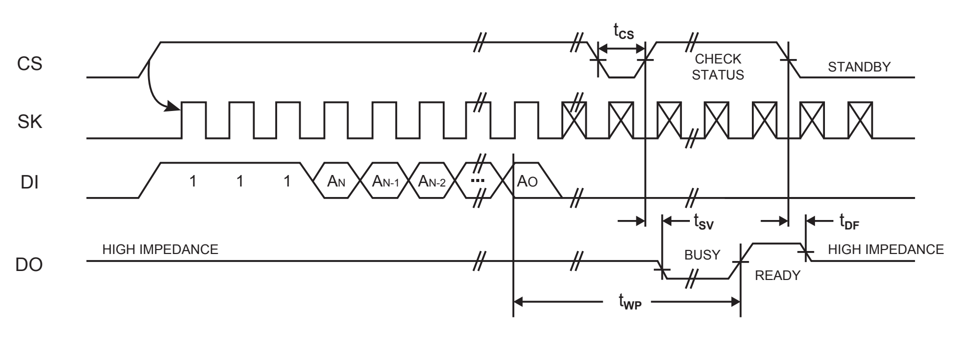


➤Figure 7：WRAL Timing(1)

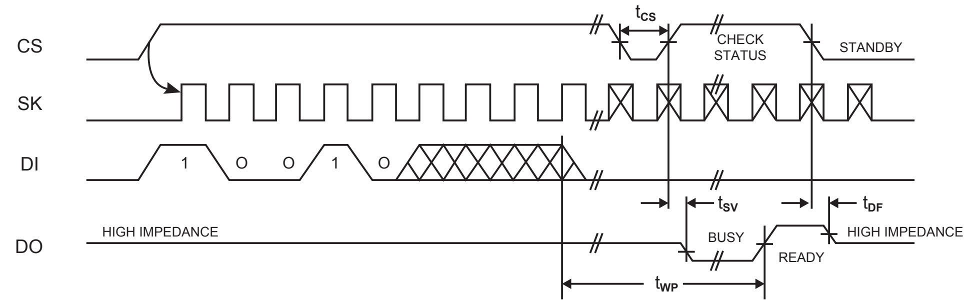


Notes:　1. Valid only at VCC = 4.5V to 5.5V.

➤Figure 8: ERASE Timing



➤Figure 9: ERAL Timing(1)



Notes: 1. Valid only at VCC = 4.5V to 5.5V.

Ordering Information

Code Number

Part Number	L	93	XXX	X	-	X	X	X	X	X
	1	2	3	4		5	6	7	8	9

1.Prefix

2.Series Name

93: Three-wire (SPI) Interface

3.EEPROM Density

C56=2K bits

C66=4K bits

4.Design Option

o=□ (Blank)

5.Package Type

D = DIP

S = SOP

T = TSSOP

W = Wafer/die

6. Temperature Range

C = Com Temp(0 ˚C-70 ˚C)

I = Ind Temp(-40 ˚C-85 ˚C)

E = Exp Temp(-40 ˚C-125 ˚C)

7.Pack Type

T = Tube

R = Tape & Reel

8.Plating Technology

Blank = Standard SnPb plating

G = ECOPACK(RoHS compliant)

9.Operating Voltage

S=2.7~5.5

A=1.8~5.5

Product Datasheet Change Notice

Datasheet Revision History

Version	Content	Date
1.0	Datasheet	2008-12-22

Disclaimers

The information in this publication has been carefully checked and is believed to be entirely accurate at the time of publication. HUAJIE assumes no responsibility, however, for possible errors or omissions, or for any consequences resulting from the use of the information contained herein.

HUAJIE reserves the right to make changes in its products or product specifications with the intent to improve function or design at any time and without notice and is not required to update this documentation to reflect such changes.

This publication does not convey to a purchaser of semiconductor devices described herein any license under the patent rights of HUAJIE or others.

HUAJIE makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does HUAJIE assume any liability arising out of the application or use of any product or circuit and specifically disclaims any and all liability, including without limitation any consequential or incidental damages.

" Typ. " parameters can and do vary in different applications. All operating parameters, including " Typ. " must be validated for each customer application by the customer's technical experts.

HUAJIE products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, for other applications intended to support or sustain life, or for any other application in which the failure of the HUAJIE product could create a situation where personal injury or death may occur.

Should the Buyer purchase or use a HUAJIE product for any such unintended or unauthorized application, the Buyer shall indemnify and hold HUAJIE and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, expenses, and reasonable attorney fees arising out of, either directly or indirectly, any claim of personal injury or death that may be associated with such unintended or unauthorized use, even if such claim alleges that HUAJIE was negligent regarding the design or manufacture of said product.

93C Series (SPI Bus) Serial EEPROM
Data Sheet, Revision 1.0