Monolithic Digital IC

SANYO

LA5657H

System Power Supply IC for Car AV Systems

Overview

The LA5657H provides 10 V/2.2 A and 5 V/1.4 A external pnp transistor based low-saturation regulators with standby functions, as well as 3.3 V, 5 V, and 8 V constant voltage, open collector, and VCC linked (VCC - 1 V) outputs that can be controlled from serial data (CCB). It also includes three reset detection circuits for the VDD, ACC, and battery systems. The LA5657H is an optimal power supply IC for car audio systems and similar products.

Features

- Built-in 10 V and 5 V regulators (external pnp transistor required) with standby (on/off) functions
- Extensive set of output systems: two 8 V systems, single 5 V, 3.25 V, and 5 to 9.7 V (set with an external resistor) systems, four open-collector output systems, and two V_{CC} linked systems.
- Three reset circuits: A_{CC}, V_{DD} (with delay circuit), and BATT
- Full complement of protection circuits
  — Overcurrent protection circuits for all output systems except the open collector and reset circuits
  — Thermal protection circuits for all outputs except the reset circuits

Package Dimensions

unit: mm

3233A-HSOP28H

[LA5657H]

SANYO: HSOP28H (375 mil)
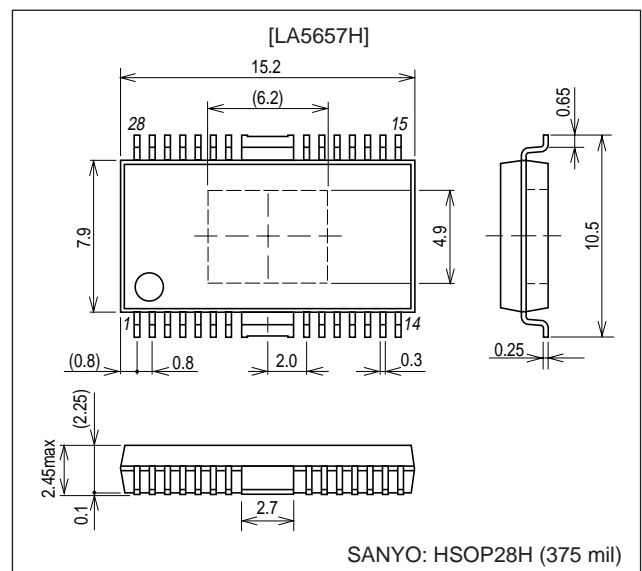
Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		24	V
Allowable power dissipation	Pd max	Ta ≤ 25°C, independent IC	0.82	W
		Ta ≤ 25°C, mounted on a 76.1 × 114.3 × 1.6 mm glass epoxy printed circuit board	2.0	W
Operating temperature	Topr		−30 to +85	°C
Storage temperature	Tstg		−55 to +150	°C

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Recommended Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}	COM10V output, normal operation	10.3 to 18	V
		COM5V output, normal operation	5.3 to 18	V
STBY pin input voltage	VST OFF	Output off control voltage	0 to 1	V
	VST ON	Output on control voltage	2.5 to 5	V
COM10V output current	I_O1		Within the ASO for the external transistor	mA
COM5V output current	I_O2		Within the ASO for the external transistor	mA
LCDV output current	I_O3		0 to 30	mA
TAPE8V output current	I_O4		0 to 30	mA
RD8V output current	I_O5		0 to 200	mA
DSP5V output current	I_O6		0 to 100	mA
DSP3.25V output current	I_O7		0 to 100	mA
AMP+B output current	I_O8		0 to 100	mA
ANT+B output current	I_O9		0 to 250	mA
CAP MR output current	I_O10		0 to 10	mA
P1 output sink current	I_O11		0 to 10	mA
P2 output sink current	I_O12		0 to 10	mA
P3 output sink current	I_O13		0 to 10	mA
ACCRO output sink current	I_O-ACCR		0 to 1	mA
V_{DD}RST output sink current	I_O-V_{DD}R		0 to 1	mA
BATRO output sink current	I_O-BATR		0 to 5	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = 13.2 V, in the specified test circuit

Parameter	Symbol	Conditions	min	typ	max	Unit
Current drain 1	$I_{CC}1$	VSTBY = 0 V, BATRO = High, RESET = High, ACCRO = Low		150	170	µA
Current drain 2	$I_{CC}2$	VSTBY = 5 V, Serial data control outputs: all off BATRO, RESET, and ACCRO outputs: all high		19	25	mA
[V_{DD} Reset Block *1]						
Reset threshold voltage	VTVDDR		4.05	4.25	4.45	V
Hysteresis	VHVDDR		50	80	130	mV
Low-level output voltage	VOLVDDR	ISINK = 50 µA		0.25	0.4	V
High-level output voltage	VOHVDDR	Resistance between RESET and ground: 1 MΩ	0.8 V_{DD}		V_{DD}	V
CDLY outflow current	ICDLY	CDLY outflow current	−4.0	−3.4	−2.8	µA
CDLY threshold voltage	VTHCDLY		1.18	1.25	1.32	V
[BAT Reset Block *2]						
Reset threshold voltage	VTBATR		1.21	1.25	1.29	V
Hysteresis	VHBATR		163	233	326	mV
Leakage current	ILKBATR		−2			µA
Low-level output voltage	VOLBATR	ISINK = 50 µA		0.25	0.4	V
High-level output voltage	VOHBATR	Resistance between BATRO and ground: 1 MΩ	0.8 V_{DD}		V_{DD}	V
[ACC Reset Block *2]						
Reset threshold voltage	VTACCR		1.21	1.25	1.29	V
Hysteresis	VHACCR		10	20	30	mV
Leakage current	ILKACCR		−2			µA
Low-level output voltage	VOLACCR	ISINK = 1 mA		0.35	0.5	V
High-level output voltage	VOHACCR	Resistance between ACCRO and ground: 1 MΩ	0.8 V_{DD}		V_{DD}	V

Continued from preceding page.

Parameter	Symbol	Conditions	Ratings min	Ratings typ	Ratings max	Unit
[COM10V Output (V_{CC} = 13.2 V, VSTBY = 5 V, I_O2 = 2.2 A)]						
Output voltage	V_O1	External transistor: 2SB921	9.55	10	10.45	V
Dropout voltage	VDROP1	V_{CC} = 9.55 V		0.3	0.6	V
Line regulation	ΔVOLN1	11.15 V ≤ V_{CC} ≤ 18 V		30	300	mV
Load regulation	ΔVOLD1	0 ≤ I_O1 ≤ 2.2 A		200	800	mV
Control input current	ICONT1		20	22	26.4	mA
Output off voltage	V_O1 OFF				0.2	V
Ripple rejection (reference value)	RREJ1	f = 120 Hz, 11.15 V ≤ V_{CC} ≤ 18 V		70		dB
[COM5V Output (V_{CC} = 13.2 V, VSTBY = 5 V, I_O2 = 1.4 A)]						
Output voltage	V_O2	External transistor: 2SB921	4.775	5	5.225	V
Dropout voltage	VDROP2	V_{CC} = 4.775 V		0.3	0.6	V
Line regulation	ΔVOLN2	5.925 V ≤ V_{CC} ≤ 18 V		30	300	mV
Load regulation	ΔVOLD2	0 ≤ I_O2 ≤ 1.4 A		200	800	mV
Control input current	ICONT2		15	16.7	20.2	mA
Output off voltage	V_O2 OFF				0.2	V
Ripple rejection (reference value)	RREJ2	f = 120 Hz, 5.925 V ≤ V_{CC} ≤ 18 V		70		dB
[LCDV Output (V_{CC} = 13.2 V, VSTBY = 5 V, I_O2 = 30 mA, CN pin: open)]						
Output voltage	V_O3		4.85	5	5.15	V
Dropout voltage	VDROP3	V_{CC} = 4.85 V		0.3	0.6	V
Line regulation	ΔVOLN3	5.85 V ≤ V_{CC} ≤ 18 V		50	75	mV
Load regulation	ΔVOLD3	0 ≤ I_O2 ≤ 30 mA		100	150	mV
Peak output current	IOP3		30			mA
Output short current (reference value)	IOSC3			60		mA
Output off voltage	V_O3 OFF				0.2	V
[TAPE8V Output (V_{CC} = 13.2 V, VSTBY = 5 V, I_O4 = 30 mA)]						
Output voltage	V_O4		7.64	8	8.36	V
Dropout voltage	VDROP4	V_O1 = 7.6 V		1.0	1.4	V
Line regulation	ΔVOLN4	9.9 V ≤ V_{CC} ≤ 18 V		50	75	mV
Load regulation	ΔVOLD4	0 ≤ I_O4 ≤ 30 mA		100	150	mV
Peak output current	IOP4		30			mA
Output short current (reference value)	IOSC4			220		mA
Output off voltage	V_O4 OFF				0.2	V
[RD8V Output (V_{CC} = 13.2 V, VSTBY = 5 V, I_O5 = 200 mA)]						
Output voltage	V_O5		7.64	8	8.36	V
Dropout voltage	VDROP5	V_O1 = 7.6 V		1.0	1.4	V
Line regulation	ΔVOLN5	9.96 V ≤ V_{CC} ≤ 18 V		50	75	mV
Load regulation	ΔVOLD5	0 ≤ I_O5 ≤ 200 mA		100	150	mV
Peak output current	IOP5		200			mA
Output short current (reference value)	IOSC5			900		mA
Output off voltage	V_O5 OFF				0.2	V
[DSP5V Output (V_{CC} = 13.2 V, VSTBY = 5 V, I_O6 = 100 mA)]						
Output voltage	V_O6		4.775	5	5.225	V
Dropout voltage	VDROP6	V_O1 = 4.775 V		1.0	1.4	V
Line regulation	ΔVOLN6	6.825 V ≤ V_{CC} ≤ 18 V		50	75	mV
Load regulation	ΔVOLD6	0 ≤ I_O6 ≤ 100 mA		100	150	mV
Peak output current	IOP6		100			mA
Output short current (reference value)	IOSC6			520		mA
Output off voltage	V_O6 OFF				0.2	V

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Parameter	Symbol	Conditions	Ratings min	Ratings typ	Ratings max	Unit
[DSP3.25V Output (V_{CC} = 13.2 V, VSTBY = 5 V, I_O7 = 100 mA)]						
Output voltage	V_O7		3.104	3.25	3.396	V
Dropout voltage	VDROP7	V_O2 = 3.104 V		1.0	1.4	V
Line regulation	ΔVOLN7	4.996 V ≤ V_{CC} ≤ 18 V		50	75	mV
Load regulation	ΔVOLD7	0 ≤ I_O7 ≤ 100 mA		100	150	mV
Peak output current	IOP7		100			mA
Output short current (reference value)	IOSC7			420		mA
Output off voltage	V_O7 OFF				0.2	V
[AMP + B Output (V_{CC} = 13.2 V, VSTBY = 5 V, I_O8 = 100 mA)]						
Output voltage	V_O8		11.7	12.2		V
Dropout voltage	VDROP8			1	1.5	V
Peak output current	IOP8		100			mA
Output short current (reference value)	IOSC8			300		mA
Output off voltage	V_O8 OFF				0.2	V
[ANT + B Output (V_{CC} = 13.2 V, VSTBY = 5 V, I_O9 = 250 mA)]						
Output voltage	V_O9		11.7	12.2		V
Dropout voltage	VDROP9			1	1.5	V
Peak output current	IOP9		250			mA
Output short current (reference value)	IOSC9			700		mA
Output off voltage	V_O9 OFF				0.2	V
[CAP MR Output (V_{CC} = 13.2 V, VSTBY = 5 V, I_O10 = 10 mA)]						
Dropout voltage	VDROP10			0.4	0.8	V
Output sink current	I_O10		10			mA
[P1 (ILL) Output (V_{CC} = 13.2 V, VSTBY = 5 V, I_O11 = 10 mA)]						
Dropout voltage	VDROP11			0.4	0.8	V
Output sink current	I_O11		10			mA
[P2 (LCD) Output (V_{CC} = 13.2 V, VSTBY = 5 V, I_O12 = 10 mA)]						
Dropout voltage	VDROP12			0.4	0.8	V
Output sink current	I_O12		10			mA
[P3 (CAP MR) Output (V_{CC} = 13.2 V, VSTBY = 5 V, I_O13 = 10 mA)]						
Dropout voltage	VDROP13			0.4	0.8	V
Output sink current	I_O13		10			mA
[Thermal Protection Circuit]						
Operating temperature *3	TSD	V_O1 and V_O2 operation V_O3 to V_O13 linked to V_O1 and V_O2 operation.	150	175		°C

Notes on items *1 to *3.
(1) V_{DD} reset block (*1)
 • The reset detection function detects the level of V_{DD}5V input to V_{DD} IN.
 • This reset function operates correctly when the V_{DD} IN voltage is over 0.5 V, but is undefined when V_{DD} IN is under 0.5 V. The reset voltage must never exceed V_{DD} IN.
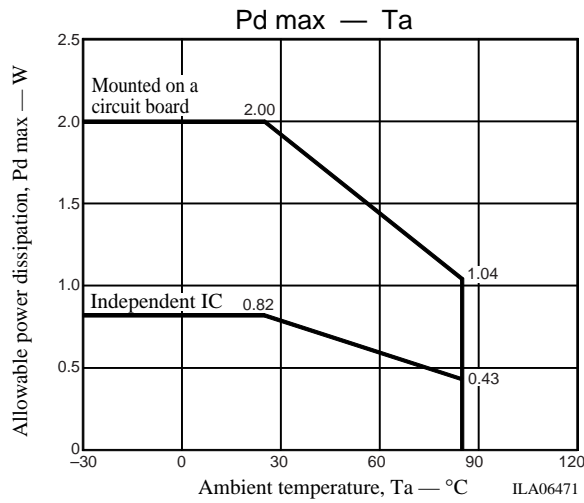 • The allowable range for the threshold voltage has a tolerance of ±4.7%.
(2) BAT and ACC reset blocks (*2)
 • These reset detection outputs must operate correctly when the V_{DD} IN voltage is over 2 V. The reset voltages must never exceed V_{DD} IN.
 • The ACC detection function has no region where detection is unpredictable according to the value of the voltage detected. That is, the low level will be detected correctly when ACC IN is 0 V.
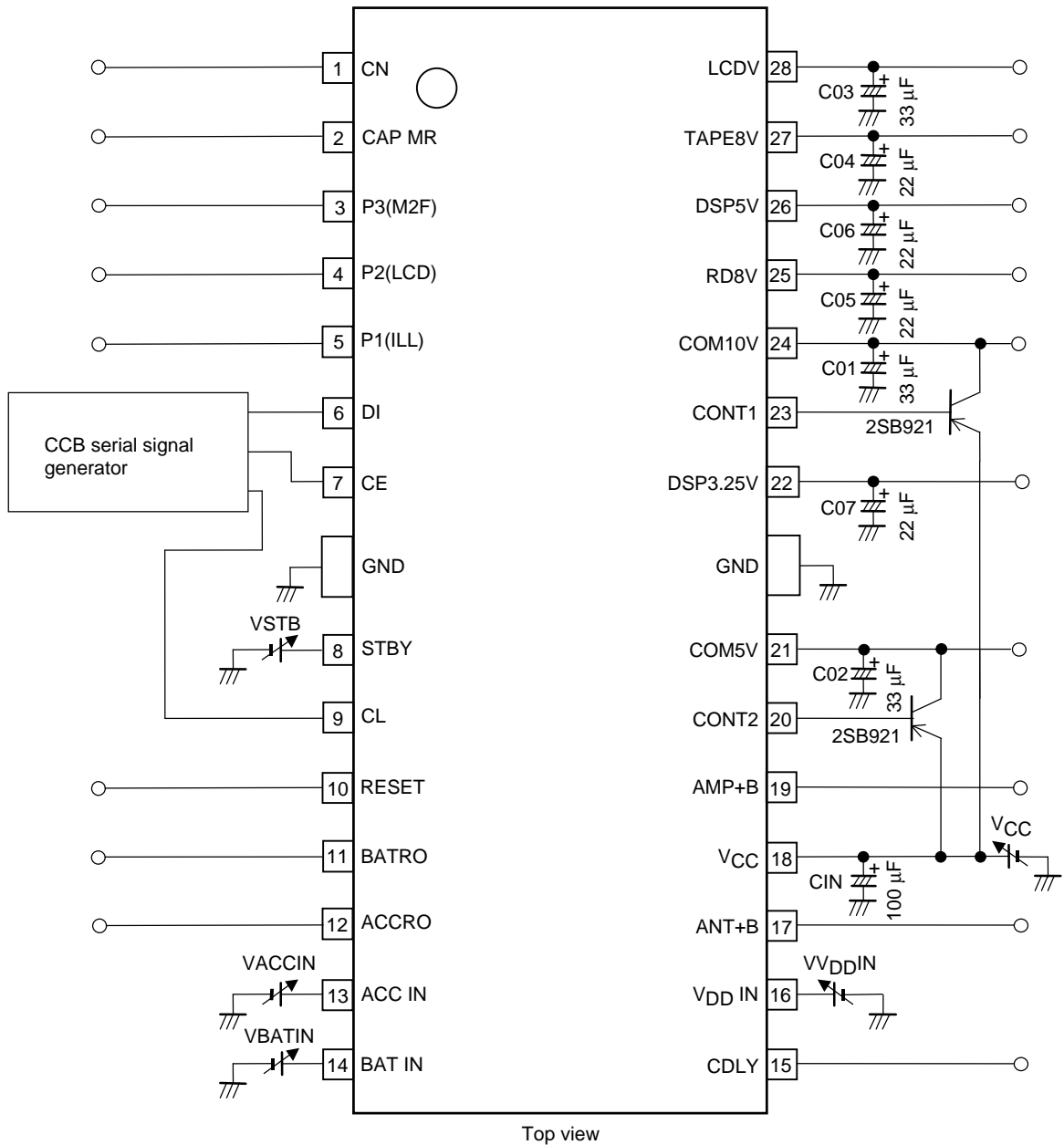 • The allowable range for the threshold voltage has a tolerance of ±3.2%.
(3) Thermal protection and operating temperature (*3)
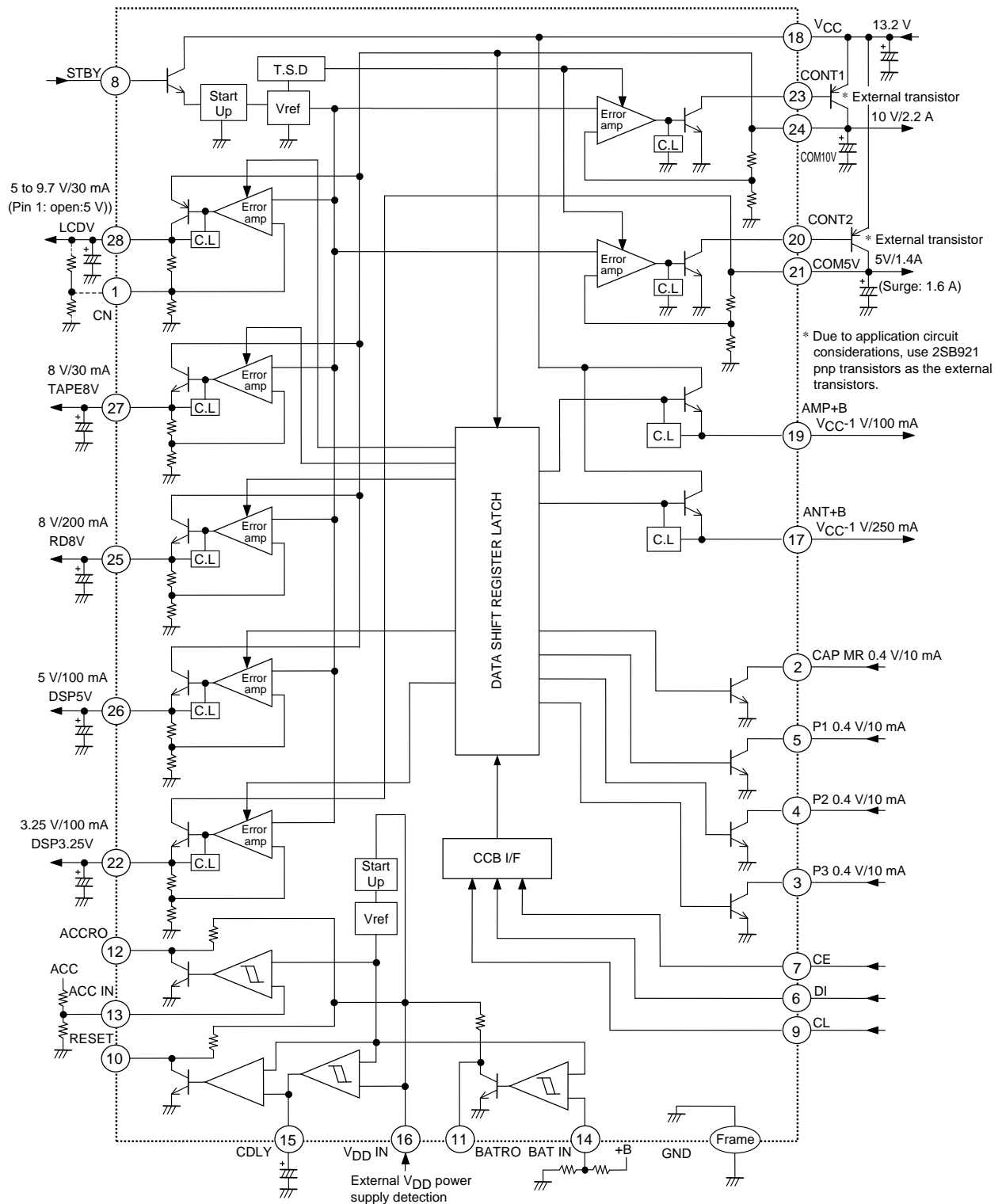 • The values shown are design target values and are not tested.
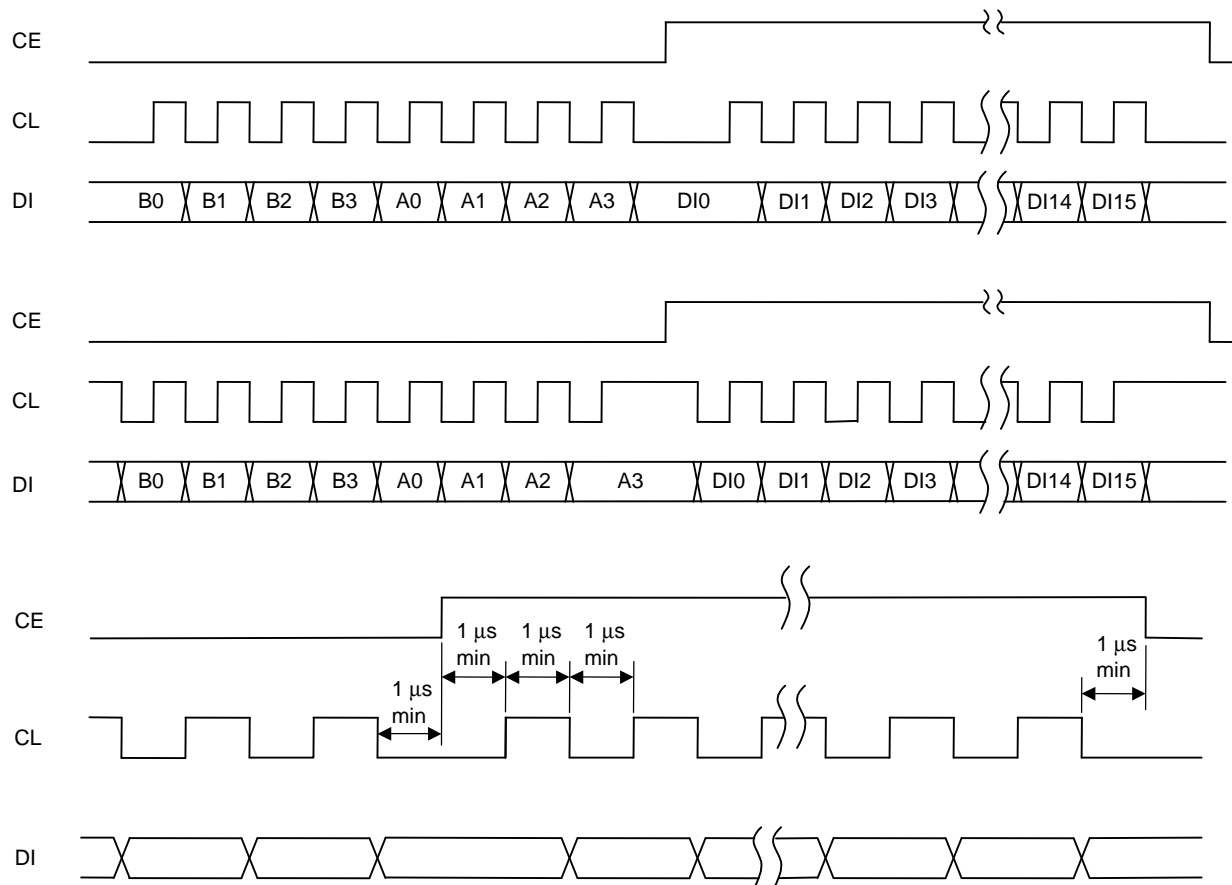
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Pd max — Ta

Allowable power dissipation, Pd max — W

Mounted on a circuit board 2.00

Independent IC 0.82

1.04

0.43

Ambient temperature, Ta — °C

ILA06471

Pin Assignment and Test Circuit

Pin	Signal		Pin	Signal
1	CN		28	LCDV
2	CAP MR		27	TAPE8V
3	P3(M2F)		26	DSP5V
4	P2(LCD)		25	RD8V
5	P1(ILL)		24	COM10V
6	DI		23	CONT1
7	CE		22	DSP3.25V
	GND			GND
8	STBY		21	COM5V
9	CL		20	CONT2
10	RESET		19	AMP+B
11	BATRO		18	V_{CC}
12	ACCRO		17	ANT+B
13	ACC IN		16	V_{DD} IN
14	BAT IN		15	CDLY

CCB serial signal generator

VSTB

VACCIN

VBATIN

C03 33 µF
C04 22 µF
C06 22 µF
C05 22 µF
C01 33 µF
2SB921
C07 22 µF
C02 33 µF
2SB921
CIN 100 µF
V_{CC}
V_{VDD}IN

Top view

LA5657H

Equivalent Circuit Block Diagram

STBY 8

Start Up

T.S.D

Vref

Error amp

C.L

V$_{CC}$ 18 13.2 V

CONT1 23 * External transistor 10 V/2.2 A

24

COM10V

5 to 9.7 V/30 mA
(Pin 1: open:5 V))

LCDV 28

C.L

Error amp

1

CN

Error amp

C.L

CONT2 20 * External transistor 5V/1.4A

COM5V 21 (Surge: 1.6 A)

* Due to application circuit considerations, use 2SB921 pnp transistors as the external transistors.

8 V/30 mA
TAPE8V 27

C.L

Error amp

AMP+B
V$_{CC}$-1 V/100 mA 19

C.L

8 V/200 mA
RD8V 25

Error amp

C.L

ANT+B
V$_{CC}$-1 V/250 mA 17

C.L

5 V/100 mA
DSP5V 26

Error amp

C.L

DATA SHIFT REGISTER LATCH

CAP MR 0.4 V/10 mA 2

P1 0.4 V/10 mA 5

3.25 V/100 mA
DSP3.25V 22

Error amp

C.L

P2 0.4 V/10 mA 4

P3 0.4 V/10 mA 3

ACCRO 12

ACC
ACC IN 13

CCB I/F

Start Up

Vref

CE 7

DI 6

RESET 10

CL 9

CDLY 15

V$_{DD}$ IN 16

External V$_{DD}$ power supply detection

BATRO 11

BAT IN 14

+B

GND

Frame

LA5657H

Control System Timing and Data Format

The LA5657H is controlled by inputting the stipulated serial data to the CL, DI, and CE pins. This data consists of a total of 24 bits of which 8 bits are address and 16 bits are data.

• Address code (B0 to A3)

  The LA5657H has an 8-bit address code that allows it to be used with the same specifications as other Sanyo serial bus CCB ICs.

Address Code

LSB							MSB	
B0	B1	B2	B3	A0	A1	A2	A3	HEX
1	0	1	0	1	0	1	1	D5

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- On/Off Control Code Assignment

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	Operation
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LCDV ON
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TAPE8V ON
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	RD8V ON
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	DSP5V ON
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	DSP3.25V ON
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	AMP+B ON
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	ANT+B ON
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	CAP MR ON
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	P1 ON
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	P2 ON
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	P3 ON

This catalog provides information as of May, 2004. Specifications and information herein are subject to change without notice.