Ordering number : ENA0003A

SANYO Semiconductors
DATA SHEET

Monolithic Linear IC

LA5663V — Phase Control Voltage Inverter Control IC

Overview

The LA5663V is Phase Control Voltage Inverter Control IC.

Functions

- Phase control technique allows the voltage transformer to be driven at a frequency that provides excellent efficiency.
- The phase can be adjusted with an external resistor.
- Allows burst adjustment.
- Full complement of built-in protection circuits, including over-voltage protection and tube current detection and protection.
- High-precision reference voltage system. VREM precision: ±1%
- The on/off state of the VREM circuit can be controlled independent.

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{CC}		24	V
Maximum power drain allowed	Pd max	Independent IC.	440	mW
Operating temperature range	Topr		-30 to 85	°C
Storage temperature range	Tstg		-55 to 150	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Input voltage	V_{CC}		4.5 to 23	V
Oscillation frequency	fosc		40 to 500	kHz
Burst drive frequency	f_{PWM}		50 to 1000	Hz
Output drive load capacity	CL1		0 to 1000	pF
	CL2		0 to 1000	pF

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Electrical Characteristics at Ta = 25°C, V_{CC} = 15.0V

Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
Current drain during standby		Ioff				5	μA
Current drain during operation		Iop	V_{CC} = 23V, DTC = 1.229V, CL = 500pF	8	11	14	mA
Regulator voltage		Vreg	V_{CC} = 4.5 to 23V, Ireg = 0 to 0.5mA	3.395	3.5	3.605	V
Regulator temperature coefficient		Vreg (T)	Ireg = 0.5mA, Ta = 0 to 60°C		0.23		%
Regulator current		Ireg		-0.3		2	mA
Reference voltage		Vref	V_{CC} = 4.5 to 23V, Iref = 0 to 0.1mA	1.972	2	2.028	V
Reference voltage temperature coefficient		Vref (T)	Iref = 0.1mA, Ta = 0 to 60°C		0.23		%
Reference voltage current		Iref		0		0.2	mA
p-channel output voltage	"H" level	Voph1	Relative to V_{CC}, load current of 0mA.	-0.4			V
		Voph2	Relative to V_{CC}, load current of 10mA.	-1.2			V
	"L" level	Vopl1	Relative to GND, load current of 0mA.			1.3	V
		Vopl2	Relative to GND, load current of 10mA.			1.4	V
	Clamp level	Vopc	Relative to V_{CC}	-12	-10	-8	V
	tr	trp	CL = 500pF		150		ns
	tf	tfp	CL = 500pF		200		ns
n-channel output voltage	"H" level	Vonh1	Relative to V_{CC}, load current of 0mA.	-1.5			V
		Vonh2	Relative to V_{CC}, load current of 10mA.	-2			V
	"L" level	Vonl1	Relative to GND, load current of 0mA.			0.4	V
		Vonl2	Relative to GND, load current of 10mA.			1.2	V
	Clamp level	Vopc	Relative to V_{CC}	8	10	12	V
	tr	trn	CL = 500pF		650		ns
	tf	tfn	CL = 500pF		50		ns
Burst drive duty	BRIGHT_VR = 2.2V	Duty1	V_{CC} = 4.5 to 23V	100			%
	BRIGHT_VR = 1.847V	Duty2	V_{CC} = 4.5 to 23V	86	90	94	%
	BRIGHT_VR = 1.229V	Duty3	V_{CC} = 4.5 to 23V	47	50	53	%
	BRIGHT_VR = 0.618V	Duty4	V_{CC} = 4.5 to 23V	7	10	13	%
	BRIGHT_VR = 0.4V	Duty5	V_{CC} = 4.5 to 23V			0	%
Burst drive duty temperature coefficient	BRIGHT_VR = 2.2V	Duty1 (T)	Ta = 0 to 60°C		0		%
	BRIGHT_VR = 1.847V	Duty2 (T)	Ta = 0 to 60°C		2		%
	BRIGHT_VR = 1.229V	Duty3 (T)	Ta = 0 to 60°C		2		%
	BRIGHT_VR = 0.618V	Duty4 (T)	Ta = 0 to 60°C		2		%
	BRIGHT_VR = 0.4V	Duty5 (T)	Ta = 0 to 60°C		0		%
Oscillation frequency	fmax	fosc1	capacity = ±1%	247	258	269	kHz
	fmin	fosc2	capacity = ±1%	195	202	209	kHz
Oscillation frequency temperature coefficient	fmax (T)	fosc1 (T)	Ta = 0 to 60°C		1.3		%
	fmin (T)	fosc2 (T)	Ta = 0 to 60°C		1.3		%
Burst drive frequency		fosc1	capacity = ±1%	191	202	213	Hz
Burst drive frequency temperature coefficient		fosc1	Ta = 0 to 60°C		0.64		%
Remote voltage	During operation	Vremon		2			V
	Stopped	Vremoff				0.7	V
OP1 output		-VCON1	V_{CC} = 22V	0.27	0.32	0.37	V
		-VCON2	V_{CC} = 7V	1.557	1.6	1.643	V
		-VCON_SINK	-VCOM sink current	100			μA
		-VCON_SOUR	-VCOM source current	10			μA
DTC-100% ON threshold voltage		V100		2.16	2.2	2.24	V
DTC-100% OFF threshold voltage		V0		0.392	0.4	0.408	V
SCP	Operation start time	tscp	SCP capacity = 0.33μF	0.7	1	1.5	s
	Threshold voltage	SCP (DET_CR)		0.23	0.26	0.29	V

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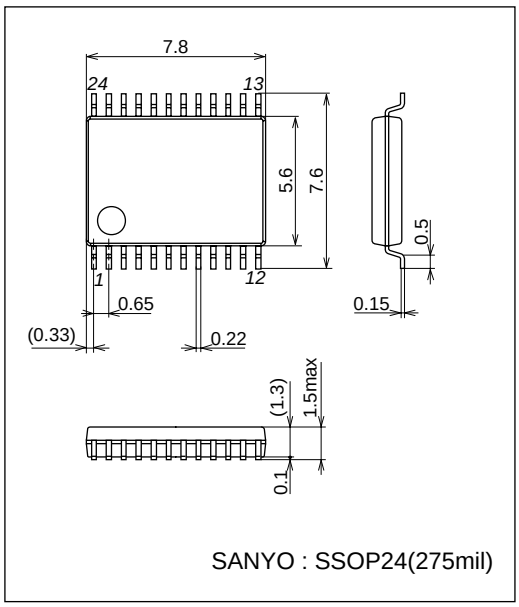
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input pin						
Input current of V_PHASE pin	IVPHASE		-0.2		0.2	µA
Input current of BRIGHT_VR pin	IBRIGHT_VR		-0.2		0.2	µA
Current of DTC	IVPHASE		-0.2		0.2	µA

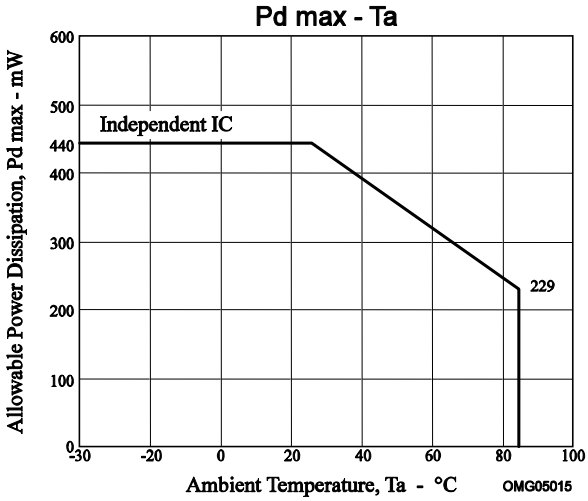
Package Dimensions

unit: mm

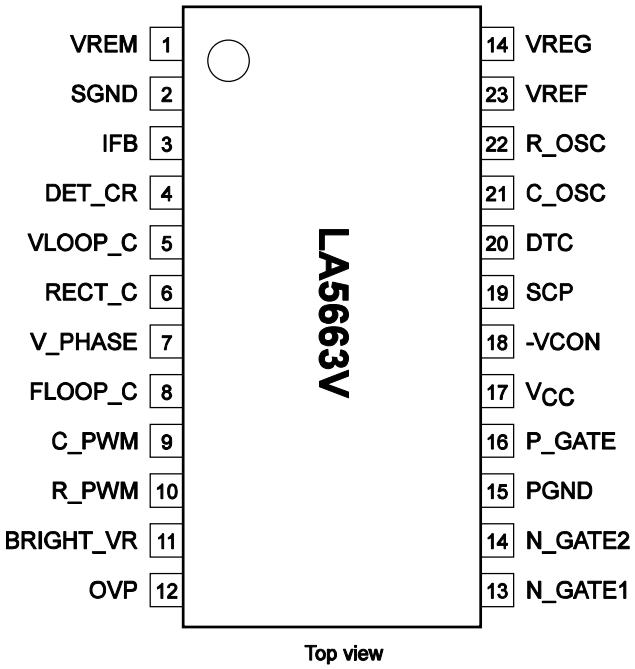
3175C



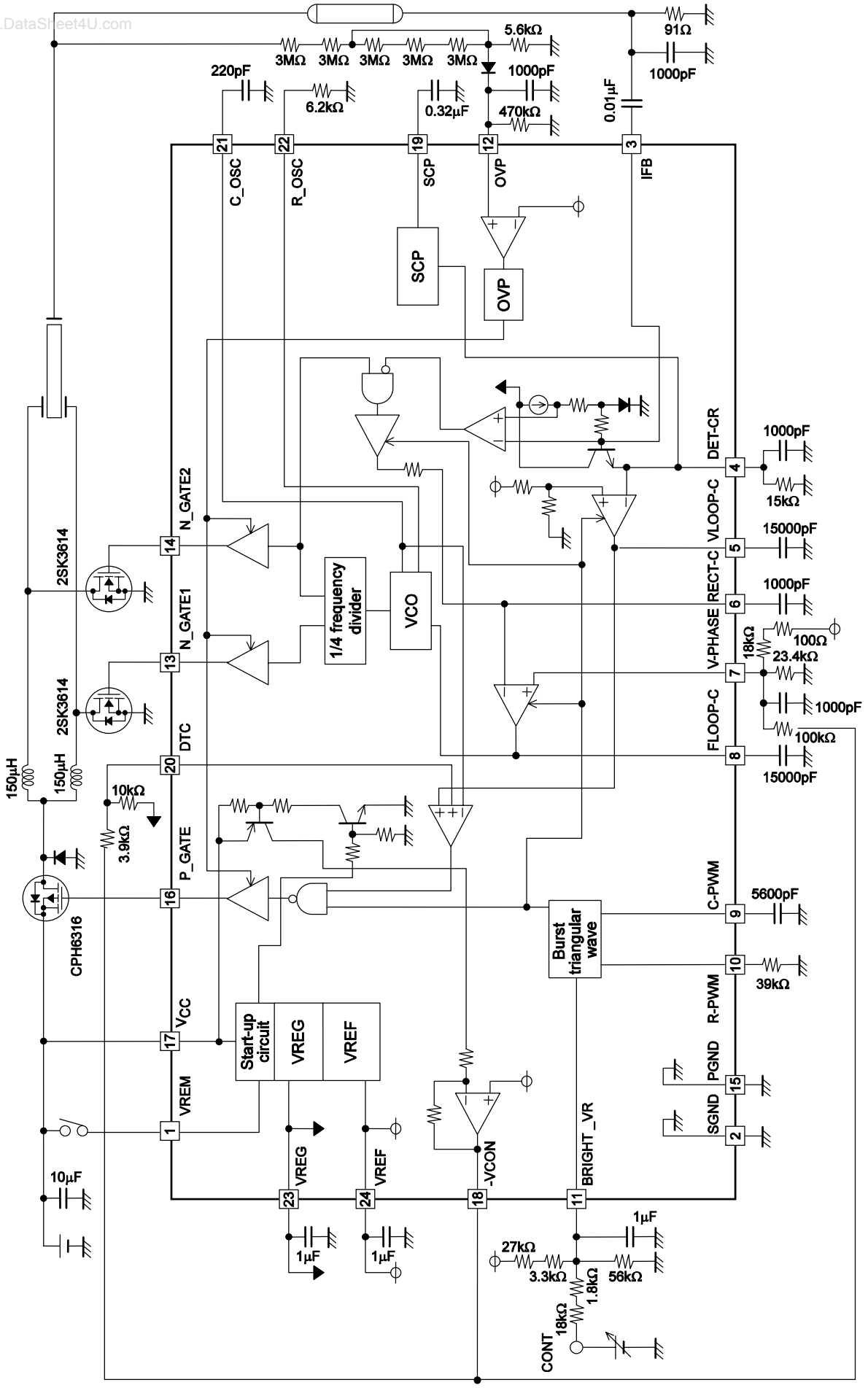
SANYO : SSOP24(275mil)



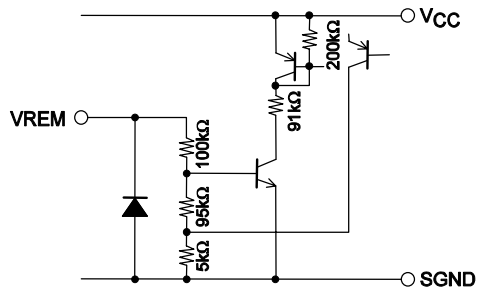
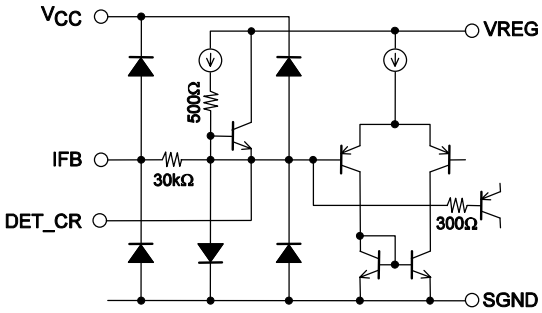
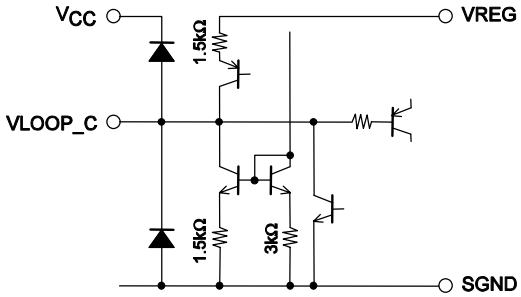
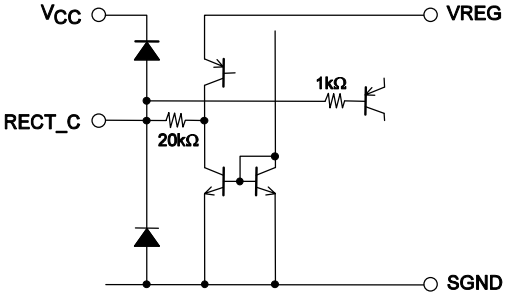
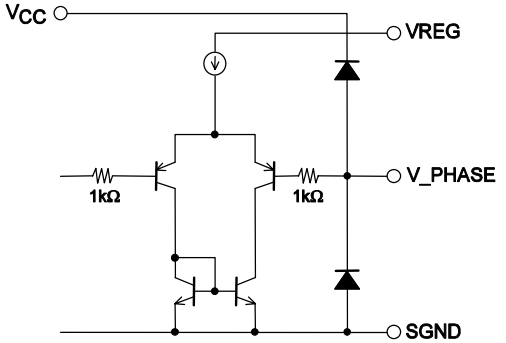
Pin Assignment



Block Diagram and Application Circuit Example



Pin Functions

Pin No.	Pin name	Function	Equivalent circuit
1	VREM	ON/OFF terminal of the IC.	
2	SGND	Signal Ground terminal.	
3	IFB	CCFL electric current waveform input terminal.	
4	DET_CR	Rectification (pulse way) waveform of CCFL output terminal.	
5	VLOOP_C	Error amplifier output terminal.	
6	RECT_C	Phase difference output terminal	
7	V_PHASE	Phase difference setup terminal	

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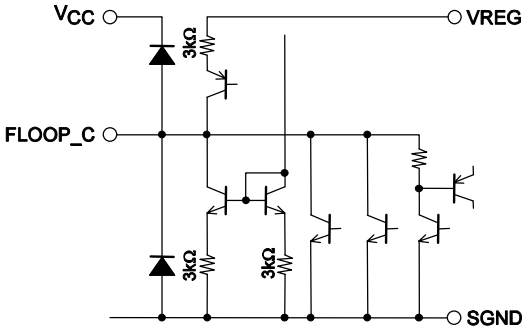
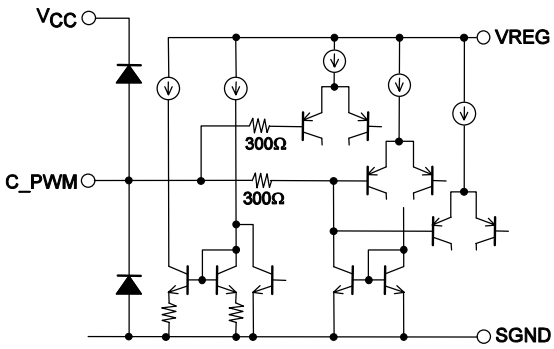
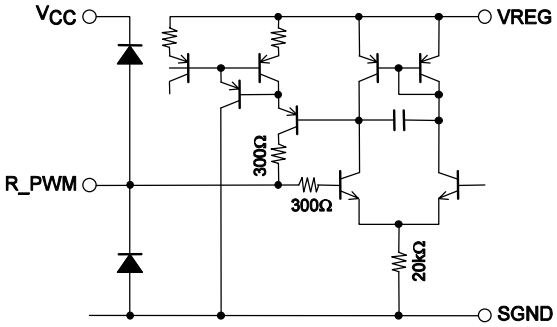
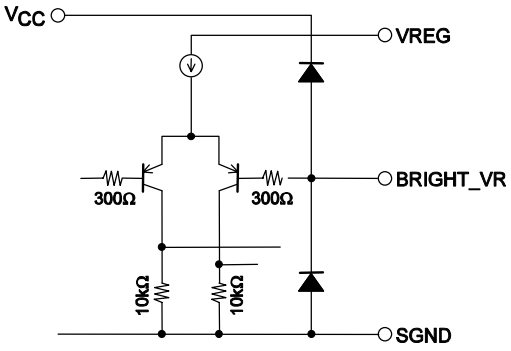
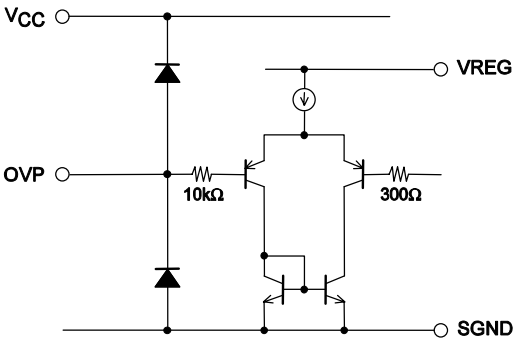
Pin No.	Pin name	Function	Equivalent circuit
8	FLOOP_C	VCO input terminal.	
9	C_PWM	Capacitor terminal for the burst drive frequency setup.	
10	R_PWM	Resistance terminal for the burst drive frequency setup.	
11	BRIGHT_VR	Burst width set up terminal.	
12	OVP	Detection input terminal of over voltage protection circuit.	

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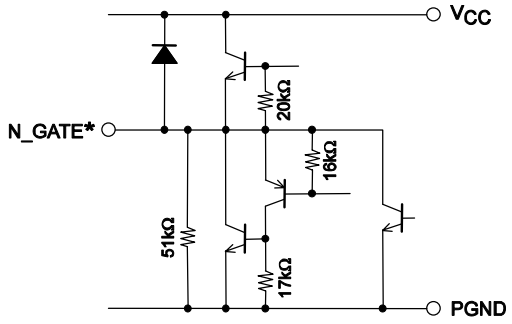
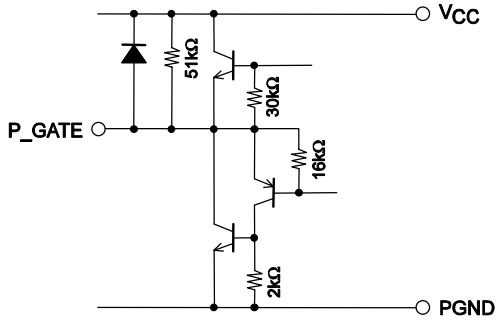
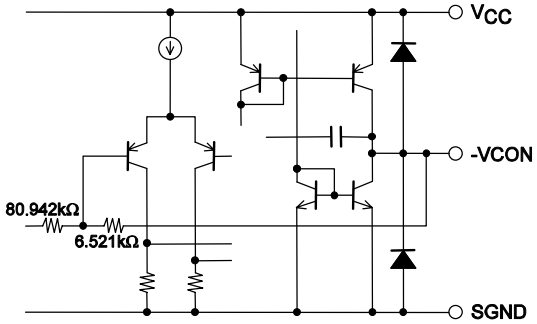
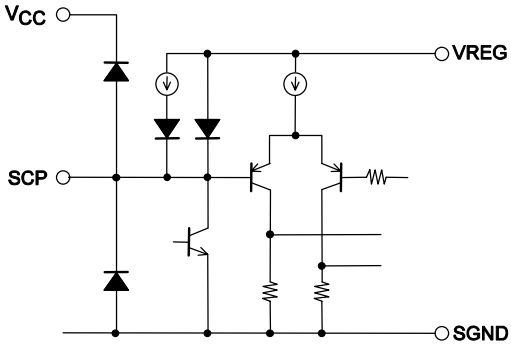
Pin No.	Pin name	Function	Equivalent circuit
13 14	N_GATE1 N_GATE2	NchMOS drive terminal. NchMOS drive terminal.	
15	PGND	Power ground terminal.	
16	P_GATE	PchMOS drive terminal.	
17	V_{CC}	Power supply terminal.	
18	-VCON	Output voltage is inversely proportional to V_{CC}.	
19	SCP	Time constant of short protection circuit setup terminal.	

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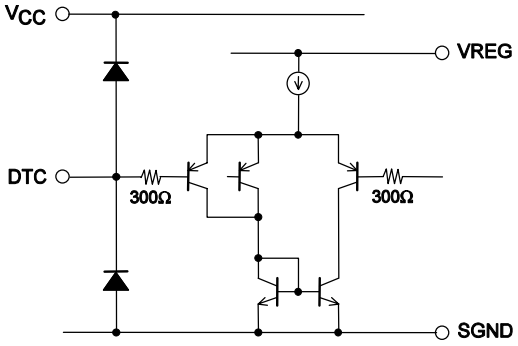
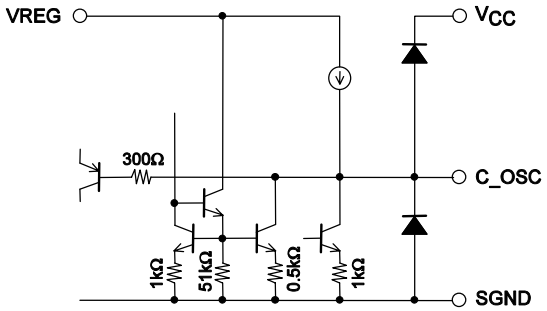
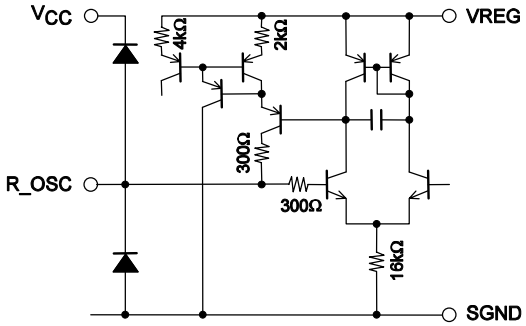
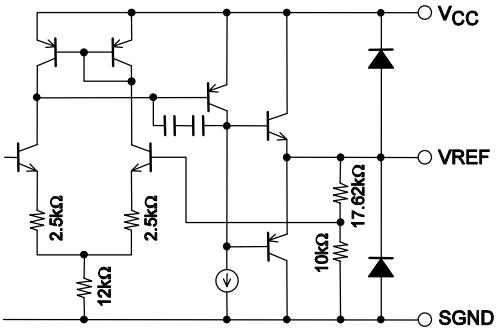
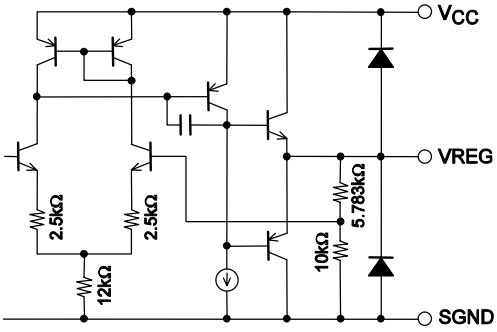
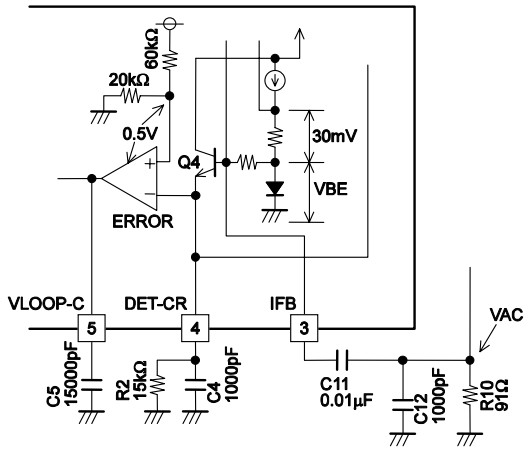
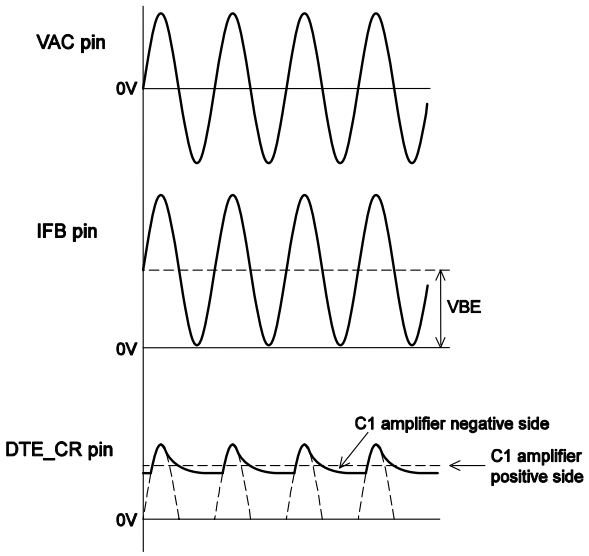
Pin No.	Pin name	Function	Equivalent circuit
20	DTC	Dead time setup terminal.	
21	C_OSC	Capacitor terminal for the VCO frequency setup.	
22	R_OSC	Resistance terminal for the VCO frequency setup.	
23	VREF	Standard voltage output terminal.	
24	VREG	Regulator voltage output terminal.	

Functional Descriptions

(1) IFB and DET_CR pins

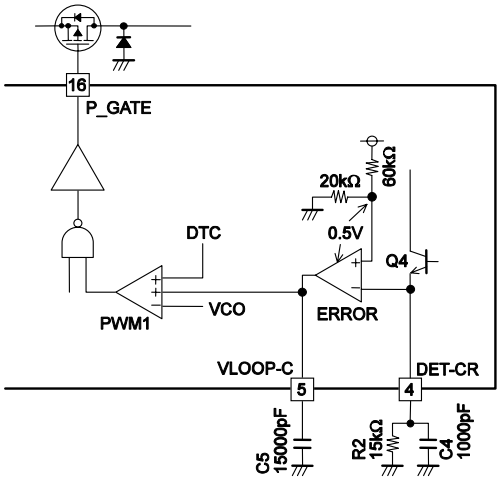
The IFB pin connects the CCFL current waveform detected by R10 to the Q4 base with bias VBE. The DET_CR pin output level depends on both the Q4 base voltage less the VF component and the time constant determined by C4 and R2. These connections rectify the AC CCFL current waveform (VAC) for input to the negative side of the ERROR amplifier.





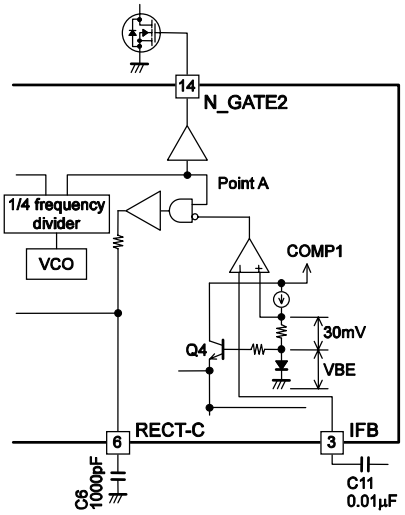
(2) VLOOP_C and PGATE pins

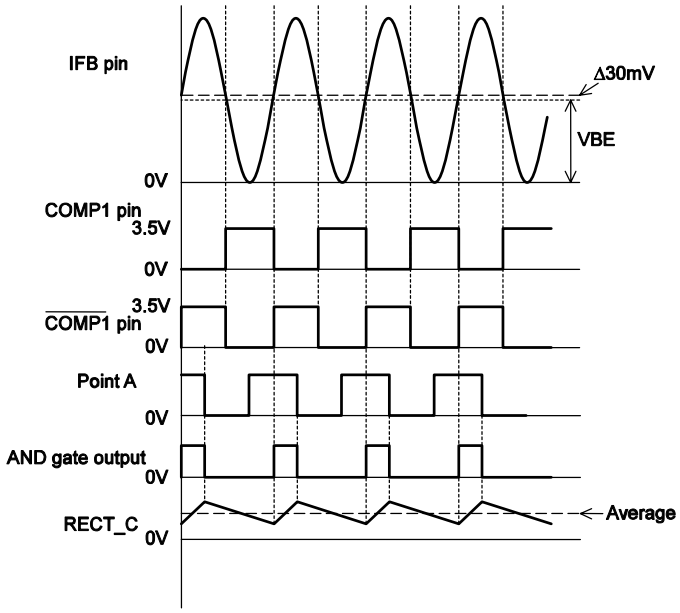
The PWM waveform output from the P_GATE pin is the result of the PWM1 amplifier comparing the VLOOP_C voltage and the VOC triangular wave so that the rectified CCFL current waveform from the DET_CR pin has the same potential (0.5V) as the positive side of the ERROR amplifier. This PWM control ensures that the CCFL current remains constant.



(3) RECT_C pin

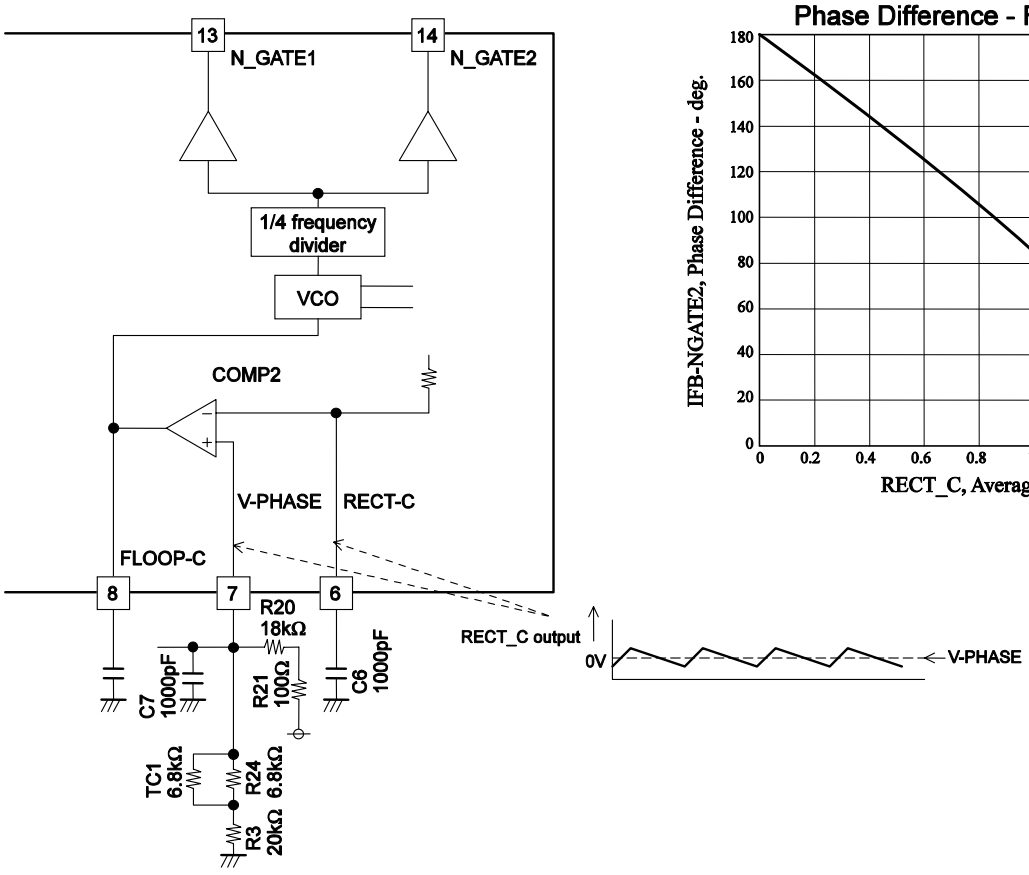
COMP1 rectifies the CCFL current waveform, plus bias VBE, from the IFB pin. ANDing this waveform voltage with that from point A (this latter has the same phase as NGATE2) averages the two, producing phase difference voltage output from the RECT_C pin.





(4) V_PHASE and FLOOP_C pins

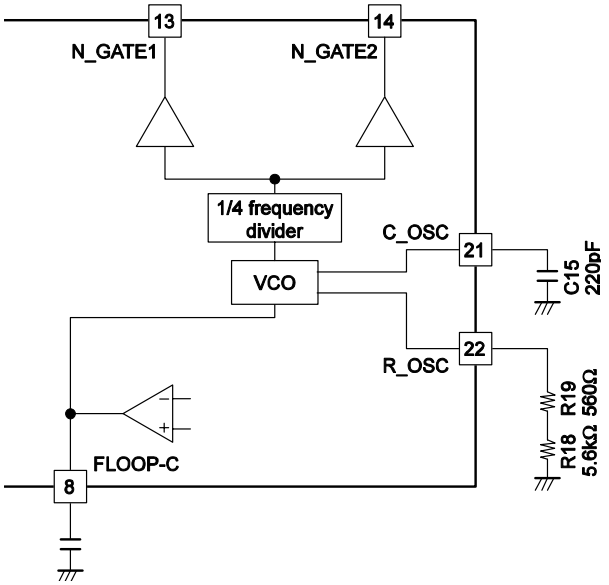
COMP2 controls the VCO frequency so that the RECT_C and V_PHASE pins have the same voltage. The RECT_C pin voltage represents a phase difference voltage, so changing the V_PHASE pin voltage adjusts the phase difference.

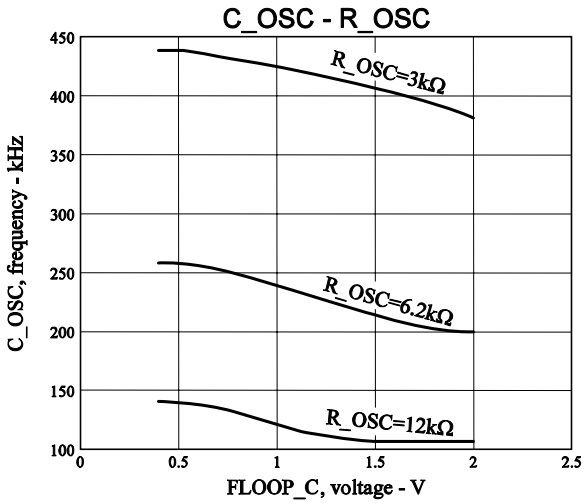


* The above graph is based on measurements for the IC in isolation. Actual phase difference adjustment requires connection to the piezoelectric transformer.

(5) C_OSC and R_OSC pins

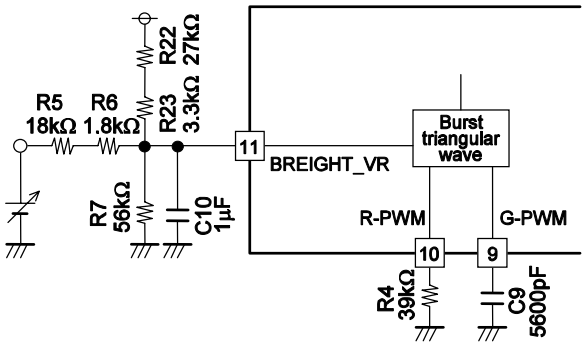
These inputs determine the VCO oscillation frequency. Use R_OSC to change the basic frequency.

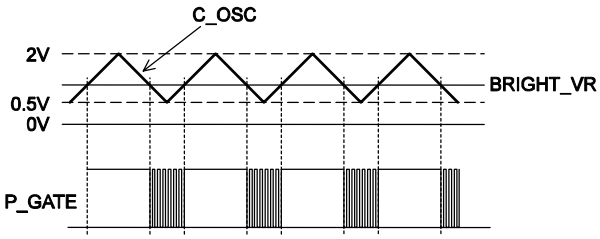


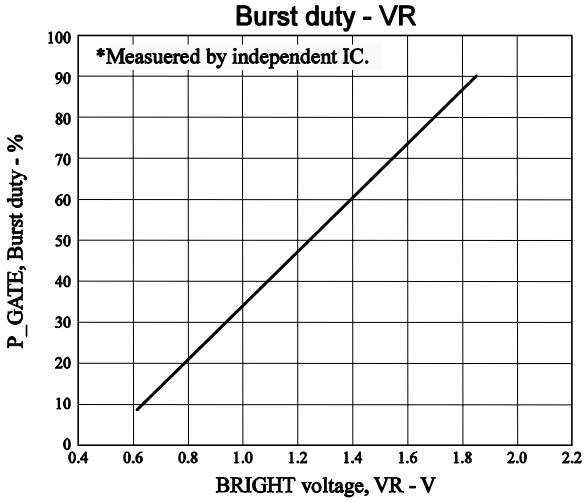


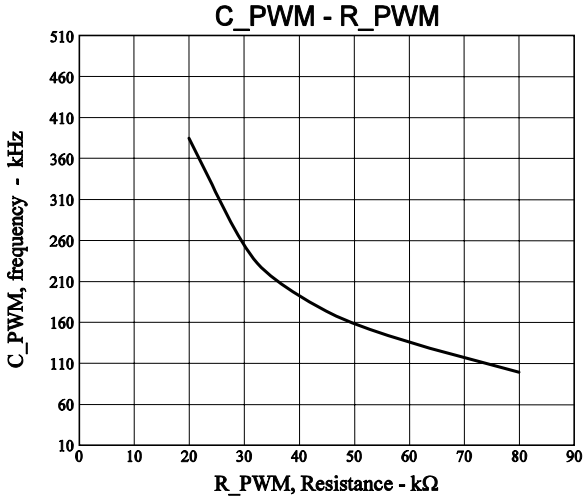
(6) C_PWM, R_PWM, and BRIGHT_VR pins

These inputs determine the burst drive frequency. Use the BRIGHT_VR pin voltage to change the burst width and R_PWM to change the burst drive frequency.







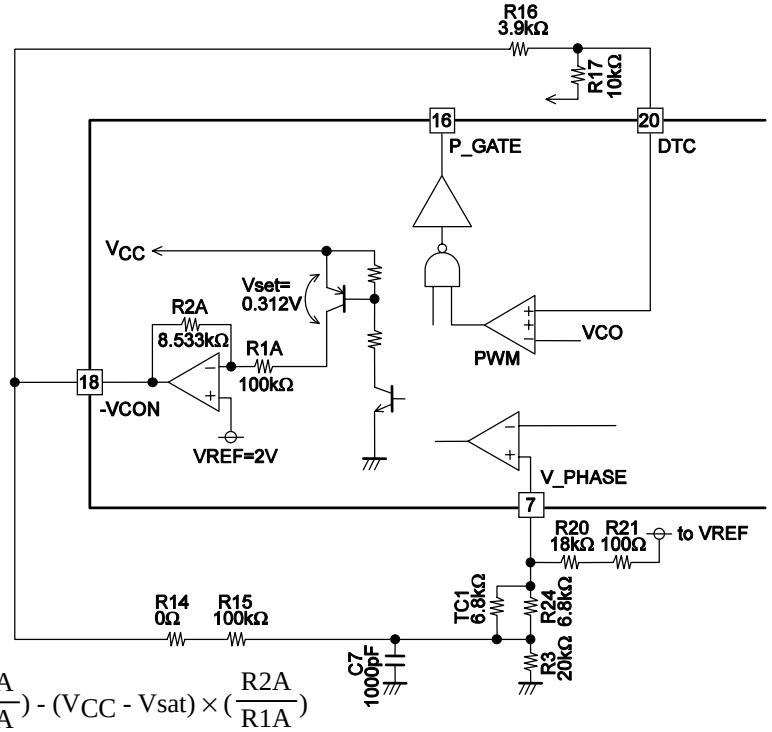


* The above graph is based on measurements for the independent IC.

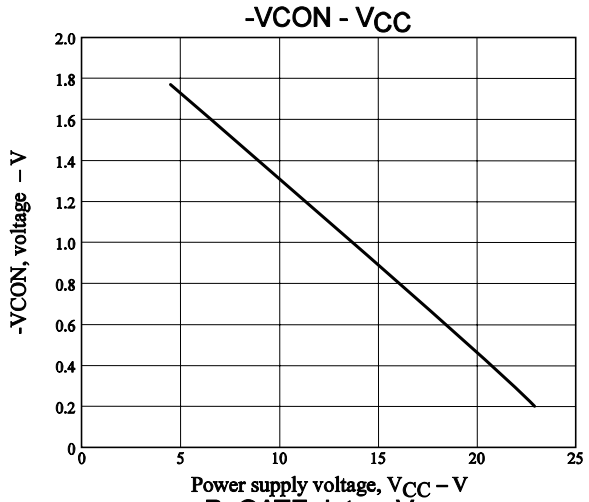
(7) –VCON and DTC pins

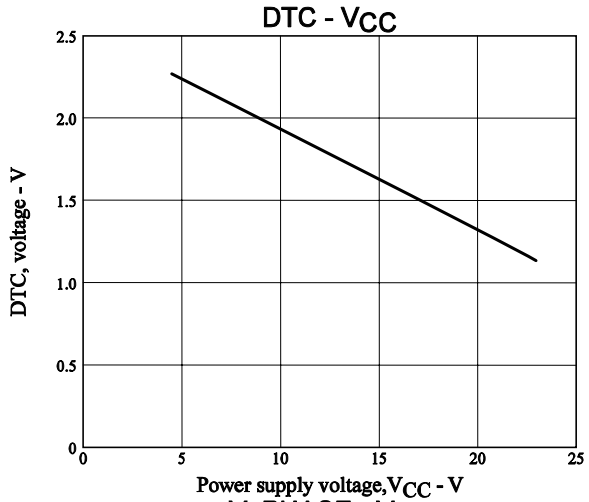
The –VCON pin output voltage is inversely proportional to V_{CC}. Using this output to create the DTC pin input voltage specifies a maximum duty dependent on V_{CC}. On the other hand, connecting this output to the V_PHASE pin input via the resistances R14 and R15 specifies a phase setting dependent on V_{CC}. (Eliminate resistances R14 and R15 if such a V_{CC}-dependent phase setting is not necessary.)

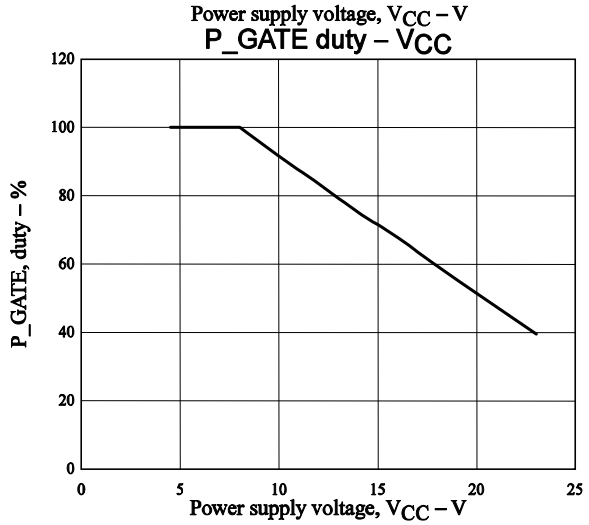
* The Specifications stipulate OP1 output electrical characteristics for the –VCON pin.

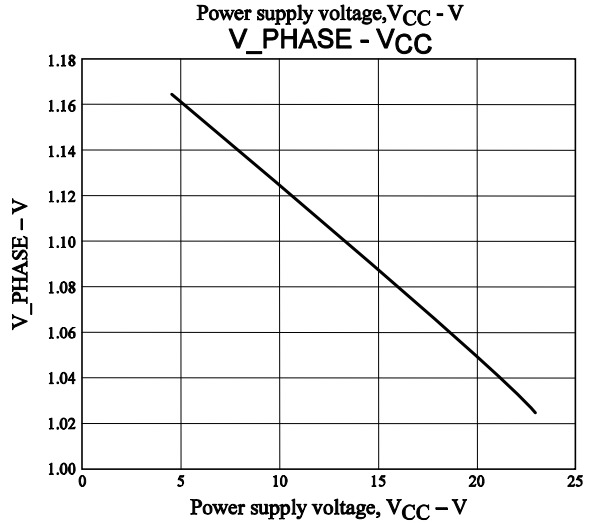


$$-VCON = VREF \times (1 + \frac{R2A}{R1A}) - (V_{CC} - Vsat) \times (\frac{R2A}{R1A})$$



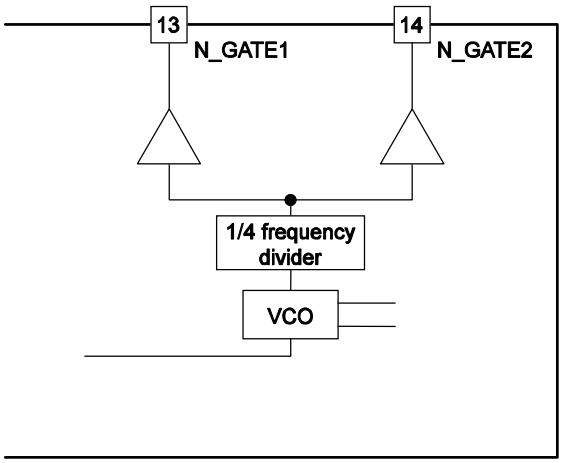






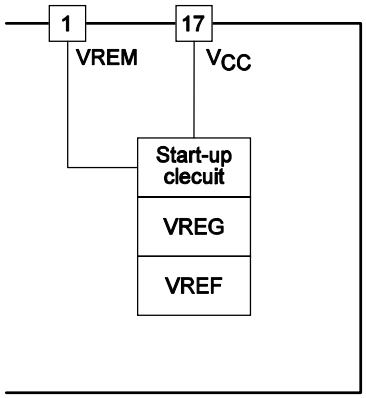
(8) N_GATE1 and N_GATE2 pins

These pins drive the n-channel MOSFET. The frequency is 1/4 the VCO frequency.



(9) VREM pin

This input turns the IC on and off. Turning the IC off reduces the current drain to 5μA or less.



(10) OVP

This is the over-voltage detection terminal.

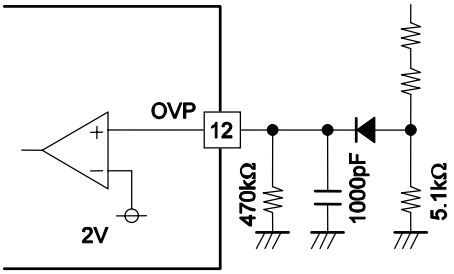
An OVP terminal gains a voltage that is divided by resistances. It works with threshold voltage 2V.

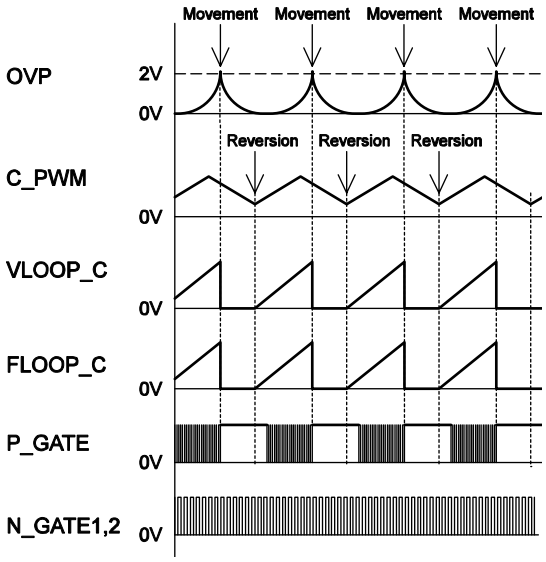
It becomes the condition of the table at the time of the movement.

Terminal	Condition
P_GATE	Hi
VLOOP_C	Low
FLOOP_C	Low
N_GATE1, 2	Drive

And once over-voltage protection works, it doesn't revert soon even if OVP is lower than 2V again.

It reverts after fixed time (the period of C_PWM) passes.





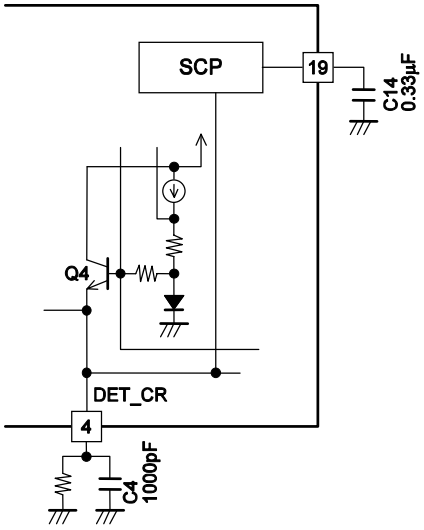
(11) SCP

CCFL electric current decrease by the CCFL opening and so on. And a charge begins in the condenser connected to SCP when the voltage of DET_CR was less than 0.26V.

Latch is set when the voltage of the condenser is more than 2V. The voltage of each terminal at this time becomes a table.

The charge of the condenser is stopped in the burst Duty again at the time of off period.

Terminal	Condition
P_GATE	Hi
VLOOP_C	Low
FLOOP_C	Low
N_GATE1, 2	Low



tscp = $3.03\times10^{6}\times$C14$\times$(100/burst duty) [S]

Example: tscp = 1 [S]

(At C14 = 0.33µF, burst duty = 100%)

(12) The polarity of the piezoelectric transformer

You must put logic with the transformer together, because a phase is controlled by comparing the common mode wave shape of N_GATE2 with the common mode wave shape of CCFL electric current.

Connect a piezoelectric transformer so that each wave shape may become relations like a figure.