Ordering number: ENN2301B

Monolithic Linear IC



**LA5665** 

# **Multifunction Multiple Voltage Regulator**

#### Overview

• Especially suited for use in micorcomputer-controlled tuners, receivers, preamplifiers and the like.

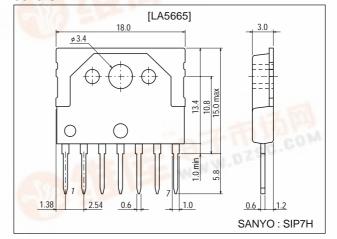
## **Features**

- Two independent voltage regulators contained in a single chip (15.5V/350mA, 5.6V/100mA).
- Reset circuit which delivers the reset signal on the positive transition, negative transition of the 5.6V output.
- Muting circuit which detects the 15.5V output and reset output to deliver the muting signal (We have the LA5666 whose detection function for reset, muting is provided on the input voltage side).

# **Package Dimensions**

unit:mm

3075-SIP7H



# **Specifications**

#### Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Input voltage	V <sub>IN</sub> 1, 2		35	V
Output current	I <sub>OUT</sub> 1, 2	Internal		Till 1
Allowable power dissipation	Pd max	IC only	1.6	W
Operating temperature	Topr		-30 to +80	°C
Storage temperature	Tstg	- ALD COS 14	-40 to +125	°C

### **Operating Conditions** at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit	
Input voltage	V <sub>IN</sub> 1	I <sub>OUT</sub> 1=200mA	19 to 35	V	
input voltage	V <sub>IN</sub> 2	I <sub>OUT</sub> 2=50mA	8.7 to 35	V	

#### **Operating Characteristics** at Ta = 25°C, $V_{IN}1=20$ V, $V_{IN}2=10$ V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	Offic
Quiescent current	I <sub>IN</sub> 1	4.0	1.8	2.8	3.8	mA
	I <sub>IN</sub> 2		3.8	5.8	7.8	mA
Output voltage	V <sub>O</sub> 1	I <sub>OUT</sub> 1=200mA	14.5	15.5	16.5	V
	V <sub>O</sub> 2	I <sub>OUT</sub> 2=50mA	5.1	5.6	6.2	V

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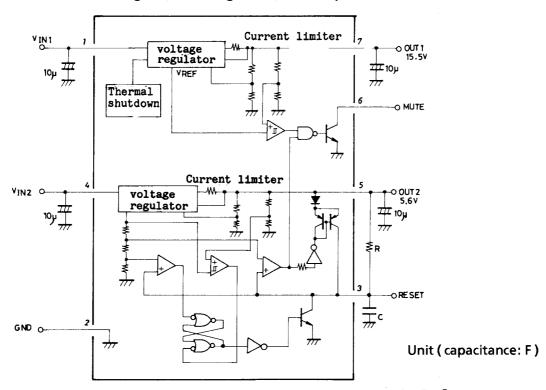
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Parameter	Symbol Conditions	Ratings			Unit	
Falametei		min	typ	max	Unit	
Line regulation	V <sub>ol</sub> 1	V <sub>IN</sub> 2=19 to 27V		6	20	mV
Line regulation	V <sub>ol</sub> 2	V <sub>IN</sub> 2=9 to 18V		2	20	mV
Load regulation	V <sub>old</sub> 1	I <sub>O</sub> =0 to 350mA		10	30	mV
Load regulation	V <sub>old</sub> 2	I <sub>O</sub> =0 to 100mA		2	20	mV
Pinnla raination	Rr1	f=120Hz, I <sub>O</sub> =200mA	56	65		dB
Ripple rejection	Rr2	f=120Hz, I <sub>O</sub> =50mA	60	75		dB
lanut output valtage dran	Vdr1	I <sub>O</sub> =200mA		1.6	2.5	V
Input-output voltage drop	Vdr2	I <sub>O</sub> =50mA		1.5	2.5	V
Reset detect voltage	٧ <sub>R</sub>	(Note 1)	4.9	5.1	5.5	V
Timer compare veltage	V <sub>C</sub> 1		1.0	1.2	1.4	V
Timer compare voltage	V <sub>C</sub> 2		0.06	0.13	0.18	V
Timer input bias current	I <sub>TB</sub>				250	nA
Muting detect voltage	٧M	(Note 2)	13.5	14.5	15.5	V
Muting output voltage	VOMUTE	I <sub>OMUTE</sub> =5mA		0.1	0.15	V

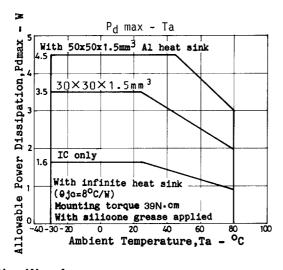
Note 1:  $V_R$  is the voltage of  $V_O$ 2 at the time reset is turned OFF. Note 2:  $V_M$  is the voltage of  $V_O$ 1 at the time muting is turned OFF.

## **Equivalent Circuit Block Diagram, Pin Assignment, and Peripheral Circuit**

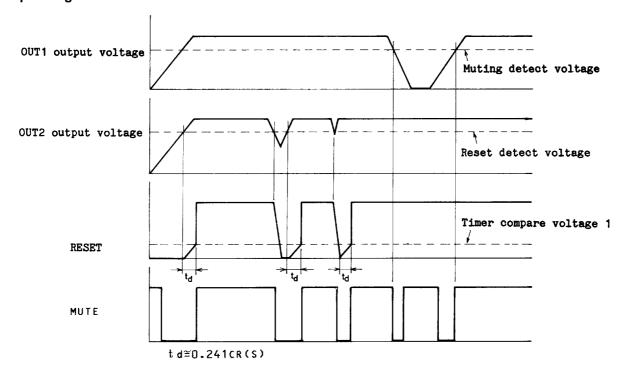


(Note) The reset delay time is set by R, C.

Pin No.	Name Description	
1	V <sub>IN</sub> 1	Input pin for 15.5V output line
2	GND	Ground
3	RESET	Reset delay time and output pin
4	V <sub>IN</sub> 2	Input pin for 5.6V output line
5	OUT2	5.6V output pin
6	MUTE	Muting signal output pin
7 OUT1		15.5V output pin



## **Operating Waveforms**



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