Ordering number : EN7742

SANYO Semiconductors
DATA SHEET

Monolithic Linear IC

LA6576 — 5-channel Driver for Compact Disk Applications

Overview

The LA6576 is a 5-channel driver for optical disc drives with a VREF switching function.

Features

- Power amplifier 5-channel built-in. (Bridge-connection (BTL): 4-channel, H bridge: 1-channel)
- I_O max 1A.
- Level shift circuit built-in (except H bridge).
- Mute circuit (output ON/OFF) built-in.
  (Operable with BTL AMP with CH1 to 4 and not operable for the H bridge of 5VREG)
- 5V regulator built-in (external PNP transistor).
- With VREF changeover function (H: external, L: internal).
- Overheat protection circuit (thermal shutdown) built-in.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		14	V
Maximum output current	I_O max	Each output for H bridge, channel 1 to 4	1	A
Maximum input voltage	VINB		13	V
Mute pin voltage	VMUTE		13	V
Allowable operation	Pd max	Independent IC	0.8	W
		Specified board*	2	W
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

*1 A circuit board for mounting (76.1mm×114.3mm×1.6mm, glass epoxy resin)

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		5.6 to 13	V

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Electrical Characteristics at $V_{CC}1 = V_{CC}2 = 8V$, VREF = 2.5V, Ta = 25°C, unless especially specified.

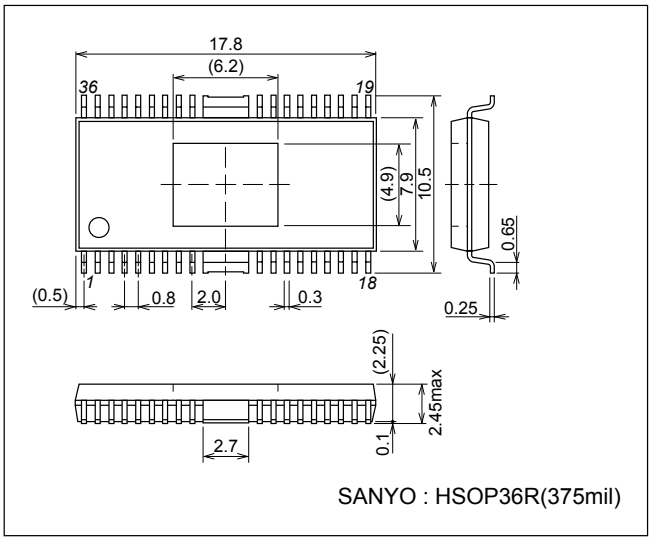
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
All blocks						
No-load current drain ON	I_{CC}-ON	BTL-AMP output ON, LOADING block OFF *1		30	50	mA
No-load current drain OFF	I_{CC}-OFF	All outputs OFF *1		10	15	mA
Thermal shutdown temperature	TSD	Design guarantee value	150	175	200	°C
VREF-AMP						
VREF-AMP offset voltage	VREF-OFFSET		-10		10	mV
VREF Input voltage range	VREF-IN		1		V_{CC}-1.5	V
VREF-OUT output current	I-VREF-OUT	CH1 input reference voltage	2	5		mA
BTL AMP Block (CH1 to CH4)						
Output offset voltage	VOFF	Voltage difference between outputs for BTL AMP, each channel. *2	-50		50	mV
Input voltage range	V_{IN}	Input voltage range for input for OP-AMP.	0		V_{CC}-1.5	V
Output voltage	V_O	Each voltage between V_O+ and V_O- when R_L = 8Ω. *3	5.7	6.2		V
Closed-circuit voltage gain	VG	Input and output gain. Input OP-AMP : BUFFER	3.6	4	4.4	deg
Slew rate	SR	AMP Independent Multiply 2 between outputs.		0.5		V/μs
MUTE ON voltage	VMUTE-ON	Output ON voltage, each MUTE *4	2			V
MUTE OFF voltage	VMUTE-OFF	Output OFF voltage, each MUTE *4			0.5	V
Input AMP Block (CH1 to CH4)						
Input voltage range	V_{IN}-OP		0		V_{CC}-1.5	V
Output current (SINK)	SINK-OP		2			mA
Output current (SOURCE)	SOURCE-OP	*5	300	500		μA
Output offset voltage	VOFF-OP		-10		10	mV
CH1 input changeover voltage 1	VSW-OP1	CH1 input AMP (B), external VREF select *6	2			V
CH1 input changeover voltage 2	VSW-OP2	CH1 input AMP (A), internal VREF select 6*			0.5	V
Loading Block (CH5, H bridge)						
Output voltage	V_O-LOAD	Between forward and reverse outputs, R_L =8Ω	5.7	6.5		V
Break output saturation voltage	VCE-BREAK	Output voltage at braking *8			0.3	V
Input low level	V_{IN}-L				1	V
Input high level	V_{IN}-H		2			V
Power Supply Block (PNP transistor: 2SB632K-use)						
5V supply output	V_{OUT}	I_O = 200mA	4.8	5.0	5.2	V
REG-IN SINK current	REG-IN-SINK	Base current to external PNP	5	10		mA
Line regulation	ΔVOLN	6V≤V_{CC}≤12V, I_O = 200mA		10	100	mV
Load regulation	ΔVOLD	5mA≤I_O≤200mA		10	100	mV

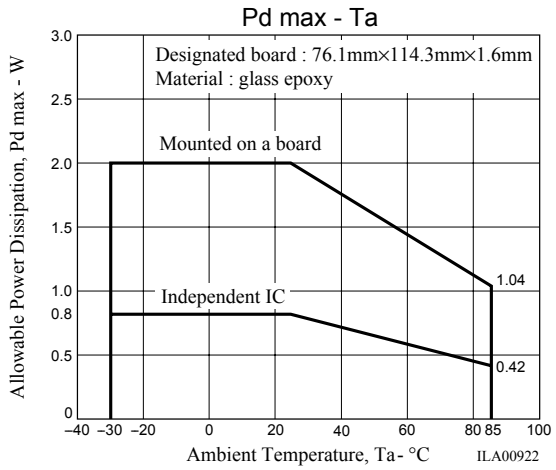
*1. Current dissipation that is a sum of $V_{CC}1$ and $V_{CC}2$ at no load.
*2. Input AMP is a BUFFER AMP.
*3. Voltage difference between both ends of load (8Ω). Output saturated.
*4. Output ON with MUTE: [H] and OFF with MUTE: [L] (HI impedance).
*5. The source of input OP-AMP is a constant current. As the 11kΩ resistance to the next stage is a load, pay due attention when setting the input OP-AMP gain.
*6. With V_{IN}1-SW: [L], the input AMP selects AMP-A while VREF selects internal VREF (≈2.5V).
With V_{IN}1-SW: [H], the input AMP selects AMP-B while VREF selects external VREF (≈2VREF-IN).
*7. Voltage of upper (SOURCE) + lower (SINK) sides. At forward/reverse, the output voltage is determined by subtracting this voltage from V_{CC}.
*8. Short (GND) brake used. SINK side output ON.
*9. 5VREG incorporates a drooping protection circuit and operated when the base current is 10mA (TYP).

Package Dimensions

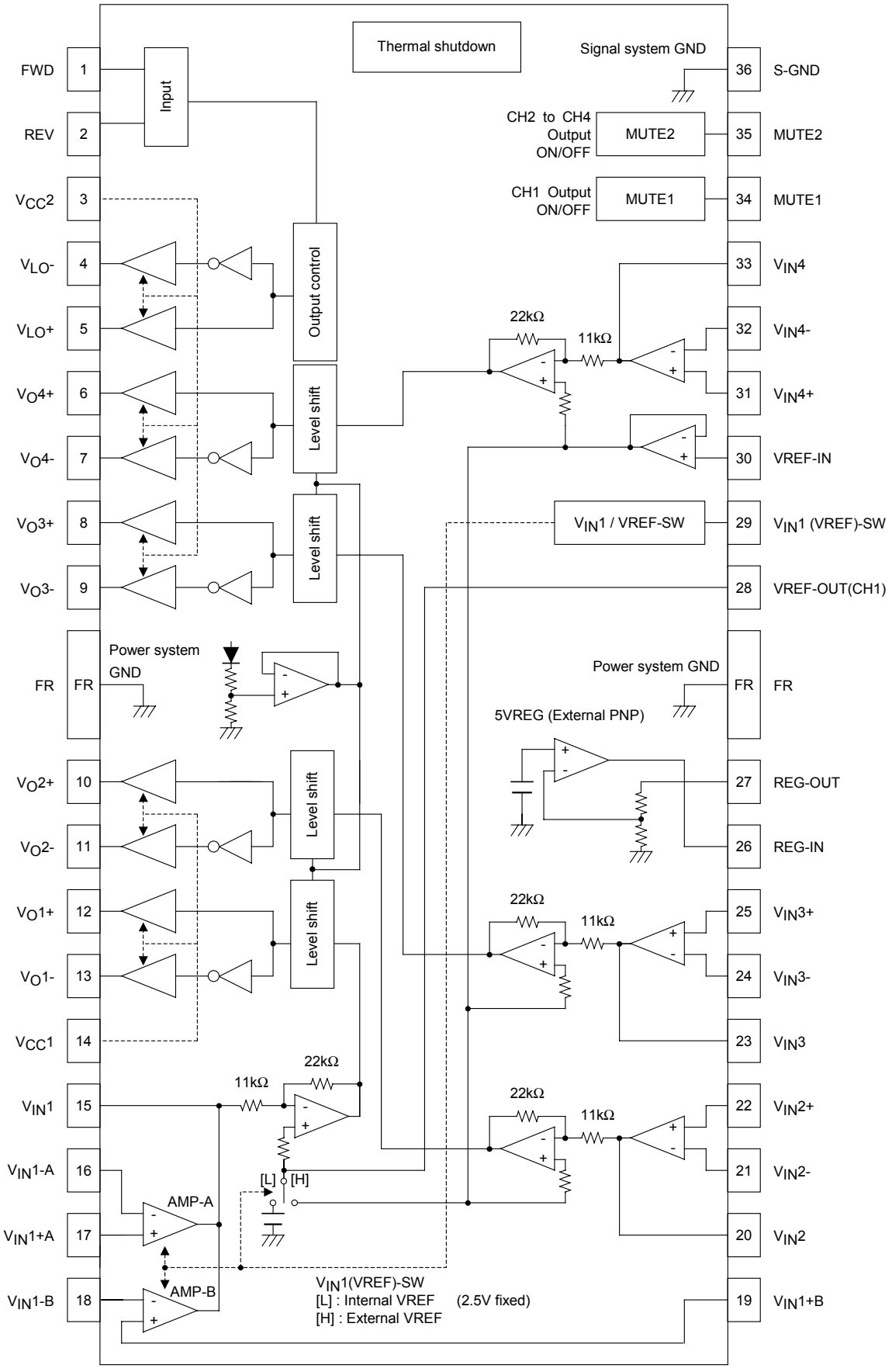
unit : mm

3251

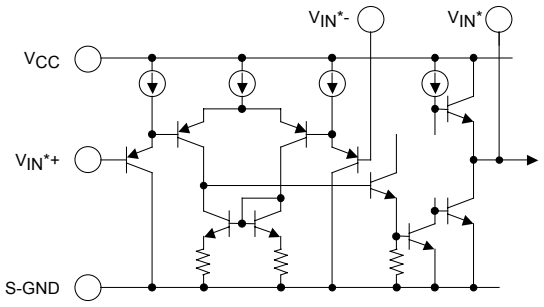
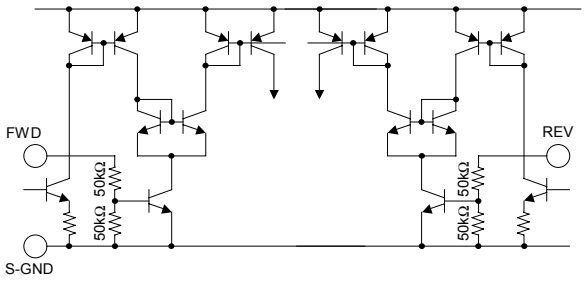
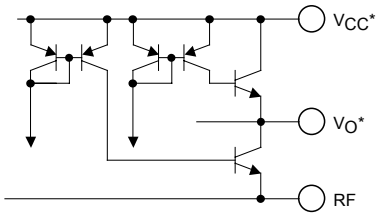
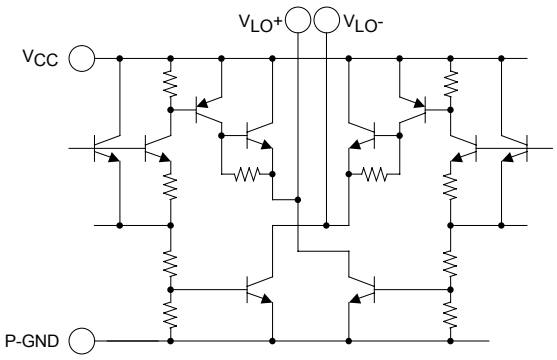
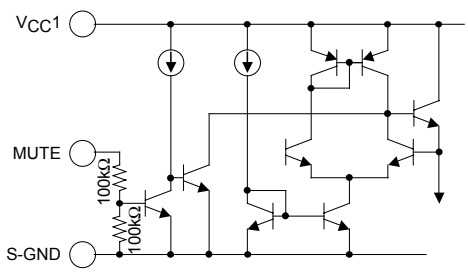




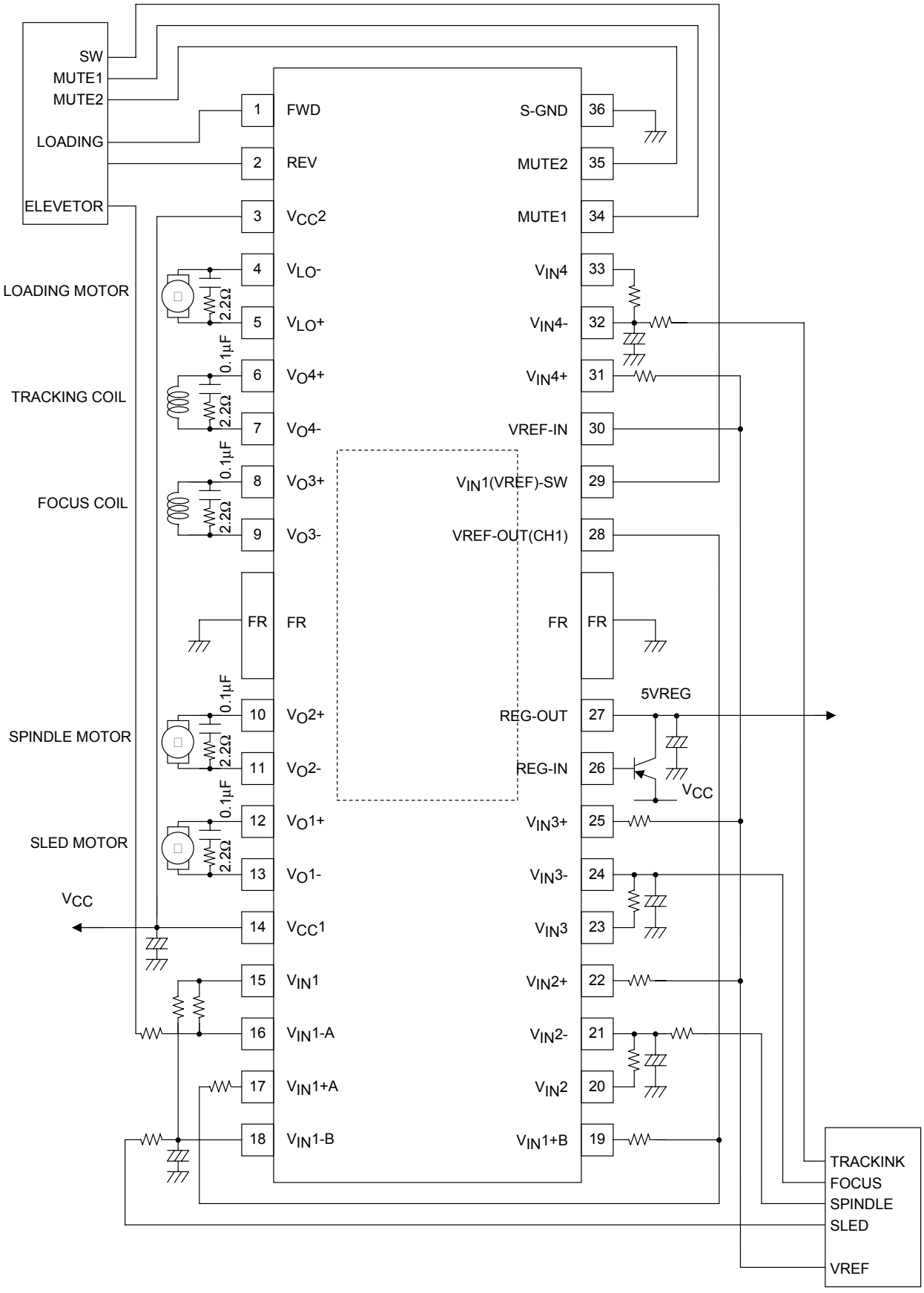
Block Diagram



Pin Description

Pin name	Pin name	Pin no.	Equivalent circuit	Pin explanation
Input (CH1 to 4)	$V_{IN}1$+A $V_{IN}1$+B $V_{IN}1$-A $V_{IN}1$-B $V_{IN}1$ $V_{IN}2$+ $V_{IN}2$- $V_{IN}2$ $V_{IN}3$+ $V_{IN}3$- $V_{IN}3$ $V_{IN}4$- $V_{IN}4$+ $V_{IN}4$	17 19 16 18 15 22 21 20 25 24 23 32 31 33		Input pin (CH1 to 4)
Input (H bridge)	FWD REV	1 2		Logic input pin. By combining H and L of this pin, any one of four modes (forward/reversed/brake/idling) can be selected.
Output (BTL-AMP)	V_O1+ V_O1- V_O2+ V_O2- V_O3+ V_O3- V_O4+ V_O4-	12 13 10 11 8 9 6 7		Output for channel 1 to 4.
Output (H bridge)	V_{LO}- V_{LO}+	4 5		H bridge (LOADING) output
MUTE	MUTE1 MUTE2	34 35		BTL AMP output, which turns ON/OFF the output for CH1 – CH4, MUTE: H Output ON MUTE: L Output OFF

Sample Application Circuit

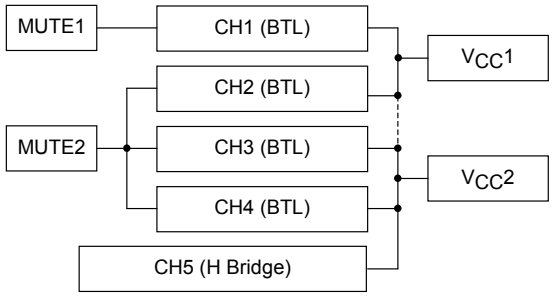


Truth Table (loading (H bridge) section)

FWD	REV	V_{LO}+	V_{LO}-	Loading output
L	L	OFF	OFF	OFF *1
	H	H	L	Forward
H	L	L	H	Reversed
	H	L	L	(Short) brake *2

*1 The output has a high impedance.
*2 At brake, the SINK side transistor is ON (short brake).
V_{LO}+ and V_{LO}- are approximately on the GND level.

Relation of MUTE and Power (V_{CC}*)



*Connect V_{CC}1 and V_{CC}2 externally.
(This is to minimize effects of voltage drop in internal and metal wirings.)

V_{IN}1 (VREF)-SW (CH1 input AMP selection and internal/external VREF selection function)

(Relation between input AMP (CH1 only) and VREF)

V_{IN}1-SW	Input AMP (CH1) state	VREF state
L	V_{IN}1-A (AMP-A)	Internal VREF (2.5V:TYP)
H	V_{IN}1-B (AMP-B)	External VREF