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| SANYO | No.4702 | LA7156 |
| | | Video and Audio Switch for PAL-SECAM 21-Pin Interface |

Overview

The LA7156 is a switching IC for use with the PAL and SECAM 21-pin connector interface. The LA7156 integrates video and audio switches in a single chip, and allows significant block reorganization and integration by providing function switching outputs with current limiters, 75 Ω video drivers, muting and other functions. The LA7156 provides a diverse set of functions, including support for single-wire serial bus control that allows complex logic to be handled by microprocessor software.

Functions and Features

- Three audio and three video switching systems
- Audio output and video decoder output muting function
- Video input sync chip clamp
- Two 6 dB video amplifier plus 75 Ω driver systems
- VPS decoder output
- FSS output with current limiting
- 5 V regulator built-in
- Serial control

Specifications

Absolute Maximum Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|---------------------|----------------|-------------|------|
| Maximum supply voltage | V _{CC max} | | 15 | V |
| Allowable power dissipation | P _{d max} | Ta \leq 65°C | 800 | mW |
| Operating temperature | T _{opr} | | -20 to +65 | °C |
| Storage temperature | T _{stg} | | -55 to +150 | °C |

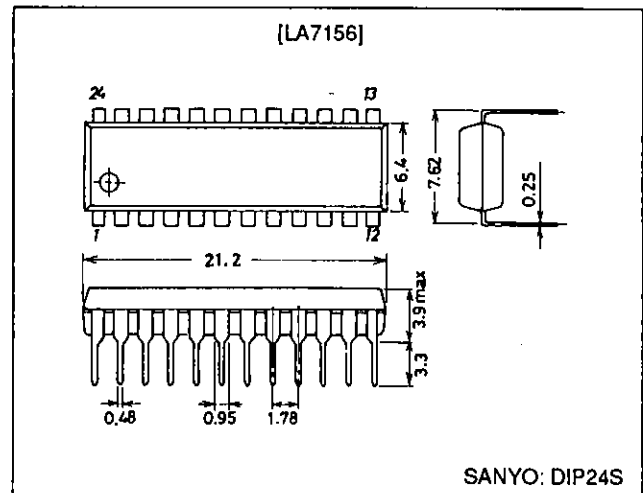
Operating Conditions at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|--------------------------------|--------------------|------------|---------|------|
| Recommended supply voltage | V _{CC} | | 9, 12 | V |
| Operating supply voltage range | V _{CC op} | | 8 to 13 | V |

Package Dimensions

unit: mm

3067-DIP24S



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Operating Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = 9\text{ V}$ and 12 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|-----------------------------------|------------------|---|------|------|----------|------------------|
| Current drain | I_{CC} | No input | 32 | 40 | 48 | mA |
| FSS output high level voltage 1 | VHFSS1 | $V_{CC} = 9\text{ V}$, load resistance: $10\text{ k}\Omega$ | 7.5 | 8.9 | 9.0 | V |
| FSS output low level voltage 1 | VLFS1 | $V_{CC} = 9\text{ V}$, load resistance: $10\text{ k}\Omega$ | | 0 | 0.5 | V |
| FSS output high level voltage 2 | VHFSS2 | $V_{CC} = 12\text{ V}$, load resistance: $10\text{ k}\Omega$ | 10.5 | 11.9 | 12.0 | V |
| FSS output low level voltage 2 | VLFS2 | $V_{CC} = 12\text{ V}$, load resistance: $10\text{ k}\Omega$ | | 0 | 0.5 | V |
| FSS output cutoff current 1 | $I_{CUTOFF1}$ | $V_{CC} = 9\text{ V}$, the outflow current when the FSS output is grounded | | 9.3 | 40.0 | mA |
| FSS output cutoff current 2 | $I_{CUTOFF2}$ | $V_{CC} = 12\text{ V}$, the outflow current when the FSS output is grounded | | 9.8 | 40.0 | mA |
| [Audio Switch Block] | | | | | | |
| Total harmonic distortion | THD | $V_{IN} = 1\text{ Vrms}$, $f = 1\text{ kHz}$, $R_{OUT} = \infty$ | | 0.02 | 1 | % |
| Maximum output voltage | $V_O\text{ max}$ | The output level when $f = 1\text{ kHz}$ and $\text{THD} = 2\%$ | 2 | 3 | | Vrms |
| Output noise voltage | V_{NO} | $R_g = 600\ \Omega$, DIN audio filter | | -100 | -90 | dBV |
| Voltage gain A | V_{GA} | The TP6 and TP8 output levels when $V_{IN} = 1\text{ Vrms}$ and $f = 1\text{ kHz}$ | 1.1 | 1.8 | 2.5 | dB |
| Interchannel crosstalk A | CTA | $V_{IN} = 1\text{ Vrms}$, $f = 1\text{ kHz}$ | | -90 | -70 | dB |
| Muting attenuation A | V_{muteA} | $V_{IN} = 1\text{ Vrms}$, $f = 1\text{ kHz}$ | | -90 | -70 | dB |
| Output offset voltage | V_{of} | The offset voltage when the switch has changed state | | 0 | 20 | mV |
| Input impedance A | $Z_{IN A}$ | | 40 | 50 | 60 | $\text{k}\Omega$ |
| [Video Switch Block] | | | | | | |
| Voltage gain V | V_{GV} | The TP2 and TP5 output levels when $V_{IN} = 1\text{ Vp-p}$ and $f = 4.43\text{ MHz}$ | -1 | 0 | +1 | dB |
| Frequency characteristics | V_f | $V_{IN} = 1\text{ Vp-p}$, $f = 100\text{ kHz}$ | -1.5 | -0.5 | +0.5 | dB |
| Second harmonic | H2 | $V_{IN} = 1\text{ Vp-p}$, $f = 4.43\text{ MHz}$ | | -45 | -40 | dB |
| Third harmonic | H3 | $V_{IN} = 1\text{ Vp-p}$, $f = 4.43\text{ MHz}$ | | -50 | -45 | dB |
| Interchannel crosstalk V | CTV | $V_{IN} = 1\text{ Vp-p}$, $f = 4.43\text{ MHz}$ | | -50 | -40 | dB |
| Muting attenuation V | V_{muteV} | $V_{IN} = 1\text{ Vp-p}$, $f = 4.43\text{ MHz}$ | | -50 | -40 | dB |
| Output voltage | V_{OUT} | The TP5 DC voltage with no input | | 0.7 | 1.0 | V |
| [Control Block] | | | | | | |
| Serial control input high level | V_{sh} | | 4 | | 5 | V |
| Serial control input middle level | V_{sm} | | 2 | | 3 | V |
| Serial control input low level | V_{sl} | | 0 | | 1 | V |
| Pin 2 input high level | V_{2H} | | 4 | | V_{CC} | V |
| Pin 2 input low level | V_{2L} | *1 | 0 | | 2 | V |
| Pin 20 input high level | V_{20H} | | 4 | | V_{CC} | V |
| Pin 20 input middle level | V_{20M} | *2 | 2 | | 3 | V |
| Pin 20 input low level | V_{20L} | | 0 | | 1 | V |
| Pin 7 output high level | V_{7H} | The TP9 DC voltage when SW3 is in the A position | 4.5 | 5.0 | 5.5 | V |
| Pin 7 output low level | V_{7L} | The TP9 DC voltage when SW3 is in the B position | 0 | | 1 | V |

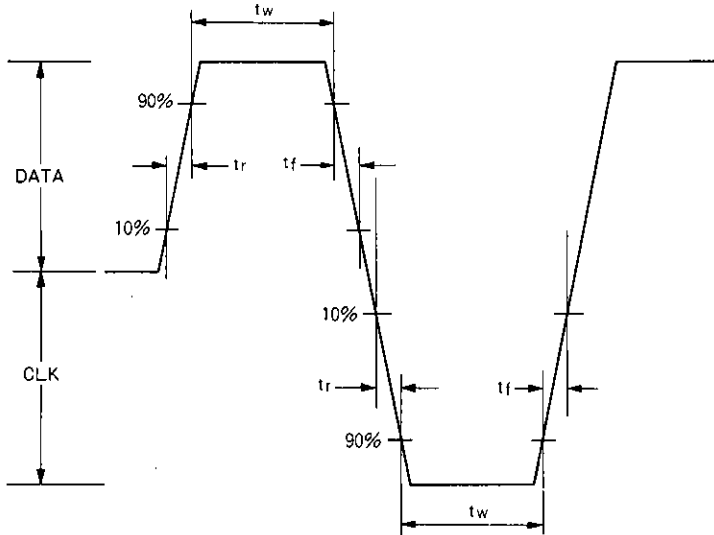
Note: In the operating characteristics listed above, characteristics items that do not differ between $V_{CC} = 9\text{ V}$ and 12 V are listed as the same item.

1. Forced to low when pin 2 is open.
2. Forced to the middle level when pin 20 is open.

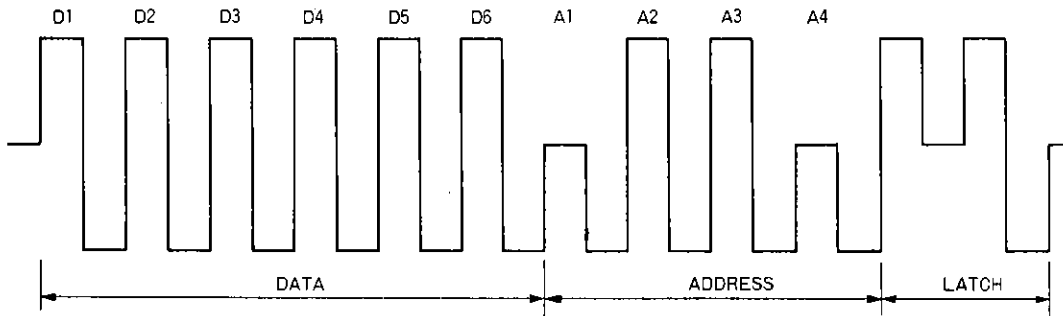
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Timing Characteristics

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---------------------------|--------|------------|-----|-----|-----|---------------|
| Minimum input pulse width | t_w | | 2 | | | μs |
| Rise time | t_r | | | | 20 | μs |
| Fall time | t_f | | | | 20 | μs |



Serial Control Input Specifications



LA7156 Command Address

| Address | A1 | A2 | A3 | A4 |
|---------|----|----|----|----|
| State | L | H | H | L |

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Switch Logic Values Table

The LA7156 provides the following switching control with control of pin 20.

1. Normal mode (when pin 20 is high)

In this mode, the LA7156 functions, including switching, FSS output and muting, can be controlled from the six bits of serial data transferred from the microprocessor. However, note that the video and audio system switch operate at the same time in this mode.

| DATA1 | | Switch state | Note | DATA4 | Switch state | Note |
|-------|-------|------------------|------|-------|------------------------------|------|
| H | | A.SW1-A, V.SW1-A | 1, 2 | H | A.SW3-A, V.SW3-A, pin 7 high | 1, 2 |
| L | | A.SW1-B, V.SW1-B | 1, 2 | L | A.SW3-B, V.SW3-B, pin 7 low | 1, 2 |
| DATA2 | DATA3 | Switch state | Note | DATA5 | FSS output state | Note |
| H | L | A.SW2-A, V.SW2-A | 1, 2 | H | Output high | |
| L | L | A.SW2-B, V.SW2-B | 1, 2 | L | Output low | |
| — | H | A.SW2-C, V.SW2-C | 1, 2 | DATA6 | Muted state | Note |
| | | | | H | Muted | |
| | | | | L | Mute released | |

Note: 1. All the audio switch and the video SW3 outputs are forcibly muted when DATA6 is high or in muting mode.
 2. A.SW indicates the audio system switches and V.SW indicates the video system switches.

2. Preset mode (when pin 20 is middle or low)

This mode uses the LA7156 internally set up logic and the six bits of data are allocated to the VCR operating states to allow the switch states to be changed.

Serial Data

| DATA No. | Item | H | L |
|----------|------------------|-----|--------|
| D1 | Power on/off | On | Off |
| D2 | VCR/TV | VCR | TV |
| D3 | Pay CH/Normal CH | Pay | Normal |
| D4 | EXT/Tuner | EXT | Tuner |
| D5 | PB/EE | PB | EE |
| D6 | Mute on/off | On | Off |

External Input Data

| Pin No. | Item | H | L |
|---------|------------|----------|--------|
| P2 | Decoder in | Scramble | Normal |

Truth Table

Pin 20: Open or Middle

| D1 | D2 | D3 | D4 | D5 | P2 | A.V.SW1 | A.V.SW2 | A.V.SW3 | FSS out | Pin 7 out |
|----|----|----|----|----|----|---------|---------|---------|---------|-----------|
| L | — | — | — | — | H | A | C | A | L | H |
| L | — | — | — | — | L | A | C | A | L | H |
| H | L | — | L | L | H | A | A | A | L | H |
| H | L | — | L | L | L | A | C | A | L | H |
| H | H | — | L | L | H | A | A | A | H | H |
| H | H | — | L | L | L | A | C | A | H | H |
| H | L | — | H | L | H | A | B | A | L | H |
| H | L | — | H | L | L | A | B | A | L | H |
| H | H | — | H | L | H | A | B | A | H | H |
| H | H | — | H | L | L | A | B | A | H | H |
| H | — | — | — | H | H | A | * | A | H | H |
| H | — | — | — | H | L | A | * | A | H | H |

Note: The previous state is retained even if another switch is changed.

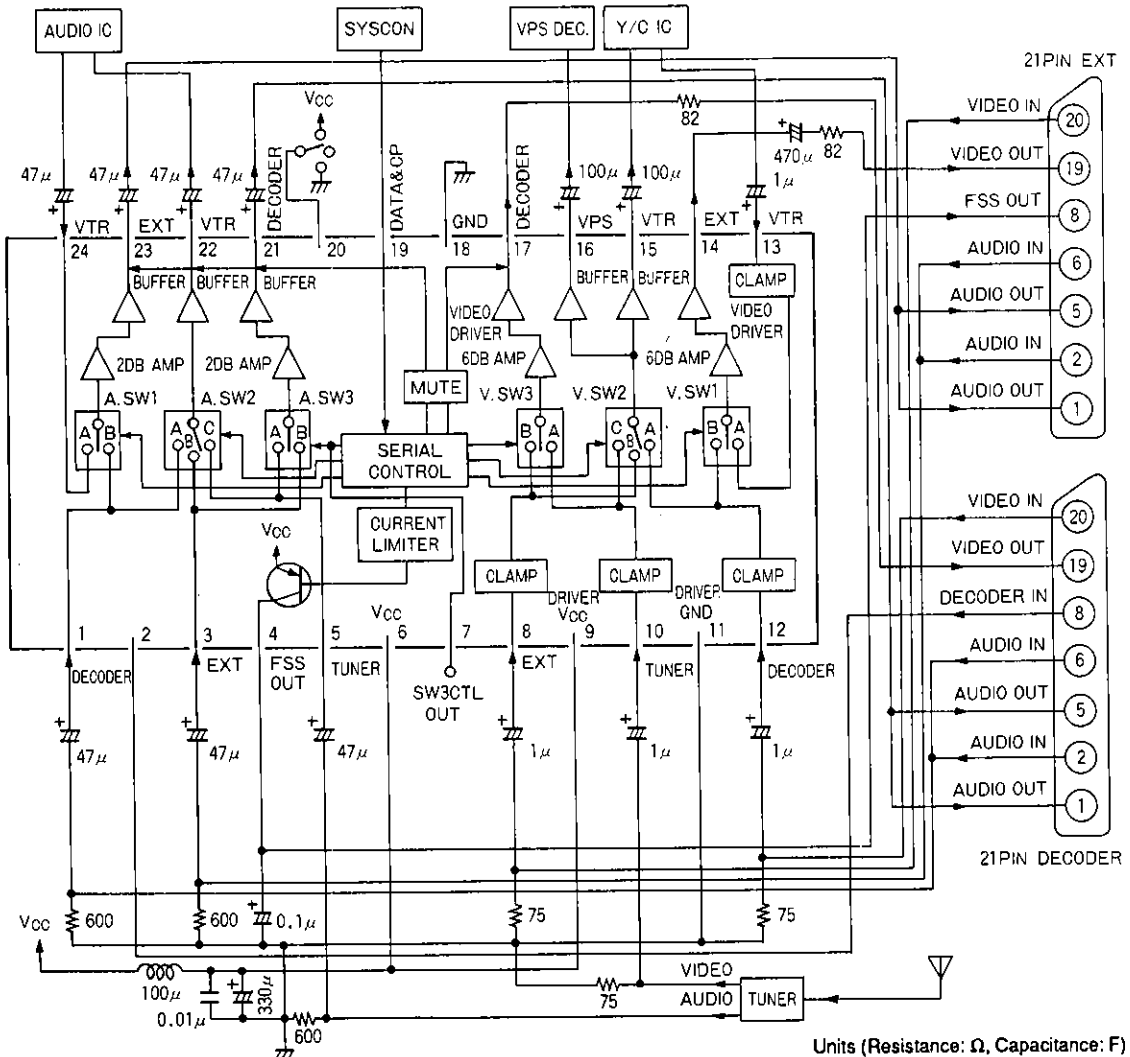
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Pin 20: Low

| D1 | D2 | D3 | D4 | D5 | P2 | A.V.SW1 | A.V.SW2 | A.V.SW3 | FSS out | Pin 7 out |
|----|----|----|----|----|----|---------|---------|---------|---------|-----------|
| L | — | — | — | — | H | B | A | B | H | L |
| L | — | — | — | — | L | B | A | B | L | L |
| H | L | L | L | L | H | B | C | B | H | L |
| H | L | L | L | L | L | A | C | B | L | L |
| H | H | L | L | L | H | A | C | A | H | H |
| H | H | L | L | L | L | A | C | A | H | H |
| H | L | H | L | L | H | A | A | A | L | H |
| H | L | H | L | L | L | A | C | A | L | H |
| H | H | H | L | L | H | A | A | A | H | H |
| H | H | H | L | L | L | A | C | A | H | H |
| H | L | — | H | L | H | A | A | B | H | L |
| H | L | — | H | L | L | A | B | B | L | L |
| H | H | — | H | L | H | A | A | B | H | L |
| H | H | — | H | L | L | A | B | B | H | L |
| H | — | — | — | H | H | A | * | * | H | * |
| H | — | — | — | H | L | A | * | * | H | * |

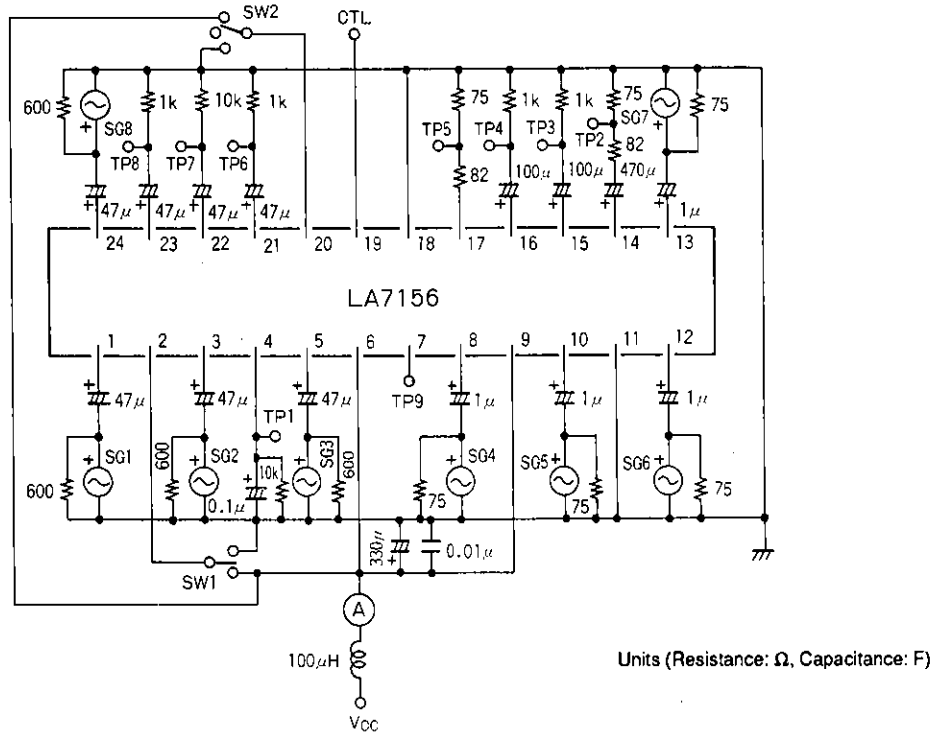
Note: The previous state is retained even if another switch is changed.

Block Diagram and Recommended Circuit Diagram



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Test Circuit



Input and Output Pin Circuit Diagrams

Unit (Resistance: Ω, Current source: A)

| Pin No. | Symbol | I/O circuit | DC voltage | Note |
|-------------------|--|-------------|------------------------------|------|
| 1 3 5 24 | A_{IN1} A_{IN2} A_{IN3} A_{IN4} | | $\frac{1}{2} V_{CC} + 0.7 V$ | |
| 2 | DEC IN | | | |
| 4 | FSS OUT | | $V_{CC} - 0.2 V$ | |
| 6 | V_{CC} | | | |

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Unit (Resistance: Ω, Current source: A)

| Pin No. | Symbol | I/O circuit | DC voltage | Note |
|---------------------|--|-------------|--------------------|---------------------------------|
| 7 | SW3 CTL OUT | | H: 5.0 V L: 0 V | |
| 8 10 12 13 | V _{IN1} V _{IN2} V _{IN3} V _{IN4} | | 2.5 V | |
| 9 | DRIVER V _{CC} | | | |
| 11 | DRIVER GND | | | |
| 14 | V _{OUT1} | | 1.6 V | External connection |
| 17 | V _{OUT2} | | | |
| 15 | V _{OUT3} | | 1.6 V | Signal processing IC connection |
| 16 | V _{OUT4} | | 1.6 V | Signal processing IC connection |
| 18 | GND | | | |

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| Pin No. | Symbol | I/O circuit | DC voltage | Note |
|---------|--------------------|-------------|---------------------|---------------------------------|
| 19 | D/C IN | | 2.5 V | |
| 20 | MODE CTL IN | | 2.5 V | |
| 21 | A _{OUT} 1 | | 1/2 V _{CC} | External connection |
| 23 | A _{OUT} 2 | | | |
| 22 | A _{OUT} 3 | | 1/2 V _{CC} | Signal processing IC connection |

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