Ordering number : EN*A1283

Preliminary

SANYO Semiconductors
DATA SHEET

Monolithic Linear IC

LA74322LP — Audio I/O Interface for Cell Phone

Overview

The LA74322LP is an audio I/O interface IC for cell phones that integrates, on a single chip, amplifiers for a monaural speaker, EVR stereo headphone, internal and external microphones, and a receiver speaker.

Features

- INT & EXT MIC amplifiers selectable (MIC power supply built-in)
- ALC amplifier (ALC level: 3 levels selectable)
- Base band/audio source input selector switch
- ALC (through switch, ALC level: 4 levels selectable)
- EVR stereo headphone amplifier
- Monaural speaker amplifier
- Receiver speaker amplifier (mono) standby control
- I^2C bus supported (first mode)

Specifications

Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		5.5	V
Allowable power dissipation	Pd max	Ta≤70°C, Mounted on a specified board *1	TBD	mW
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-55 to +150	°C

*1: Mounted on a specified board: TBD

SANYO Semiconductor Co., Ltd.
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage ($V_{CC}A$)	$V_{CC}A$		3.0	V
Recommended supply voltage ($V_{CC}HP$)	$V_{CC}HP$		3.0	V
Recommended supply voltage ($V_{CC}SP$)	$V_{CC}SP$		3.6	V
Allowable operating voltage range ($V_{CC}A$)	$V_{CC}Aop$		2.7 to 3.6	V
Allowable operating voltage range ($V_{CC}HP$)	$V_{CC}HPop$		2.7 to 3.6	V
Allowable operating voltage range ($V_{CC}SP$)	$V_{CC}SPop$	*2	2.7 to 5.0	V

*2: Take care not to exceed Pd max.

Electrical Characteristics at Ta=25°C, $V_{CC}A$=$V_{CC}HP$=3.0V, $V_{CC}SP$=5.0V, f=1kHz, ALC1 LEVEL=-17dBV MODE, ALC2 LEVEL=-11dBV MODE

No.	Parameter	Symbol	Conditions	Ratings			Unit
				min	typ	max	
Circuit current							
1	$V_{CC}A$ current dissipation	$I_{CC}A$	$V_{CC}A$=3.0V, MIC1 ON, audio source system (stereo) OFF, receiver system ON		9.5		mA
2	$V_{CC}A$ STANDBY current dissipation	$I_{CC}AS$	$V_{CC}A$=3.0V, 0V applied to STANBDY pin			10	μA
3	$V_{CC}HP$ current dissipation 1	$I_{CC}HP1$	$V_{CC}HP$=3.0V: Receiver SPK AMP POWER SAVE MODE		8.5		mA
4	$V_{CC}HP$ current dissipation 2	$I_{CC}HP2$	$V_{CC}HP$=3.0V: H/P AMP POWER SAVE MODE		2.7		mA
5	$V_{CC}HP$ STANDBY current dissipation	$I_{CC}HPS$	$V_{CC}HP$=3.0V, 0V applied to STANBDY pin			10	μA
6	$V_{CC}SP$ current dissipation 1	$I_{CC}SP1$	$V_{CC}SP$=5.0V: SPK POWER ON MODE		6.5		mA
7	$V_{CC}SP$ current dissipation 2	$I_{CC}SP2$	$V_{CC}SP$=5.0V: SPK POWER SAVE MODE		0.3		mA
8	$V_{CC}SP$ STANDBY current dissipation	$I_{CC}SPS$	$V_{CC}SP$=5.0V, 0V applied to STANBDY pin			10	μA
MIC output system							
9	INT MIC voltage gain	VGIMIC	INT MIC input, V_{IN}=-29dBV		10		dB
10	INT MIC output distortion	HDIMIC	INT MIC input, V_{IN}=-29dBV, THD: from 2nd to 5th harmonic		0.03		%
11	INT MIC output noise voltage	VNIMIC	INT MIC no input, JIS-A Filter		-100		dBV
12	INT MIC maximum input level	VMIMIC	INT MIC input, INT MIC input level at which up to 5th order distortions of MIC output are reduced to 3% or less			-20	dBV
13	INT MIC supply voltage	VVIMIC	At 6.2kΩ load		1.7		V
14	EXT MIC voltage gain	VGEMIC	EXT MIC input, V_{IN}=-29dBV		10		dB
15	EXT MIC output distortion	HDEMIC	EXT MIC input, V_{IN}=-29dBV, THD: from 2nd to 5th harmonic		0.03		%
16	EXT MIC output noise voltage	VNEMIC	EXT MIC no input, JIS-A Filter		-100		dBV
17	EXT MIC maximum input level	VMEMIC	EXT MIC input, EXT MIC input level at which up to 5th order distortions of MIC output are reduced to 3% or less			-20	dBV
18	EXT MIC supply voltage	VVEMIC	At 6.2kΩ load		1.7		V
REC output system: ALC1 level=-17dBV mode							
19	REC reference output level	VOREC	ALC1 input, V_{IN}=-40dBV		-16.5		dBV
20	REC reference output distortion	HDREC	ALC1 input, V_{IN}=-40dBV, THD: from 2nd to 5th harmonic		0.03		%
21	ALC1 level characteristics	VOALC1	ALC1 input, V_{IN}=-14dBV (reference+26dB)		-10		dBV
22	ALC1 distortion characteristics	VDALC1	ALC1 input, V_{IN}=-14dBV (reference+26dB), THD: from 2nd to 5th harmonic		0.3		%
23	REC output noise voltage	VNOR	ALC1 no input, JIS-A Filter		-83		dBV
24	ALC1 maximum input level	VMXALC	ALC1 input, ALC1 input level at which up to 5th order distortions of REC output are reduced to 3% or less			-10	dBV

Continued on next page.

Continued from preceding page.

No.	Parameter	Symbol	Conditions	Ratings			unit
				min	typ	max	
EVR output system: ALC2 level=-11dBV mode							
25	EVR reference output level 1 (V_Ol=Max)	VOEVR1	Audio source pin input, V_{IN}=-25dBV, EVR=Max		-17.3		dBV
26	EVR reference output distortion	HDEVR	Audio source pin input, V_{IN}=-25dBV, EVR=Max, THD: from 2nd to 5th harmonic		0.003		%
27	EVR reference output level 2 (V_Ol=Typ)	VOEVR2	Audio source pin input, V_{IN}=-25dBV, EVR=Typ (5Bit: 11011)		-22.5		dBV
28	EVR reference output level 3 (V_Ol=Min)	VOEVR3	Audio source pin input, V_{IN}=-25dBV, EVR=Min, JIS-A Filter		-96		dBV
29	EVR maximum input level	VMXEVR	ALC2=Through MODE, audio source input level at which up to 5th order distortions of EVR output are reduced to 3% or less l			-3	dBV
H/P output system: Measured at HP load = 16Ω, ALC2=Through mode							
30	H/P reference output level	VOHP	Base band input, V_{IN}=-11dBV, EVR=Max		-19		dBV
31	H/P reference output distortion	HDHP	Base band input, V_{IN}=-11dBV, THD: from 2nd to 5th harmonic		0.1		%
32	H/P output noise voltage	VNHP	No base band input, EVR=Max, JIS-A Filter		-100		dBV
33	H/P maximum input level	VMXHP	Base band input, base band input level at which up to 5th order distortions of H/P output are reduced to 3% or less			-10	dBV
SPK output system: Measured at SPK load = 8Ω, ALC2 level=-11dBV mode							
34	SPK reference output level	VOSPK	Audio source pin input, V_{IN}=-30dBV, V_Ol=Max		-4		dBV
35	SPK reference output distortion	VDSPK	Audio source pin input, V_{IN}=-30dBV, V_Ol=Max, THD: from 2nd to 5th harmonic		0.9		%
36	SPK output noise voltage	VNSPK	No input at audio source pin, EVR=Max, JIS-A Filter		-70		dBV
37	SPK maximum output power	VMXSPK	Audio source pin input, SPK output power at which up to 5th order distortions of SPK output are reduced to 3% or less, ALC2=Through MODE		1000		mW
38	SPK ALC level 1	VOSPK1	Audio source pin input, V_{IN}=-10dBV, V_Ol=Max, LC2=-13dBV MODE		4.5		dBV
39	SPK ALC level 2	VOSPK2	Audio source pin input, V_{IN}=-10dBV, V_Ol=Max, ALC2=-12dBV MODE		5.5		dBV
40	SPK ALC level 3	VOSPK3	Audio source pin input, V_{IN}=-10dBV, V_Ol=Max, ALC2=-11dBV MODE		6.4		dBV
41	SPK ALC level 4	VOSPK4	Audio source pin input, V_{IN}=-10dBV, V_Ol=Max, ALC2=-10.5dBV MODE		7		dBV
Receiver SPK output system: Measured at SPK load = 32Ω							
42	Receiver SPK reference output level 1 (V_Ol=Max)	VORSP1	Base band input, V_{IN}=-22dBV, V_Ol=Max		-4		dBV
43	Receiver SPK reference output distortion	VDRSP	Base band input, V_{IN}=-22dBV, V_Ol=Max, THD: from 2nd to 5th harmonic		0.9		%
44	Receiver SPK reference output level 2 (V_Ol=Typ)	VORSP2	Base band input, V_{IN}=-22dBV, V_Ol=Typ (5Bit: 11011)		-10		dBV
45	EVR reference output level 3 (V_Ol=Min)	VORSP3	Base band input, V_{IN}=-22dBV, EVR=Min, JIS-A Filter		-80		dBV
46	Receiver SPK output noise voltage	VNRSP	Base band no input, EVR=Max, JIS-A Filter		-80		dBV
47	Receiver SPK maximum output power	VMXRSP	Base band input, SPK output power at which up to 5th order distortions of SPK output are reduced to 3% or less		110		mW
Control system							
48	Serial CLOCK frequency	FCLK	I^2C bus first mode			400	kHz
49	Serial input LOW level	SERLO		0		0.6	V
50	Serial input HIGH level	SERHI		2.4		3.5	V

Electrical Characteristic: Serial Communication Condition Table

No.	Symbol	Address(0 1)								Address(0 2)								Address(0 3)								Address(0 4)							
		D8	D7	D6	D5	D4	D3	D2	D1	D8	D7	D6	D5	D4	D3	D2	D1	D8	D7	D6	D5	D4	D3	D2	D1	D8	D7	D6	D5	D4	D3	D2	D1
1	ICCA	0	0	1	0	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
2	ICCAS	0	0	1	0	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
3	ICCHP1	1	1	1	1	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0
4	ICCHP2	1	1	1	1	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
5	ICCHPS	1	1	1	1	0	0	0	0	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
6	ICCSP1	1	1	1	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0
7	ICCSP2	1	1	1	1	0	0	1	1	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0
8	ICCSPS	1	1	1	1	0	0	1	1	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0
9	VGIMIC	0	0	1	0	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0
10	HDIMIC	0	0	1	0	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0
11	VNIMIC	0	0	1	0	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0
12	VMIMIC	0	0	1	0	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0
13	VVIMIC	0	0	1	0	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0
14	VGEMIC	0	1	1	0	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0
15	HDEMIC	0	1	1	0	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0
16	VNEMIC	0	1	1	0	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0
17	VMEMIC	0	1	1	0	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0
18	VVEMIC	0	1	1	0	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0
19	VOREC	1	1	1	0	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0
20	HDREC	1	1	1	0	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0
21	VOALC1	1	1	1	0	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0
22	VDALC1	1	1	1	0	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0
23	VNOR	1	1	1	0	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0
24	VMXALC	1	1	1	0	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0
25	VOEVR1	1	1	1	1	0	0	1	1	0	0	1	0	0	0	1	1	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0
26	HDEVR	1	1	1	1	0	0	1	1	0	0	1	0	0	0	1	1	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0
27	VOEVR2	1	1	1	1	0	0	1	1	0	0	1	0	0	0	1	1	0	0	0	1	1	0	1	1	1	1	1	0	0	0	0	0
28	VOEVR3	1	1	1	1	0	0	1	1	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0
29	VMXEVR	1	1	1	1	0	0	1	1	0	0	1	0	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0
30	VOHP	1	1	1	1	0	0	0	0	1	1	1	0	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0
31	HDHP	1	1	1	1	0	0	0	0	1	1	1	0	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0
32	VNHP	1	1	1	1	0	0	0	0	1	1	1	0	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0
33	VMXHP	1	1	1	1	0	0	0	0	1	1	1	0	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0
34	VOSPK	1	1	1	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0
35	VDSPK	1	1	1	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0
36	VNSPK	1	1	1	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0
37	VMXSPK	1	1	1	1	0	0	1	1	0	0	1	0	1	1	1	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0
38	VOSPK1	1	1	1	1	0	0	1	1	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0
39	VOSPK2	1	1	1	1	0	0	1	1	0	0	0	1	0	0	1	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0
40	VOSPK3	1	1	1	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0
41	VOSPK4	1	1	1	1	0	0	1	1	0	0	1	1	0	0	1	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0
42	VORSP1	1	1	1	1	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1
43	VDRSP	1	1	1	1	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1
44	VORSP2	1	1	1	1	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	1	1	0	1	1
45	VORSP3	1	1	1	1	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
46	VNRSP	1	1	1	1	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1
47	VMXRSP	1	1	1	1	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1

↑ It is SW of Lch SPK setting.
Here always sets “1” = OFF.

Serial Data Specification (I^2C bus communication)

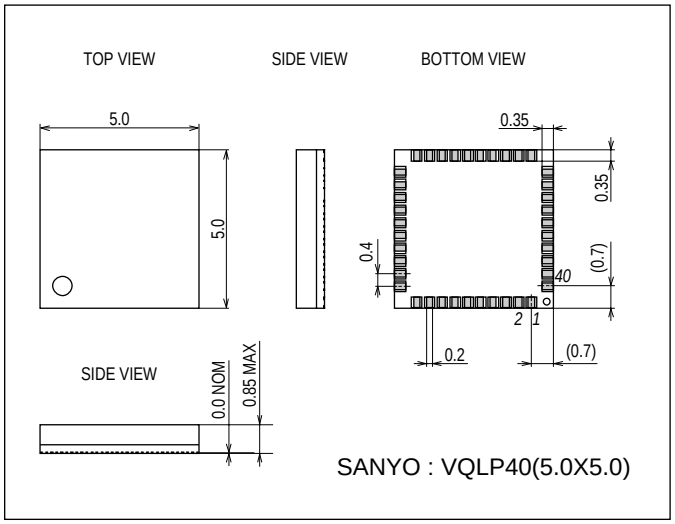
[Slave Address: 1 1 1 0 1 0 0 0]

Data byte (Underline is initial setting)

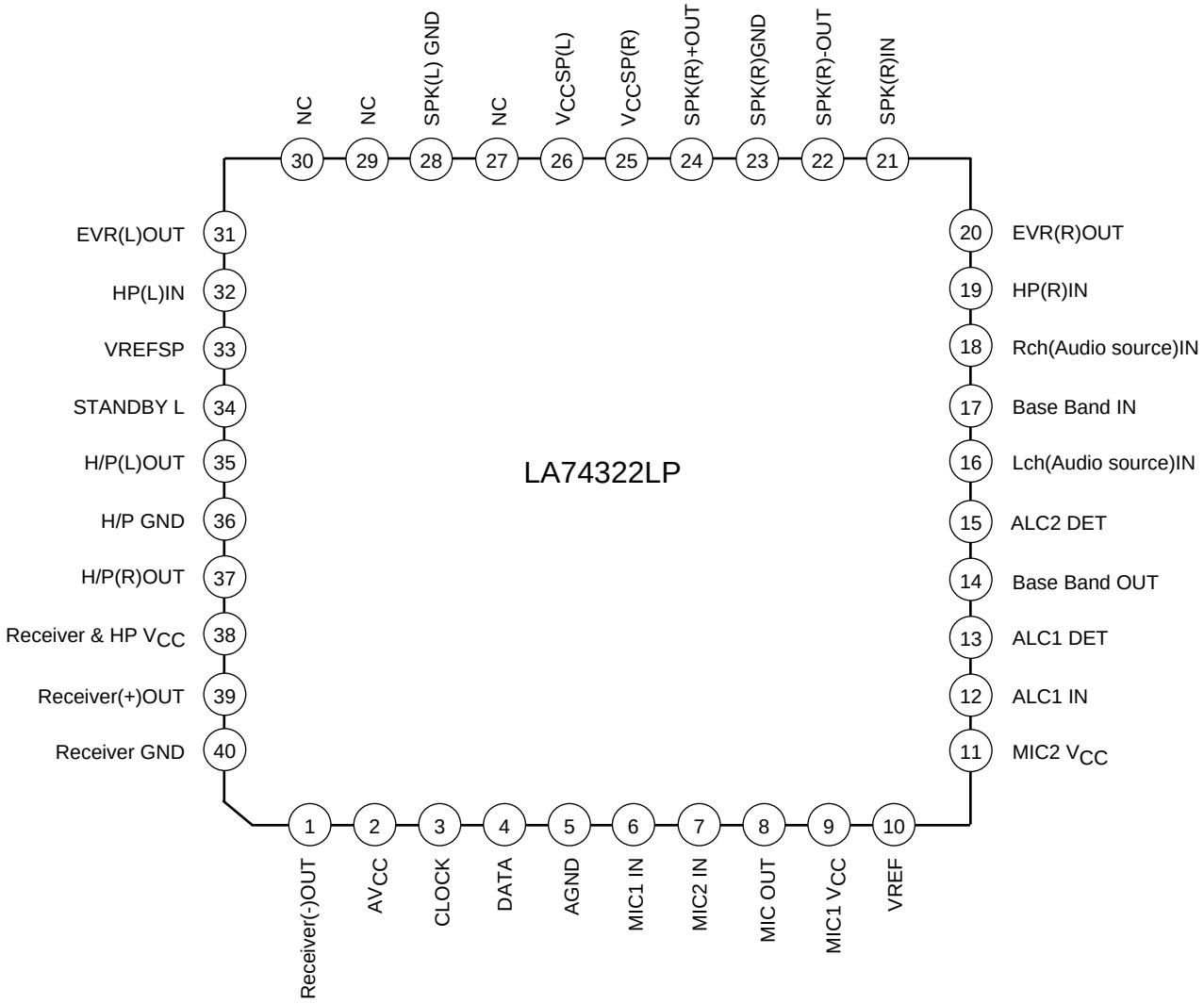
Address	MSB D8	D7	D6	D5	D4	D3	D2	LSB D1
(0 1) 00000001	MIC1 & 2 Power Save CTL MIC1 or 2 Input Select		ALC1 & REC AMP Power Save CTL ALC1 LEVEL=-21/-19/-17dBV CTL		ALC1 DET Discharge CTL	ALC2 DET Discharge CTL	Lch H/P Power Save CTL	Rch H/P Power Save CTL
	D8,D7	0,0 0,1 1,0 1,1	D6,D5	0,0 0,1 1,0 1,1	D4	D3	D2	D1
	MIC1	ON OFF OFF OFF	-21dBV	ON - - -	ALC1 DET discharge	ALC2 DET discharge	Lch H/P	Rch H/P
	MIC2	OFF ON OFF OFF	-19dBV	- ON - -				
			-17dBV	- - ON -				
			OFF	- - - ON				
(0 2) 00000010	Sound source & Base Band (B.B.) Input Select		ALC2 LEVEL =-13/-12/-11/-10.5dBV CTL		Lch ALC2 CTL Power Save & Through SW	Rch ALC2 CTL Power Save & Through SW	Lch Speaker Power Save CTL	Rch Speaker Power Save CTL
	D8,D7	0,0 0,1 1,0 1,1	D6,D5	0,0 0,1 1,0 1,1	D4	D3	D2	D1
	Lch Input SW	ON ON OFF OFF	-13dBV	ON - - -	ALC2	ALC2	Lch SPK Power	Rch SPK Power
	Rch Input SW	ON OFF ON OFF	-12dBV	- ON - -	Through SW	Through SW	ON OFF	ON OFF
	B.B. input SW	OFF OFF OFF ON	-11dBV	- - ON -			*Note Please set OFF.	
			-10.5dBV	- - - ON				
(0 3) 00000011	VREF Charge CTL	Lch EVR Power Save CTL	Rch EVR Power Save CTL		EVR Setting (Sound source & Base Band) 5bit			
	D8 0 1	D7 0 1	D6 0 1	D5 0 1	D4 0 1	D3 0 1	D2 0 1	D1 0 1
	VREF charge SW OFF ON	Lch EVR Power ON OFF	Rch EVR Power ON OFF	EVR D16 Gain ATT AMP	EVR D08 Gain ATT AMP	EVR D04 Gain ATT AMP	EVR D2 Gain ATT AMP	EVR D1 Gain ATT AMP
				D16(10000)	D08(01000)	D04(00100)	D02(00010)	D01(00001)
(0 4) 00000100	Receiver Speaker Power Save CTL	Receiver Input Select SW	Receiver EVR Power Save CTL		EVR Setting (Receiver) 5bit			
	D8 0 1	D7 0 1	D6 0 1	D5 0 1	D4 0 1	D3 0 1	D2 0 1	D1 0 1
	Receiver Speaker ON OFF	Input Select SW ON OFF	Receiver EVR ON OFF	EVR D16 Gain ATT AMP	EVR D08 Gain ATT AMP	EVR D04 Gain ATT AMP	EVR D2 Gain ATT AMP	EVR D1 Gain ATT AMP
				D16(10000)	D08(01000)	D04(00100)	D02(00010)	D01(00001)

Package Dimensions

unit : mm (typ)
3302A



Pin Assignment



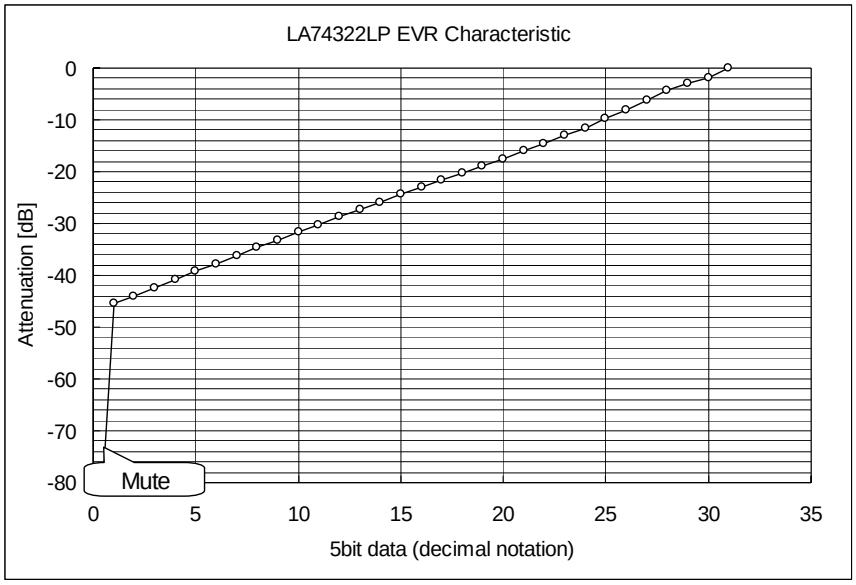
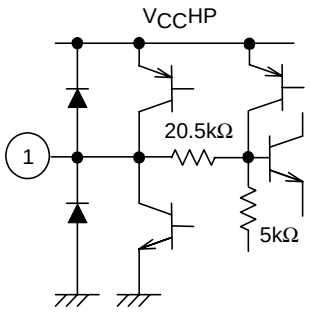
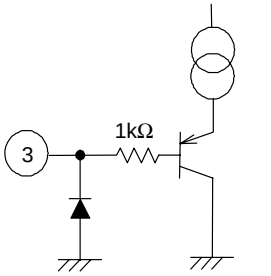
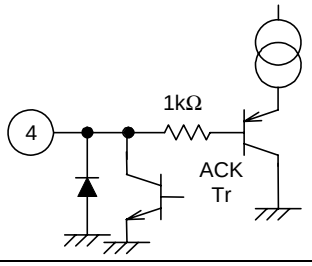
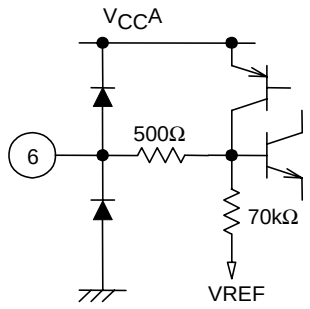
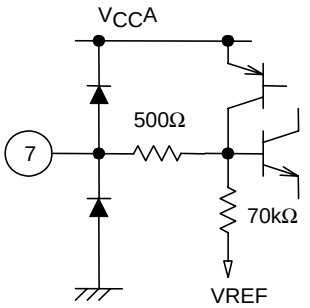
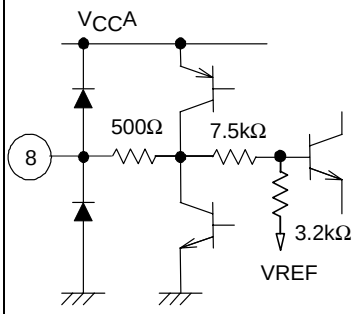
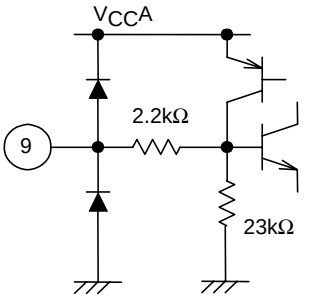
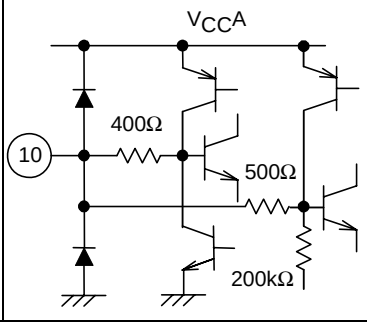


Table of Input/Output Forms

PIN	Pin Name	DC voltage	AC voltage	Description of functions	Equivalent circuit diagram in pin
1	Receiver (-) output	1.65V	Reference output level =-10dBV (@ EVR=Max. audio source input =-30dBV)	Receiver reverse phase output pin	
2	V_{CC} A	3.0V		Power pin for analog signal part	
3	CLOCK			CLOCK input pin	
4	DATA			DATA input pin	
5	A GND	0V		GND pin for analog signal part	

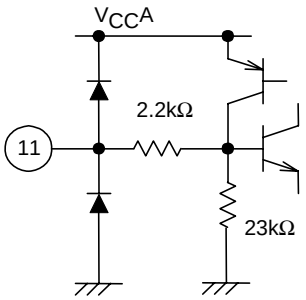
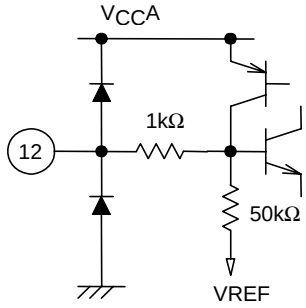
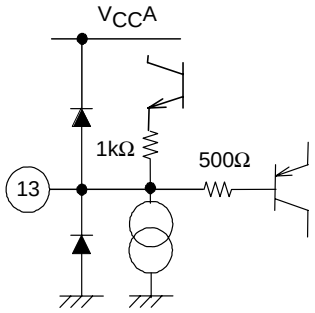
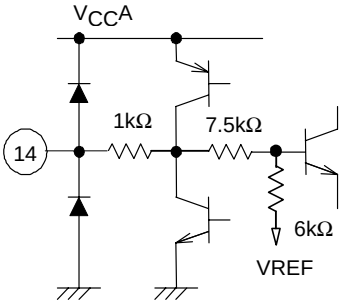
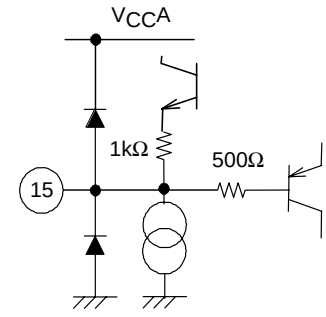
Continued on next page.

Continued from preceding page.

PIN	Pin Name	DC voltage	AC voltage	Description of functions	Equivalent circuit diagram in pin
6	MIC1 IN	1.5V	Reference input level =-50dBV Maximum input level =-20dBV	MIC1 input pin	
7	MIC2 IN	1.5V	Reference input level =-50dBV Maximum input level =-20dBV	MIC2 input pin	
8	MIC OUT	1.5V	Reference output level =-40dBV Maximum output level =-10dBV	MIC output pin	
9	MIC1 V_{CC}	2.3V		MIC1 power pin	
10	VREF	2.3V		MIC V_{CC} and VREF ripple rejection pin	

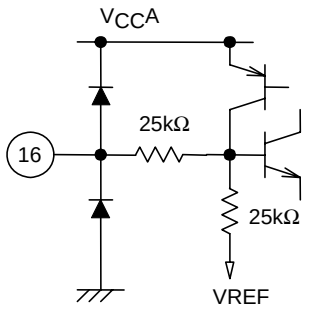
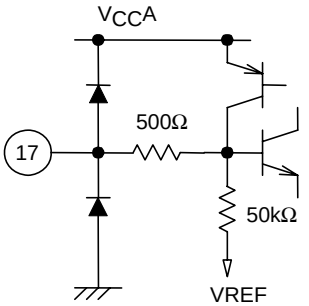
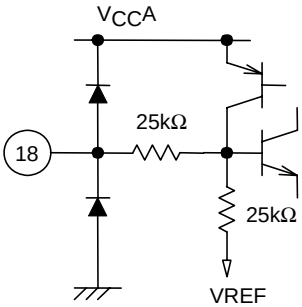
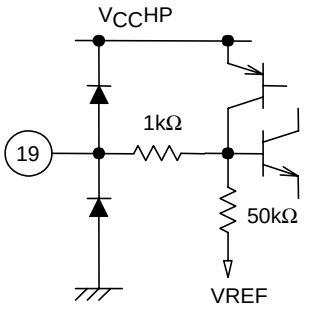
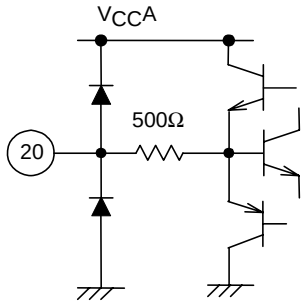
Continued on next page.

Continued from preceding page.

PIN	Pin Name	DC voltage	AC voltage	Description of functions	Equivalent circuit diagram in pin
11	MIC2 V_{CC}	2.3V		MIC2 power pin	
12	ALC1 IN		Reference output level =-40dBV Maximum output level =-10dBV	ALC1 input pin	
13	ALC1 DET			ALC1 detection pin	
14	Base_Band OUT	1.5V	Reference output level =-16dBV Maximum input level =-3dBV	Base band output pin	
15	ALC2 DET			ALC2 detection pin	

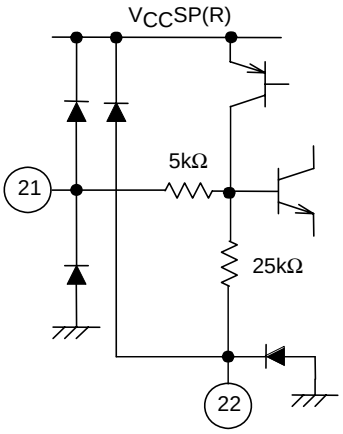
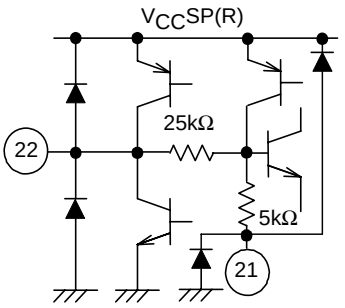
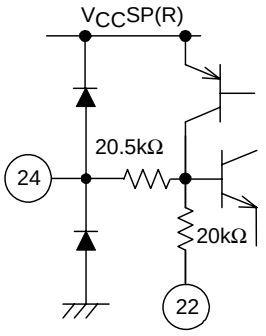
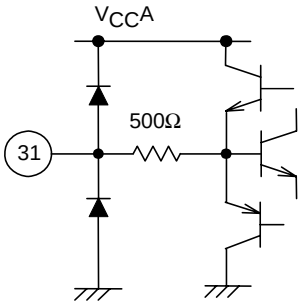
Continued on next page.

Continued from preceding page.

PIN	Pin Name	DC voltage	AC voltage	Description of functions	Equivalent circuit diagram in pin
16	Lch audio source IN	1.5V	Reference output level =-15dBV Maximum input level =-3dBV	Lch audio input pin	
17	Base Band IN	1.5V	Reference output level =-16dBV Maximum output level =-10dBV	Base band input pin	
18	Rch audio source IN	1.5V	Reference output level =-15dBV Maximum input level =-3dBV	Rch audio source input pin	
19	Rch HP IN	1.5V	Reference output level =-16dBV (@Base band input) =-21dBV (@audio source input) Maximum input level =-10dBV (@Base band input) =-9dBV (@audio source input)	Rch HP input pin	
20	Rch EVR OUT	1.5V	Reference output level =-16dBV (@Base band input) =-21dBV (@audio source input) Maximum input level =-10dBV (@Base band input) =-9dBV (@audio source input)	Rch EVR output pin	

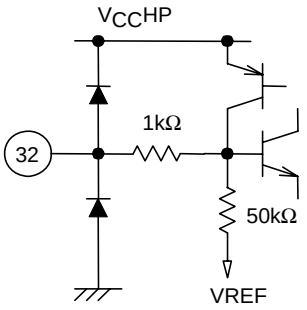
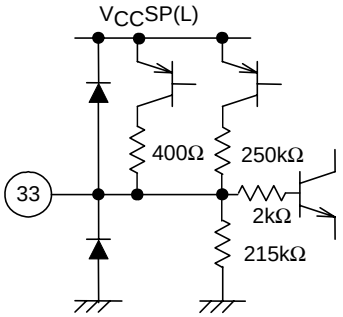
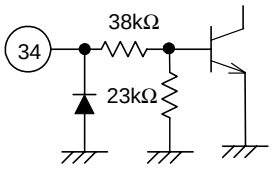
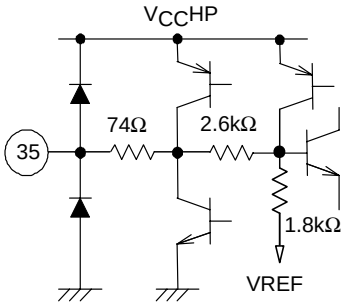
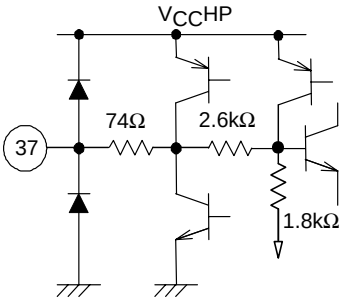
Continued on next page.

Continued from preceding page.

PIN	Pin Name	DC voltage	AC voltage	Description of functions	Equivalent circuit diagram in pin
21	Rch SPK IN	1.65V	Reference output level =-16dBV (@Base band input) =-21dBV (@audio source input) Maximum input level =-10dBV (@Base band input) =-9dBV (@audio source input)	Rch Speaker input pin	
22	Rch SPK(-)OUT	1.65V	Reference output level =-1dBV (@audio source input =-15dBV)	Rch speaker reverse phase output pin	
23	GND SPK(R)	0V		Rch speaker GND pin	
24	Rch SPK(+)OUT	1.65V	Reference output level =-1dBV (@audio source input =-15dBV)	Rch speaker normal phase output pin	
25	V_{CC} SP(R)	3.6V		Rch speaker power pin	
26	V_{CC} SP(L)	3.6V		Lch speaker power pin	
27	NC			NC pin	
28	GND SPK(L)	0V		Lch speaker GND	
29	NC			NC pin	
30	NC			NC pin	
31	Lch EVR OUT	1.5V	Reference output level =-16dBV (@Base band input) =-21dBV (@audio source input) Maximum input level =-10dBV (@Base band input) =-9dBV (@audio source input)	Lch EVR output pin	

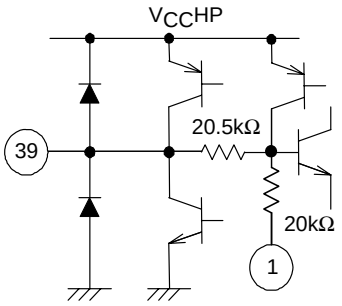
Continued on next page.

Continued from preceding page.

PIN	Pin Name	DC voltage	AC voltage	Description of functions	Equivalent circuit diagram in pin
32	Lch HP IN	1.5V	Reference output level =-16dBV (@Base band input) =-21dBV (@audio source input) Maximum input level =-10dBV (@Base band input) =-9dBV (@audio source input)	Lch HP input pin	
33	VREFSP	1.65V		SPK VREF and ripple rejection pin	
34	STANDBY L			STANDBY control pin	
35	Lch HP OUT	1.5V	Reference output level =-23.5dBV Maximum output level =-3dBV	Lch HP output pin	
36	GND HP	0V		HP GND pin	
37	Rch HP OUT	1.5V	Reference output level =-23.5dBV Maximum output level =-3dBV	Rch HP output pin	

Continued on next page.

Continued from preceding page.

PIN	Pin Name	DC voltage	AC voltage	Description of functions	Equivalent circuit diagram in pin
38	V_{CC}HP	3.0V		HP & receiver speaker power pin	
39	Receiver (+) OUT	1.5V	Reference output level =-10dBV (@ EVR=Max audio source input =-30dBV)	Receiver speaker normal phase output pin	
40	Receiver GND	0V		Receiver GND	

Internal Equivalent Circuit Diagram