



SANYO Semiconductors

DATA SHEET

LA75501V — Monolithic Linear IC For Use in TV/VTR Applications VIF/SIF Signal Processing IC

Overview

The LA75501V is an adjustment free VIF/SIF signal processing IC for PAL TV/VCR. It supports 38MHz, 38.9MHz, and 39.5MHz as the IF frequencies, as well as PAL sound multi-system (M/N,B/G, I, D/K), and contains an on-chip sound carrier trap and sound carrier BPF. To adjust the VCO circuit, AFT circuit, and sound filter, 4MHz external crystal or 4MHz external signal is needed.

Function

- VIF Block: VIF Amplifier, PLL Detector, IF AGC, RF AGC, Equalizer, amplifier, Buzz Canceller, SIF Trap, Digital AFT, FLL, 4MHz X'tal oscillation
- 1st SIF Block: 1st SIF Amplifier, 1st SIF Detector, 1st SIF AGC
- SIF Block: Limiter Amplifier Down Converter, PLL FM Detector SIF PLL SIF VCO, SIF BPF
- Others: IF SW (38.9MHz, 38MHz), SIF4 System SW (B/G, I, D/K, M/N), IFAGC 2nd filter

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum Supply voltage	V _{CC}		7	V
Circuit voltage	V ₁₆		V _{CC}	V
	V ₁₈		V _{CC}	V
Circuit Current	I ₃₀		-1	mA
	I ₁₇		+0.5	mA
	I ₆		-10	mA
	I ₄		-3	mA
Allowable power dissipation	P _{d max}	Ta ≤ 80°C *	500	mW
Operating temperature	T _{opr}		-20 to +85	°C
Storage temperature	T _{stg}		-55 to +150	°C

* Mounted on a board : 65×72×1.6mm³, paper phenol board.

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Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V _{CC}		5.0	V
Operating supply voltage	V _{CC op}		4.5 to 6.0	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 5V, fp = 38.9MHz

VIF Block

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Circuit current	I ₂₁			64.0	73.6	mA
Maximum RF AGC voltage	V _{17H}	Collector load 30k VC2 = 9V	8.5	9		V
Minimum RF AGC voltage	V _{17L}		0.0	0.3	0.7	V
Input sensitivity	v _i		33	39	45	dBμV
AGC range	GR		58			dB
Maximum allowable input	V _{i max}		92	97		dBμV
No-signal video output voltage	V ₆		2.9	3.3	3.7	V
Sync. Signal tip voltage	V _{6tip}		0.9	1.2	1.5	V
Video output amplitude	V _O		1.5	1.8	2.1	Vp-p
Video S/N	S/N	B/G	48	52		dB
C-S best	IC-S	PS = 10dB	26	32	38	dB
Differential gain	DG	80dBμ, 87.5% MOD		5	10	%
Differential phase	DP	80dBμ, 87.5% MOD		2	10	°C
Black noise threshold voltage	V _{BTH}			0.7		V
Black noise clamp voltage	V _{BCL}			1.8		V
VIF input resistance	R _i			2.5	3.0	kΩ
VIF input capacitance	C _i			3	6	PF
Maximum AFT voltage	V _{16H}		4.3	4.7	5.0	V
Minimum AFT voltage	V _{16L}		0	0.2	0.7	V
AFT tolerance 1	dfa1	f = 38.9MHz		±35	±70	KHz
AFT tolerance 2	dfa2	f = 38.0MHz		±35	±70	KHz
ATF detection sensitivity	sf	R _L = 100k/100KΩ	30	55	80	mV/kHz
AFT Dead Zone	fda			30	60	MHz
APC pull-in range (U)	fpu		1.5	2.0		MHz
APC pull-in range (L)	fpl		1.5	2.0		MHz
VCO maximum variable range (U)	dfu		1.5	2.0		MHz
VCO maximum variable range (L)	dfl		1.5	2.0		MHz
VCO control sensitivity	β		2.0	4.0	8.0	kHz/mV
N Trap 1 (4.5M)	NT1		-30	-35		dB
N Trap 2 (4.8M)	NT1-1		-19	-24		dB
B/G Trap 1 (5.5M)	BT1		-27	-32		dB
B/G Trap 2 (5.85M)	BT1-1		-20	-25		dB
I Trap 1 (6.0M)	IT1		-25	-30		dB
I Trap 2 (6.55M)	IT1-1		-15	-20		dB
D/K Trap1 (6.5M)	DT1		-25	-30		dB
Group delay 1 NTSC (3.0M)	ngd1		30	60	90	ns
Group delay 1-1 NTSC (3.5M)	ngd1-1		160	230	300	ns
Group delay 2 B/G (4M)	bgd2		70	100	130	ns
Group delay 2-1 B/G (4.4M)	bgd2-1		160	230	300	ns
Group delay 3 I (4M)	bgd3		20	50	80	ns
Group delay 3-1 I (4.4M)	bgd3-1		60	90	120	ns
Group delay 4 D/K (4M)	bgd4		0	30	60	ns
Group delay 4-1 D/K (4.4M)	bgd4-1		10	40	70	ns

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1st SIF Block

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Conversion gain	V_G	fp-5.5MHz, $V_i = 500\mu V$	26	32	36	dB
SIF carrier output level	S_o	$V_i = 10mV$		100		mVrms
1st SIF maximum input	$S_i \text{ max}$	$S_o \pm 2dB$		106		dB μV
1st SIF input resistance	R_{iS}			2.0	2.4	K Ω
1st SIF input capacitance	C_{iS}			3	6	PF

SIF Block

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Limiting sensitivity	$V_i \text{ (lim)}$	$f = 5.5MHz$	46	52	58	dB μV
FM detector output voltage	$V_O \text{ (FM)}$	$\Delta F = \pm 30kHz$ at 400Hz	480	600	750	mVrms
AM rejection ratio	AMR	AM = 30% at 400Hz	50	60		dB
Distortion	THD	$f = 5.5MHz$ $\Delta F = \pm 30kHz$		0.3	1.0	%
FM detector output S/N	S/N (FM)	DIN. Audio	55	60		dB
BPF 3dB band width	BW			± 100		kHz
PAL de-emphasis	Pdeem	fm = 3kHz		-3		dB
NTSC de-emphasis	Ndeem	fm = 2kHz		-3		dB
PAL/NT Audio voltage gain difference	GD			6		dB

Others

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Minimum 4MHz level (at external input)	X_4MIN	Terminal value	80	86	92	dB μ
SIF system SW threshold voltage	V_{13} V_{14}			1.4		V
IF system SW threshold voltage	V_{15}				270	K Ω
Split/Inter SW	V_{20}			0.5		V

System Changeover

SW/SIF system SW

The SIF system can be changed over by setting A (pin 13) and B (pin 14) to GND and the open state respectively.

A	B	B/G	I	D/K	M/N	FM DET LEVEL	De-emphasis
GND	GND				O	6dB	75 μs
GND	OPEN			O		0dB	50 μs
OPEN	GND		O			0dB	50 μs
OPEN	OPEN	O				0dB	50 μs

Note: 'O' indicates that the system is selected.

IF system SW

The IF frequency is selected 38.9MHz mode with the pin 15 (crystal oscillation) open.

The IF frequency is selected 38MHz mode by adding 220K Ω between the pin 15 and GND.

Inter carrier SW

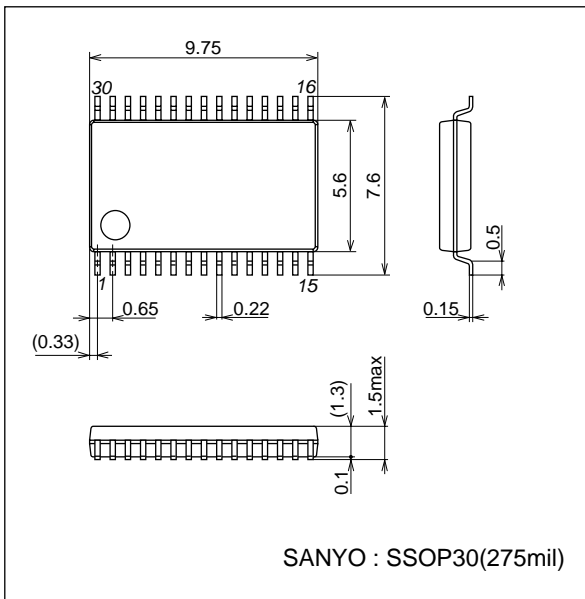
Inter-carrier is selected by setting the 1st SIF input (pin 20) to GND.

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Package Dimensions

unit : mm

3191B



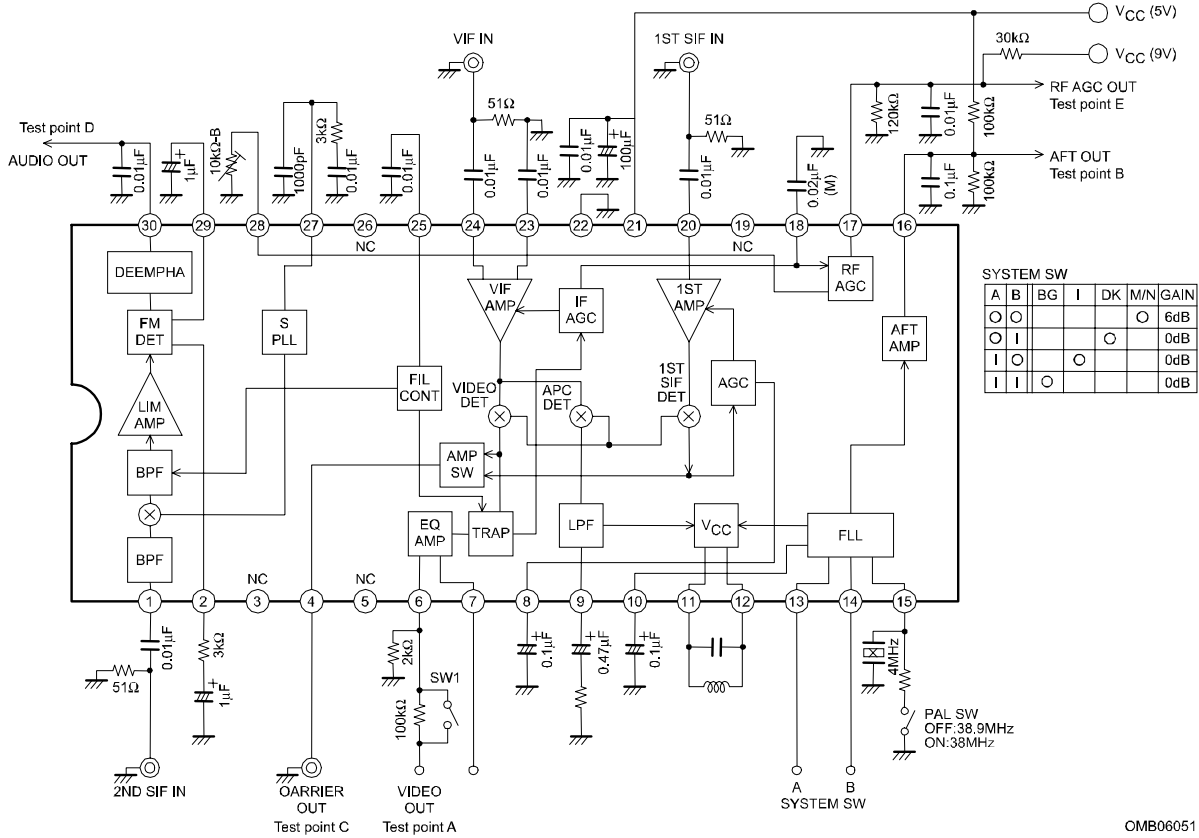
Pin Assignment

SIF INPUT	1	LA75501V	30	FM DET OUT
AUDIO FILTER	2		29	FM NOISE FILTER
NC	3		28	RF AGC VR
1ST SIF OUT	4		27	SIF PLL FILTER
NC	5		26	NC
VIDEO DET OUT	6		25	FILTER CONTROL CAPACITOR
EQ FILTER	7		24	VIF INPUT
SIF AGC FILTER	8		23	VIF INPUT
APC FILTER	9		22	GND
FLL FILTER	10		21	V _{CC}
VCO COIL	11		20	1ST SIF INPUT
VCO COIL	12		19	NC
SYSTEM SW [A]	13		18	IF AGC FILTER
SYSTEM SW [B]	14		17	RF AGC OUT
4MHz OSC	15		16	AFT OUT

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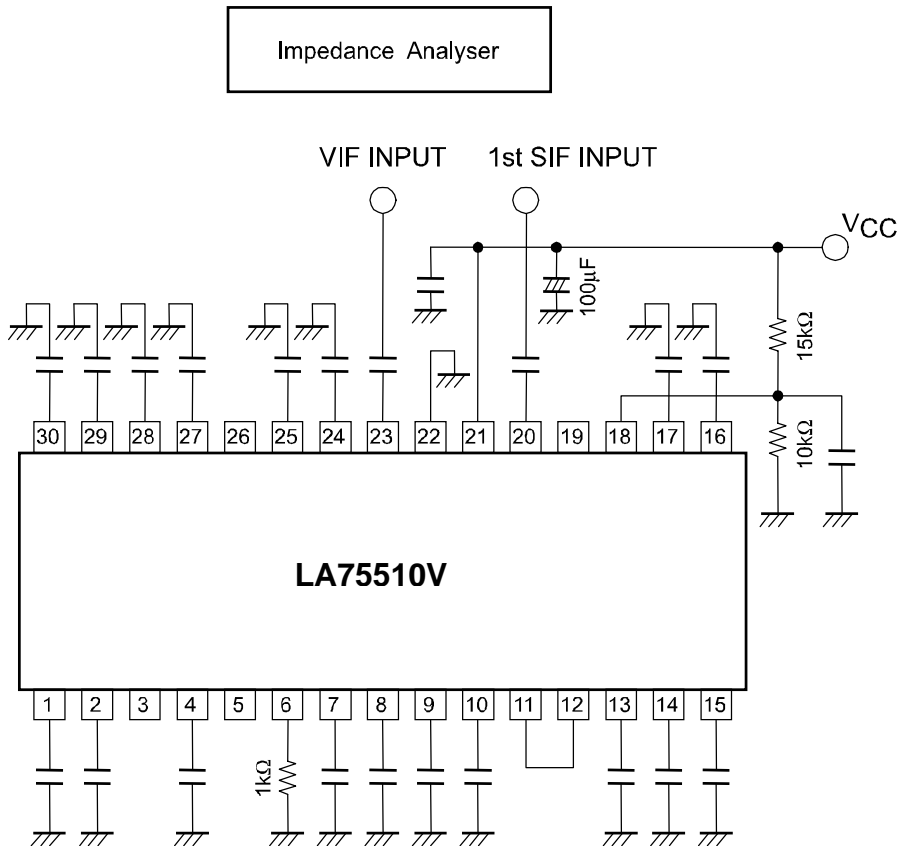
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Block Diagram and AC Characteristics Test Circuit



OMB06051

Input Impedance Test Circuit



0.01µF for the capacitor which has not been specified.

OMB06050

Test Conditions**V1. Circuit current [I₂₁]**

- (1) External AGC (V₁₈ = 1.5V)
- (2) RF AGC VR MAX
- (3) Connect an ammeter to the V_{CC} and measure the incoming current to pin 17.

V2. V3. Maximum RF AGC voltage, Minimum RF AGC voltage [V_{17H}, V_{17L}]

- (1) Internal AGC
- (2) Input a 38.9MHz, 10mVrms, continuous wave to the VIF input pin.
- (3) Adjust the RF AGC VR (resistance max.) and measure the maximum RF AGC voltage.
- (4) Adjust the RF AGC VR (resistance min.) and measure the minimum RF AGC voltage.
- (3), (4) Measuring point F

V4. Input sensitivity [V_i]

- (1) Internal AGC
- (2) fp = 38.9MHz 400Hz 40% AM (VIF input)
- (3) Turn off the SW1 and put 100kΩ through.
- (4) Measure the VIF input level at which the 400Hz detection output level at test point A becomes 0.7Vp-p.

V5. AGC range [GR]

- (1) Apply the V_{CC} voltage to the external AGC, If AGC (pin 18).
- (2) In the same manner under the same conditions as for V4 (input sensitivity), measure the VIF input level at which the detection output level becomes 0.7Vp-p. V_{il} *V_i: Input sensitivity

(3) $GR = 20 \log \frac{V_{il}}{V_i} \text{ dB}$

V6. Maximum allowable input [V_i max]

- (1) Internal AGC
- (2) fp = 38.9MHz 15kHz 78% AM (VIF input)
- (3) VIF input level at which the detection output level at test point A becomes video output (V_O) ±1dB.

V7. No-signal video output voltage [V₆]

- (1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 18).
- (2) Measure the DC voltage of VIDEO output (A).

V8. Sync. signal tip voltage [V_{6tip}]

- (1) Internal AGC
- (2) Input a 38.9MHz, 10mVrms, continuous wave to the VIF input pin.
- (3) Measure the DC voltage of VIDEO output (A).

V9. Video output level [V_O]

- (1) Internal AGC
- (2) fp = 38.9MHz 15kHz 78% AM
V_i = 10mVrms (VIF input)
- (3) Measure the peak value of the detection output level at test point A. (V_{p-p})

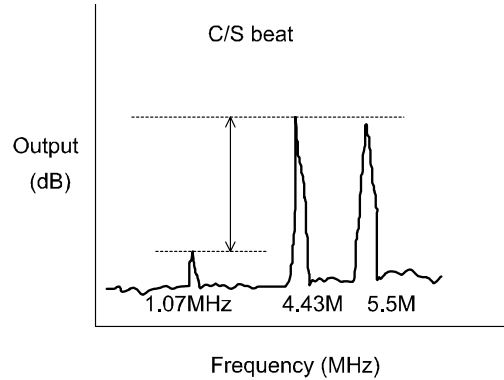
V10. Video S/N [S/N]

- (1) Internal AGC
- (2) fp = 38.9MHz CW = 10mVrms (VIF input)
- (3) Measure the noise voltage at test point A in RMS volts through a 10kHz to 4MHz band-pass filter.
..... Noise voltage (N)

(4) $S/N = 20 \log \frac{\text{Video voltage (V}_{p-p})}{N \text{ (V}_{rms})} = 20 \log \frac{1.12V_{p-p}}{N(V_{rms})} \text{ (dB)}$

V11. C/S beat [Ics]

- (1) Apply DC voltage to the external AGC IF AGC (pin 18) and vary it.
- (2) $f_p = 38.9\text{MHz}$ CW;10mVrms
 $f_c = 34.47\text{MHz}$ CW;10mVrms - 10dB
 $f_s = 33.4\text{MHz}$ CW;10mVrms - 10dB
- (3) Adjust the IF AGC (pin 18) voltage so that the output level at test point A becomes 1.3Vp-p.
- (4) Measure the difference between the levels for 4.43MHz and 1.07MHz components at test point A.



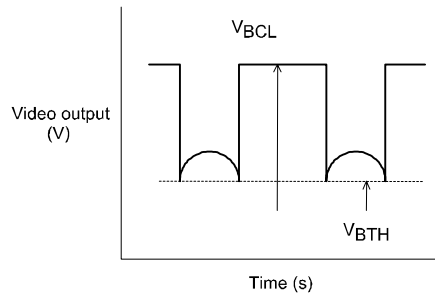
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V12.V13. Differential gain, differential phase [DG, DP]

- (1) Internal AGC
- (2) $f_p = 38.9\text{MHz}$ APL50% 87.5% Modulation video signal
 $V_i = 10\text{mVrms}$
- (3) Measure the DG and DP at test point A.

V14.V15. Black noise threshold and clamp voltage [V_{BTH} , V_{BCL}]

- (1) Apply DC voltage (1 to 3V) to the external AGC, IF AGC (pin 18) and adjust the voltage.
- (2) $f_p = 38.9\text{MHz}$ 400Hz 40% AM 10mVrms (VIF input)
- (3) Adjust the IF AGC (pin 18) voltage to operate the noise canceller.
 Measure the V_{BTH} , V_{BCL} at test point A.



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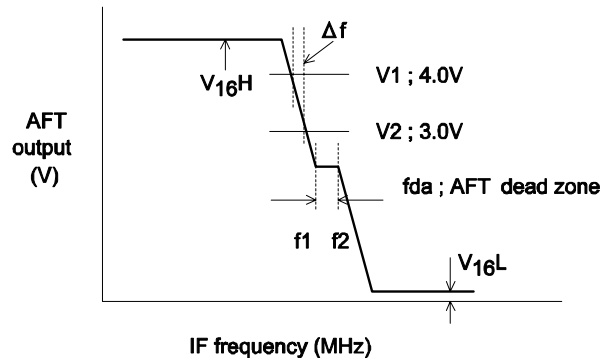
V16. V17. VIF input resistance, input capacitance [R_i , C_i]

- (1) External AGC ($V_{18} = 2\text{V}$)
- (2) Referring to the Input Impedance Test Circuit, measure R_i and C_i with an impedance analyzer.

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V18. V19. Maximum, minimum AFT voltage, AFT detection sensitivity [V_{16H}, V_{16L}]

- (1) Internal AGC
- (2) $f_p = 38.9\text{MHz} \pm 1.5\text{MHz}$ $V_i = 10\text{mVrms}$ (VIF input)
- (3) Measure maximum and minimum AFT output voltage (at the measuring point B) by changing the input frequency.
- (4) Maximum voltage: V_{16H}, minimum voltage: V_{16L}.



V20.V21.V22.V23. AFT tolerance 1,2,AFT detector sensitivity, AFT Dead Zone [dfa, Sf, fda]

- (1) Measure the frequency deviation when the voltage at the measuring point B changes from V₁ to V₂. Δf

$$Sf \text{ (mV/kHz)} = \frac{V_1 - V_2}{\Delta f}$$

- (2) Measure the width in which the voltage at the measuring point B does not change.
- (3) Calculate as follows:
 $fda \text{ (kHz)} = f_2 - f_1$
- (4) Calculate as follows:
IF Center frequency: 38.9MHz, 38MHz

$$dfa \text{ (kHz)} = f_c - \frac{f_1 + f_2}{2}$$

V24.V25. APC pull-in range [fpu, fpl]

- (1) Internal AGC
- (2) FLL: Free
- (3) $f_p = 33\text{MHz}$ to 44MHz CW; 10mVrms
- (4) Adjust the SG signal frequency to be higher than $f_p = 38.9\text{MHz}$ to bring the PLL to unlocked state.
Note; The PLL is taken as in unlocked state when a beat signal appears at test point A.
- (5) When the SG signal frequency is lowered, the PLL is brought to locked state again. f₁
- (6) Lower the SG signal frequency to bring the PLL to unlock state.
- (7) When the SG signal frequency is raised, the PLL is brought to locked state again. f₂
- (8) Calculate as follows:
 $f_{pu} = f_1 - 38.9\text{MHz}$
 $f_{pl} = f_2 - 38.9\text{MHz}$

V26.V27. VCO maximum variable range (U, L) [dfu, dfll]

- (1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 18).
- (2) f_l is taken as the frequency when 1V is applied to the APC pin (pin 9). In the same manner, f_u is taken as the frequency when 5V is applied to the APC pin (pin 9).
 $dfu = f_u - 38.9\text{MHz}$
 $dfll = f_l - 38.9\text{MHz}$

V28. VCO control sensitivity [β]

- (1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 18).
- (2) Apply the 3V to the external FLL, FLL (pin 10).
- (3) Pick up the VCO oscillation frequency from the VIDEO output (A), GND, etc.
And adjust the VCO coil so that the frequency becomes 38.9MHz.
- (4) f_1 is taken as the frequency when 2.8V is applied to the APC pin (pin 9).
In the same manner, f_2 is taken as the frequency when 3.2V is applied to the APC pin (pin 9).

$$\beta = f_2 - \frac{f_1 - f_2}{400} \quad (\text{kHz/mV})$$

F1. 1st SIF conversion gain [V_G]

- (1) Internal AGC
- (2) $f_p = 38.9\text{MHz}$ CW; 10mV (VIF input)
 $f_s = 33.4\text{MHz}$ CW; 500 μV (1st SIF input) V_1
- (3) measure the detection output level at test point C (5.5MHz) V_2

$$(4) V_G = 20\log \frac{V_2}{V_1} \text{ dB}$$

F2. 5.5MHz output level [S_o]

- (1) Internal AGC
- (2) $f_p = 38.9\text{MHz}$ CW; 10mV (VIF input)
 $f_s = 33.4\text{MHz}$ CW; 10mV (1st SIF input) V_1
- (3) Measure the detection output level at test point C (5.5MHz). S_o (mVrms)

F3. 1st maximum input [$S_i \text{ max}$]

- (1) Internal AGC
- (2) $f_p = 38.9\text{MHz}$ CW; 10mV (VIF input)
 $f_s = 33.4\text{MHz}$ CW; Variable (1st SIF input)
- (3) Input level at which the detection output (5.5MHz) at test point C becomes $S_o \pm 2\text{dB}$ $S_i \text{ max}$

F4.F5. 1st SIF input resistance, input capacitance [R_i (SIF1), C_i (SIF1)]

- (1) Referring to the Input Impedance Test Circuit, measure R_i and C_i with an impedance analyzer.

S1. SIF Limiting sensitivity [V_i (lim)]

- (1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 18).
- (2) $f_s = 5.5\text{MHz}$ $f_m = 400\text{Hz}$ $\Delta F = \pm 300\text{kHz}$ (SIF input)
- (3) Set the SIF input level to 31.6mVrms and measure the level at test point D. V_1
- (4) Lower the SIF input level and measure the input level which becomes V_1 3dB.

S2.S4. FM detection output voltage, total harmonics distortion [$V_O(\text{FM})$, THD]

- (1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 18).
- (2) $f_s = 5.5\text{MHz}$ $f_m = 400\text{Hz}$ $\Delta f = \pm 30\text{kHz}$
(SIF input $V_i = 31.6\text{mVrms}$)
- (3) Measure the FM detection output voltage, total harmonics distortion at test point D.

S3. AM rejection ratio [AMR]

- (1) External AGC ($V_{18} = V_{CC}$)
- (2) $f_s = 5.5\text{MHz}$ $f_m = 400\text{Hz}$ AM = 30%
(SIF input $V_i = 31.6\text{mVrms}$)
- (3) Measure the output level at test point D. V_{AM}

$$(4) \text{AMR} = 20\log \frac{V_O(\text{DET})}{V_{AM}} \text{ dB}$$

S5. SIF S/N [S/N (FM)]

- (1) External AGC ($V_{15} = V_{CC}$)
- (2) $f_s = 5.5\text{MHz}$ NO MOD $V_i = 31.6\text{mVrms}$
- (3) Measure the output level at test point D. V_n

$$(4) \text{S/N} = 20\log \frac{V_O(\text{DET})}{V_n} \text{ dB}$$

S7.S8. PAL, NT de-emphasis [Pdeem, Ndeem]

- (1) External AGC ($V_{18} = V_{CC}$)
- (2) $f_s = 5.5\text{MHz}$ $f_m = 3\text{kHz}$ $\Delta F = \pm 30\text{kHz}$
(SIF input $V_i = 31.6\text{mVrms}$)
- (3) Open system switches (A (pin 13) and B (pin 14)). (BG mode)
- (4) Measure the FM detector output voltage at test point D. V_p
- (5) Calculate as follows:
 $P_{deem} (\text{dB}) = V_p - V_O (\text{FM})$
- (6) $f_s = 4.5\text{MHz}$ $f_m = 2\text{kHz}$ $\Delta F = \pm 30\text{kHz}$
(SIF input $V_i = 31.6\text{mVrms}$)
- (7) Set system switches [A (pin 13) and B (pin 14)] to GND. (NT mode)
- (8) Measure the FM detector output voltage at test point D. V_p
- (9) Calculate as follows:
 $N_{deem} (\text{dB}) = V_{nt} - V_O (\text{FM})$

S9. PAL/NT Audio voltage gain difference [GD]

- (1) External AGC ($V_{18} = V_{CC}$)
- (2) $f_s = 4.5\text{MHz}$ $f_m = 400\text{Hz}$ $\Delta F = \pm 30\text{kHz}$
(SIF input $V_i = 31.6\text{mVrms}$)
- (3) Set system switches [A (pin 13) and B (pin 14)] to GND.
- (4) Measure the FM detector output voltage at test point D. V_{nt}
- (5) Calculate as follows:
 $GD (\text{db}) = V_{nt} - V_O (\text{FM})$

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