Ordering number : ENA1256

SANYO Semiconductors
DATA SHEET

LA75525AVA — Monolithic Linear IC For TV and VCR sets VIF/SIF Signal-Processing IC

Overview

The LA75525AVA is a completely adjustment-free NTSC VIF/SIF signal-processing IC for TV sets and VCRs. It supports IF frequencies of 45.75MHz. It integrates an automatic adjustment circuit for the VCO, an AFT circuit, and an audio carrier trap circuit on the same chip and requires the input of either a 4MHz or 3.58MHz reference signal.

Functions

- VIF block: VIF amplifier, buzz canceller, IF-VCO, PLL detector, IF-AGC, RF-AGC, digital AFT, equalizer amplifier
- 1stSIF block: 1stSIF amplifier,1stSIF detector
- SIF block: Limiter amplifier, PLL FM detector
- Others: reference frequency changeover SW, AFT mute voltage SW

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		6	V
Circuit voltage	V12		V_{CC}	V
Circuit current	I5		-3	mA
	I9		-7	mA
	I24		-2	mA
Allowable power dissipation	Pd max	Ta ≤ 75°C, Mounted on a specified board *	500	mW
Operating temperature	Topr		-20 to +75	°C
Storage temperature	Tstg		-55 to +150	°C

* Specified board: 114.3mm×76.1mm×1.6mm, glass epoxy board.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		5	V
Operation supply voltage	V_{CC} op		4.5 to 5.5	V

Electrical Characteristics at V_{CC}=5V, S7, S9: Short

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
VIF Block						
Circuit current (external trap)	I_4(EXT)	External Trap	60	70	80	mA
Max RFAGC voltage	V_{14}H		V_{CC}-0.5	V_{CC}		V
Min RFAGC voltage	V_{14}L			0	0.5	V
Input sensitivity	Vi	Video out2	34	40	46	dBμV
AGC range	GR		58	63		dB
Max allowable input	Vi max		95	100		dBμV
No-signal state video output voltage (Ext TRAP)	V_5		1.85	2.2	2.55	V
Sync signal edge voltage	V5tip		0.8	1.0	1.2	V
Video output level (External trap)	VOT		0.89	1.05	1.21	Vpp
Black noise threshold voltage	VBTH		0.40	0.65	0.90	V
Black noise clamp voltage	VBCL		1.2	1.5	1.8	V
Video S/N (External trap)	S/N(EXT)	External Trap	48	52		dB
C-S beat	IC-S	P/C = P/S = 10dB	38	43		dB
Frequency characteristics	Fc	6MHz	-3	-1.5		dB
Differential gain	DG			3	6.5	%
Differential phase	DP			3	5	deg
No-signalt AFT voltage	V12	pin 15 to GND	2.0	2.5	3.0	V
Max AFT voltage	V12H		V_{CC}-1	V_{CC}-0.5	V_{CC}	V
Min AFT voltage	V12L		0	0.18	1	V
AFT detection sensitivity	Sf		8.5	12.5	16.5	mV/kHz
AFT output resolution	Res-aft			3.125		kHz/bit
VIF input resistance	Ri			1.0		kΩ
VIF input capacity	Ci			3		pF
APC pull-in range (U)	Fpu		2.0	2.4		MHz
APC pull-in range (L)	Fpl			-2.4	-2.0	MHz
1st SIF block: Pin 13 41.25MHz input						
Conversion gain	VG	S = 40dBμ	37	43	49	dB
Output level	S_O	S = 80dBμ	100	110	120	dBμV
SIF output gain	Gbpf	Reference to SIF input (Pin 1)	0	3	6	dB
1st SIF max input	Si max		100	110		dBμV
1st SIF input resistance	Ri(SIF)	41.25MHz		2		kΩ
1st SIF input capacity	Ci(SIF)	41.25MHz		3		pF
SIF block: Pin 13 41.25MHz input						
Limiting sensitivity	Vli(lim)		50	56	62	dBμV
FM detection output voltage	V_OFM	+/-25kHz	420	600	780	mVrms
AMR	AMR		50	60		dB
Distortion factor	THD			0.3	0.8	%
SIF S/N	S/N(FM)		59	65		dB
Control block						
Inter carrier control voltage	V_{13}				0.3	V
AFT mute level control voltage	V_{15}				0.3	V
Others						
Reference clock input level	Reflev	4.0MHz	83	90	95	dBμV
Reference frequency SW threshold resistance value	R_{11}		150	270		kΩ

A: IF system SW

The IF frequency becomes 45.75MHz when pin 10 is open.

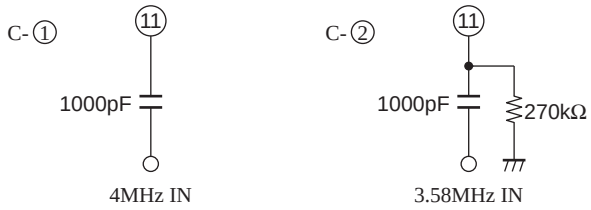
B: Split / Inter carrier SW

Inter-carrier is selected by setting the 1st SIF input (pin 13) to GND.

C: Reference frequency changeover SW

The reference frequency becomes 4.0MHz when pin 11 is set to ”C-①”

This frequency becomes 3.58MHz when this pin is set to ”C-②”



D: AFT mute level

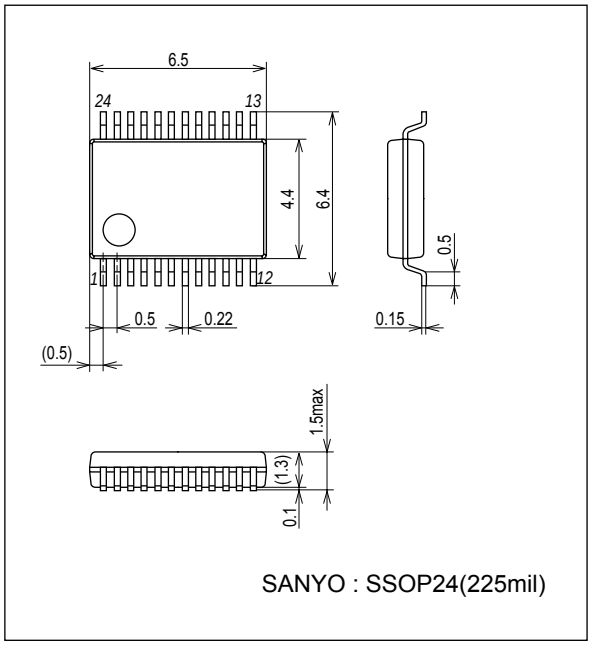
The AFT mute level becomes HI (V_{CC}) when pin 15 is open.

This level becomes MIDDLE ($V_{CC}/2$) when pin 15 is connected to GND.

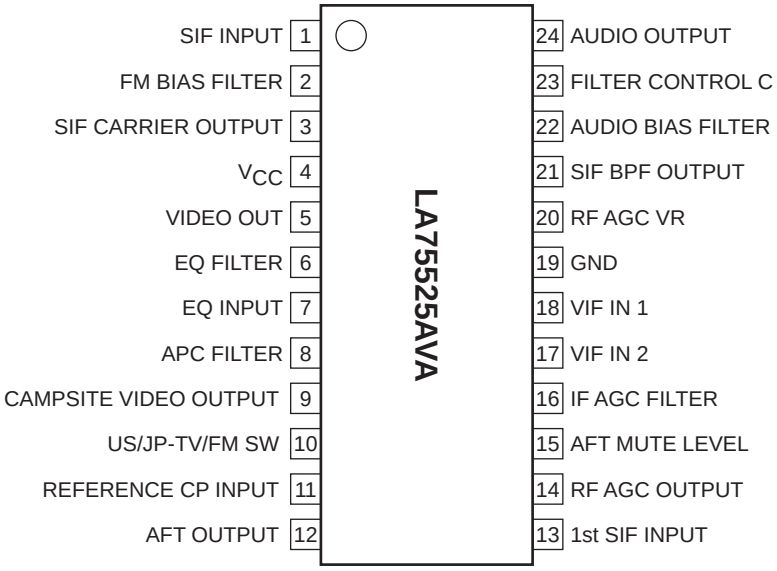
* For V_{CC} = 5 V

Package Dimensions

unit : mm (typ)
3287

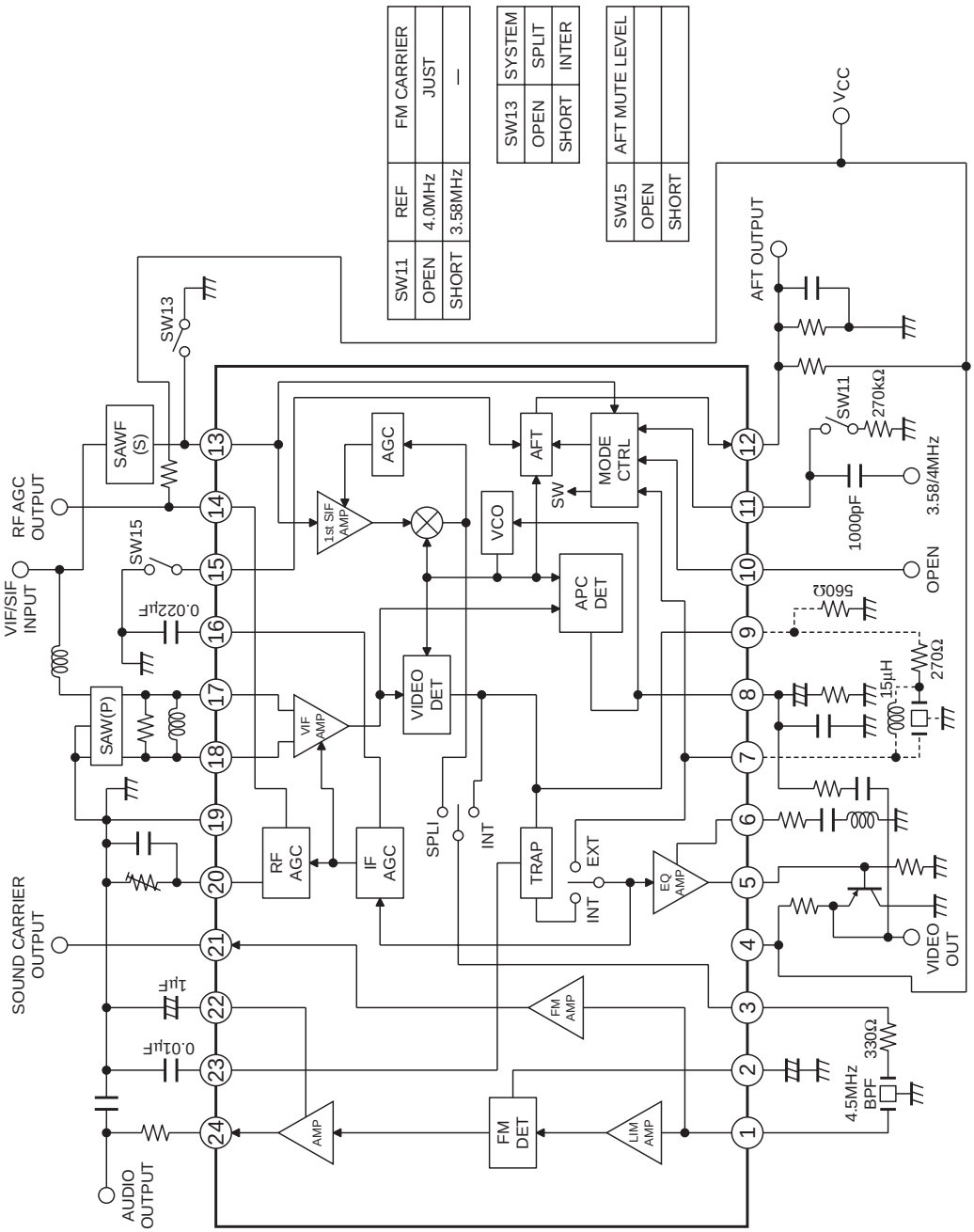


Pin Assignment

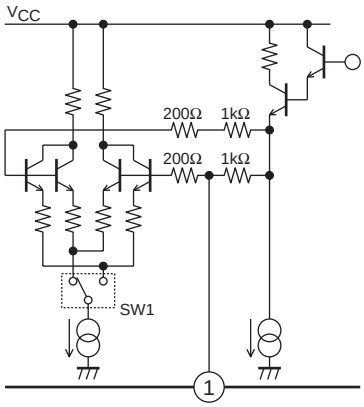
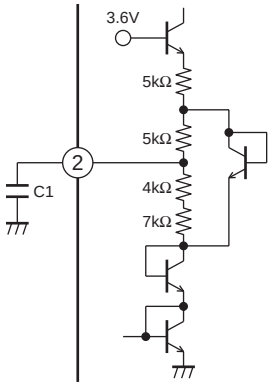
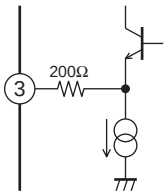
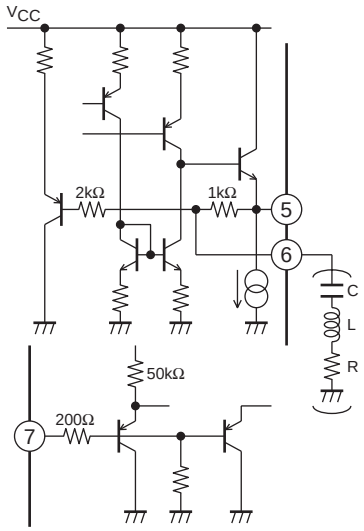


Top View

Block Diagra



Pin Function

Pin No.	Pin name	Function	Equivalent circuit
1	SIF INPUT	SIF input. The input impedance is about 1kΩ. Since buzzing and buzz beating can occur if interference enters this input pin, care must be taken when design the pattern layout for this pin. Note that the video and chrominance signals are especially likely to interface with the audio signal. Also, the VIF carrier signal can also cause interference. By SW1, Gain at the time of Intercarrier and Split system is switched.	
2	FM BIAS FILTER	FM detector bias line filter input. Used to improve the FM detector signal-to-noise ratio. C1 should be at least 0.47μF, and 1μF is recommended. If the FM detector is not used, connect pin 2 to ground through a 2kΩ resister. This stops the FM detector VCO.	
3	SIF CARRIER OUTPUT	SIF carrier output. A 200Ω resister is inserted in series with an emitter-follower output.	
4	V_{CC}	Use the shortest distance possible when decoupling Capacitors V_{CC} and ground.	
5 6 7	VIDEO OUT EQ FILTER EQ INPUT	Equalizer circuit. This circuit is used to correct the video signal frequency characteristics. Pin 7 is the EQ amplifier input. Notes on equalizer amplifier is designed as a gain of about 0dB. when user for frequency characteristics correction, a capacitor, inductor, and resistor must be connected in series between pin 6 and ground. Approach used in the equalizer amplifier If Vi the input signal and V_O is the output signal, then: $\frac{R1}{2} + 1(Vi + Vin) = V_O \times G$ Where G is the voltage-follower amplifier gain. Assume: Vin: Imaginary short G ≈ 0. Vin ≈ 0. Then: $AV = \frac{V_O G}{Vi} = \frac{R1}{Z} + 1$ R1 is the IC internal resistance, and is 1kΩ. In the application design, simply select Z to correspond to the desired characteristics. However, since the EQ amplifier gain will be maximum at the resonant point defined by Z, care is required to assure that distortion dose not occur.	

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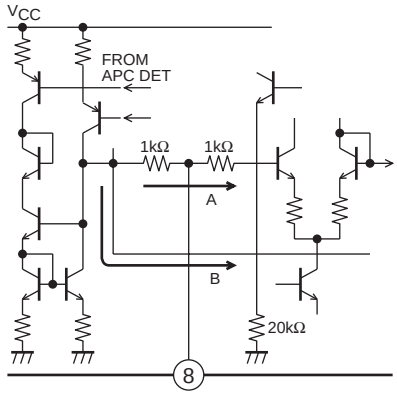
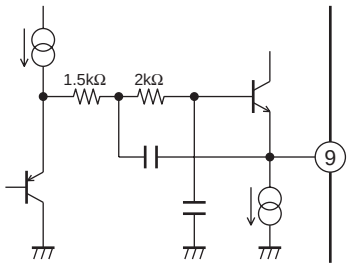
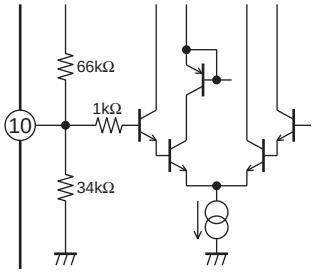
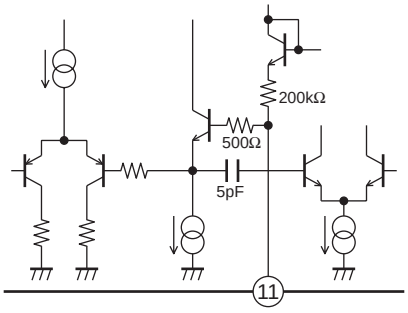
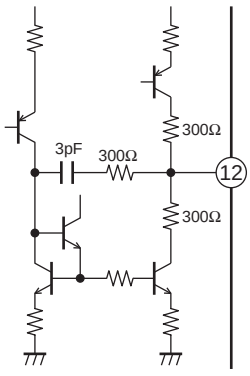
Pin No.	Pin name	Function	Equivalent circuit
8	APC FILTER	PLL detector APC filter connection. For this APC filter we recommend: R = 150Ω C = 0.47μF	
9	COMPOSIT VIDEO OUTPUT	Output for the video signal that includes the SIF carrier. A resistor must be inserted between pin 9 and ground to acquire adequate drive capability R2 ≥ 560Ω	
10	US/JP-TV/FM SW	Please use this pin only with OPEN.	
11	REFERENCE CP INPUT	Reference frequency input from this pin. The reference frequency is 3.58MHz, inserting 270kΩ between this pin to GND. The reference frequency is 4.0MHz, this pin leaving open.	
12	AFT OUTPUT	AFT output. AFT center voltage is generated by an external bleeder. The AFT gain is increased by increasing the resistance of this external bleeder resister. However, this resister must not exceed 390Ω. This circuit includes a control function that control the AFT voltage to naturally approach the center voltage during weak field reception.	

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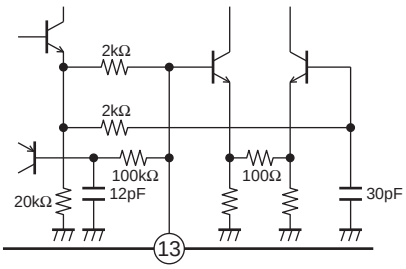
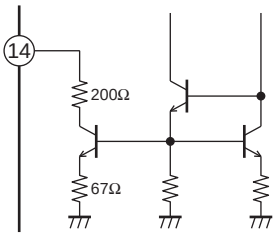
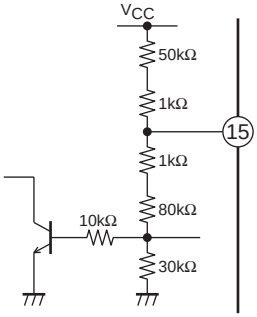
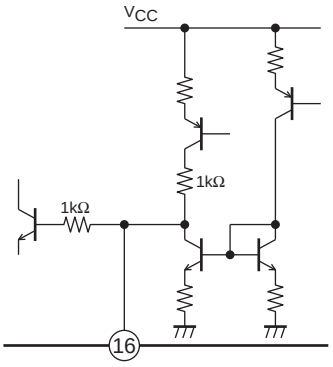
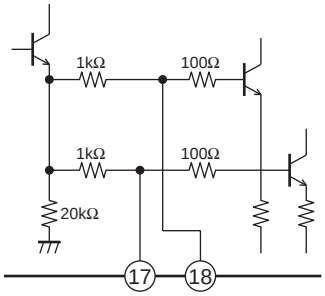
Pin No.	Pin name	Function	Equivalent circuit
13	1st SIF INPUT	First SIF input. ADC cut capacitor must be used in the input circuit. If a SAW filter is used: The first SIF sensitivity can be increased by inserting an inductor between the SAW filter and the IC to neutralize the SAW filter output capacitance and the IC input capacitance. When used in an intercarrier system: This pin (pin 13) maybe connect to GND.	
	RF AGC OUTPUT	RF AGC OUT PUT. This output controls the tuner RF AGC. A protective 200Ω resister is inserted in series with the open collector out put. Determine the external bleeder resister value in accordance with the specifications of the tuner.	
15	AFT MUTE LEVEL	The MUTE voltage of AFT is set up this pin. It becomes a voltage that generated by an external bleeder resistor, when this pin is connected with GND. It becomes a High voltage (V_{CC}) when this pin is leaving open.	
16	IF AGC INPUT	IF AGC filter connection. The signal peak-detected by the built-in AGC detector is converted to the AGC voltage at pin 16. Additionally, a second AGC filter (a lag-lead filter) used to create the dual time constants is provided internally in the IC. Use a 0.022μF capacitor as the external capacitor, and other characteristics.	
17 18	VIF IN 2 VIF IN 1	VIF amplifier input. The input circuit is a balanced circuit, and the input constants are: R = 1.0kΩ C = 3pF	
19	GND	GND	

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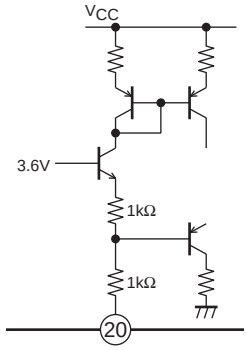
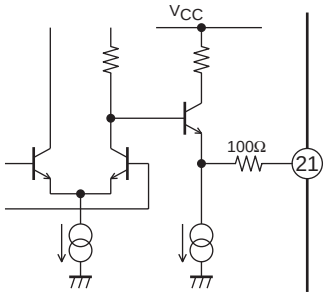
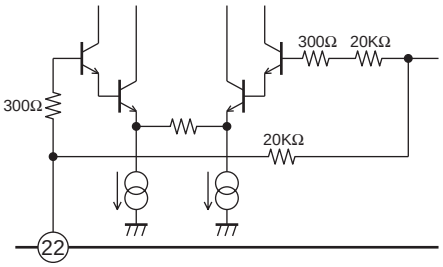
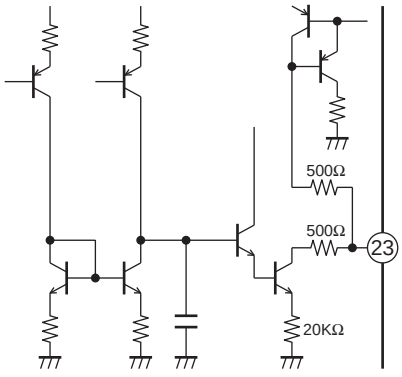
Pin No.	Pin name	Function	Equivalent circuit
20	RF AGC VR	RF AGC VR connection. This pin sets the tuner RF AGC operating point Also, the FM output and the video output can both be muted the same time by connecting this pin to GND.	
21	SIF BPF OUTPUT	The output to the external band-pass filter is passed through an internal 6dB amplifier before being output.	
22	AUDIO BIAS FILTER	Connection for a filter used to hold the FM detector output DC voltage fixed. Normally, a 1μF electrolytic capacitor should be used. The capacitance should be increased if the low band (around 50Hz) frequency characteristics need to be improved. The FM detector output level can be reduced and the FM dynamic range can be increased by inserting a resistor and a capacitor in series between pin 22 and GND.	
23	FILTER CONTROL C	Internal sound carrier TRAP are tuned using the capacitor connected to pin 23. A value between 0.47μF and 1μF is considered desirable taking video S/N, and AM and PM noise into consideration.	
24	AUDIO OUTPUT	Audio FM detector output. A 54kΩ resister is inserted in series with an emitter-follower output. For applications that support mono: Create an external de-emphasis circuit. t = C1 × R1