Ordering number : ENN7939B

SANYO Semiconductors

DATA SHEET

Monolithic Linear IC

LA7567BVA — TV and VCR IF Signal Processor (VIF + SIF + SIF converter)

The LA7567BVA is a PAL/NTSC multiformat VIF/SIF IC that adopts a semi-adjustment-free system. The VIF block adopts a system in which VCO adjustment makes AFT adjustment unnecessary to simplify adjustment. The FM detector adopts a PLL detection system that supports multi-detection audio. This IC also integrates an SIF converter, making design of multisystem products easier. The LA7567BVA uses the 5V supply voltage common in multimedia equipment. In addition, the LA7567BVA also includes a buzz canceller that suppresses Nyquist buzzing for superb audio quality.

Functions

- VIF block: VIF amplifier, buzz canceller, PLL detector, IF AGC, RF AGC, AFT, equalizer amplifier.
- First SIF block: First SIF amplifier, first SIF detector.
- SIF block: Limiter amplifier, PLL FM detector.

Features

- No AFT or SIF coils are required, making these circuits adjustment free.
- Allows PAL/NTSC multiformat systems to be implemented easily.
- Built-in buzz canceller for excellent audio quality.
- V_{CC} = 5V, low power: 250mW

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Rated value	Unit
Maximum supply voltage	V_{CC} max		6	V
Circuit voltage	V_{13}, V_{17}		V_{CC}	V
Circuit current	I_6		–3	mA
Allowable power dissipation	I_{10}		–10	
	I_{24}		–2	
	Pd max	Ta = ≤ 70°C, when mounted on a PCB*	600	mW
Operating temperature	T_{opr}		–20 to +70	°C
Storage temperature	T_{stg}		–55 to +150	°C

*: Printed circuit board: 114.3mm × 76.1mm × 1.6mm, glass epoxy board.

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Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Rated value	Unit
Recommended supply voltage	V_{CC}		5	V
Operating supply voltage	V_{CC} op		4.5 to 5.5	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 5V, fp = 38.9MHz

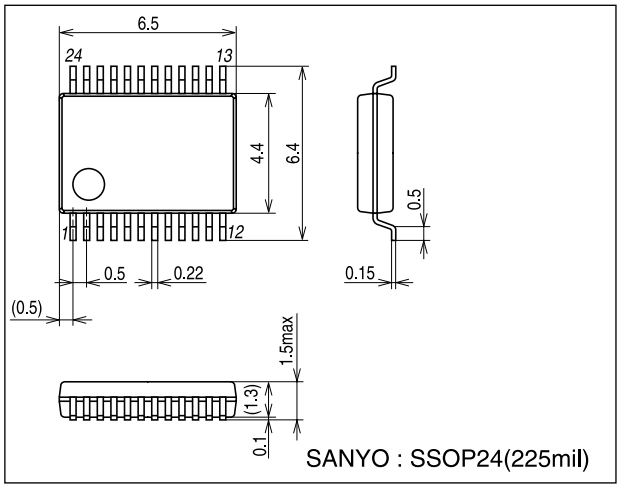
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[VIF Block]						
Circuit current	I_5		40.8	48	55.2	mA
Maximum RF AGC voltage	V_{14H}		V_{CC} –0.5	V_{CC}		V
Minimum RF AGC voltage	V_{14L}			0	0.5	V
Input sensitivity	V_I	S1 = OFF	27	33	39	dBµV
AGC range	G_R		58	63		dB
Maximum allowable input	V_I max		95	100		dBµV
No signal voltage output voltage	V_6		2.7	3.0	3.3	V
Sync. signal tip voltage	V_{6tip}		0.4	0.7	1.0	V
Video output level	V_O		1.7	2	2.3	Vp–p
Black noise threshold voltage	V_{BTH}		0.5	0.8	1.1	V
Black noise clamp voltage	V_{BCL}		1.6	1.9	2.2	V
Video SNR	S/N		48	52		dB
C-S beating	$I_{C–S}$		38	43		dB
Frequency characteristics	f_c	6MHz	–3	–1.5		dB
Differential gain	D_G			3	6.5	%
Differential phase	D_P			3	5	ºC
No signal AFT voltage	V_{13}		2.0	2.5	3.0	V
Maximum AFT voltage	V_{13H}		4.0	4.4	5.0	V
Minimum AFT voltage	V_{13L}			0.18	1.0	V
AFT detection sensitivity	S_f		17	25	34	mV/kHz
VIF input resistance	R_i	38.9MHz		1.5		kΩ
VIF input capacitance	C_i	38.9MHz		3		pF
APC pull-in range (U)	f_{pu}		0.7	1.5		MHz
APC pull-in range (L)	f_{pl}			–1.5	–0.9	MHz
AFT tolerance frequency	d_{fa1}		–250	0	+200	kHz
VCO 1 maximum variability (U)	d_{fu}		1.0	1.5		MHz
VCO 1 maximum variability (L)	d_{fl}			–1.5	–1	MHz
VCO control sensitivity	B		1.6	3.2	6.4	kHz/mV
Synchronization ratio	V_S		25.0	28.5	31.5	%
[First SIF Block]						
Conversion gain	V_G		22	28	32	dB
5.5MHz output level	S_O		32	70	110	mVrms
First SIF maximum input	S_i max		50	100		mVrms
First SIF input resistance	R_i (SIF)	33.4MHz		2		kΩ
First SIF input capacitance	C_i (SIF)	33.4MHz		3		pF
[SIF Block]						
Limiting sensitivity	V_{Ii} (lim)		42	48	54	dBµV
FM detector output voltage*	V_O (FM)	5.5MHz ± 30kHz	470	600	760	mVrms
AMR	AMR		50	60		dB
Total harmonic distortion	THD			0.3	0.8	%
SIF S/N	S/N (FM)		57	62		dB
[SIF Converter]						
Conversion gain	V_G (SIF)		8	11	14	dB
Maximum output level	V max		103	109	115	dBµV
Carrier suppression ratio	V_{GR} (5.5)		15	21		dB
Oscillator level	V_{OSC}		35	70		mVp–p
Oscillator leakage	OSC_{leak}		14	25		dB
Oscillator stop current	I_4				300	µA

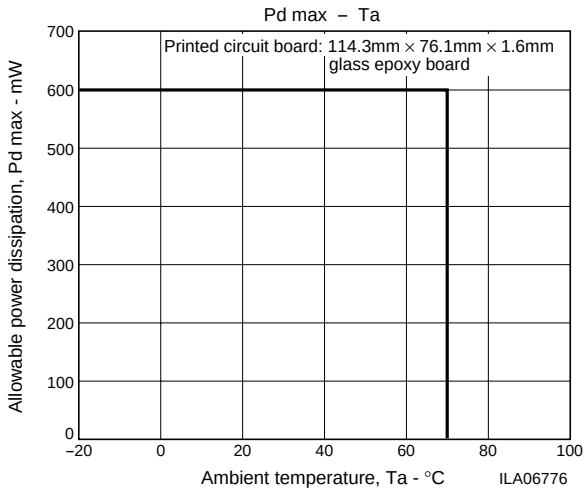
*: To acquire the maximum dynamic range from the FM detector, insert a resistor and capacitor in series between pin 23 and ground to adjust the level.

Package Dimensions

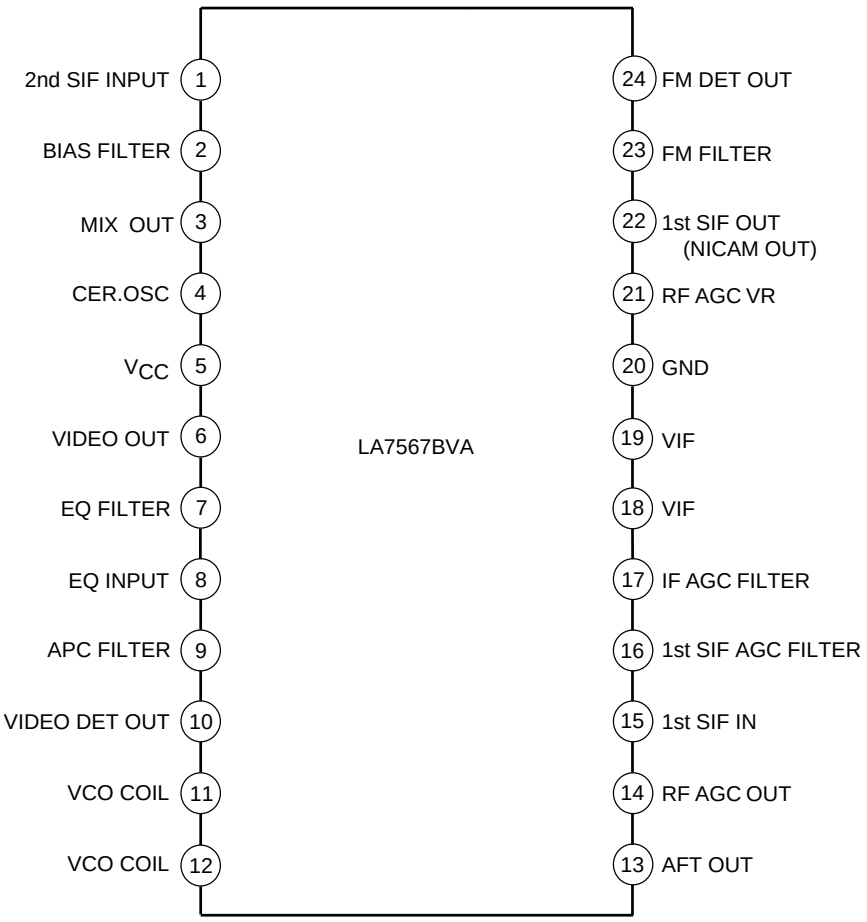
unit : mm

3287

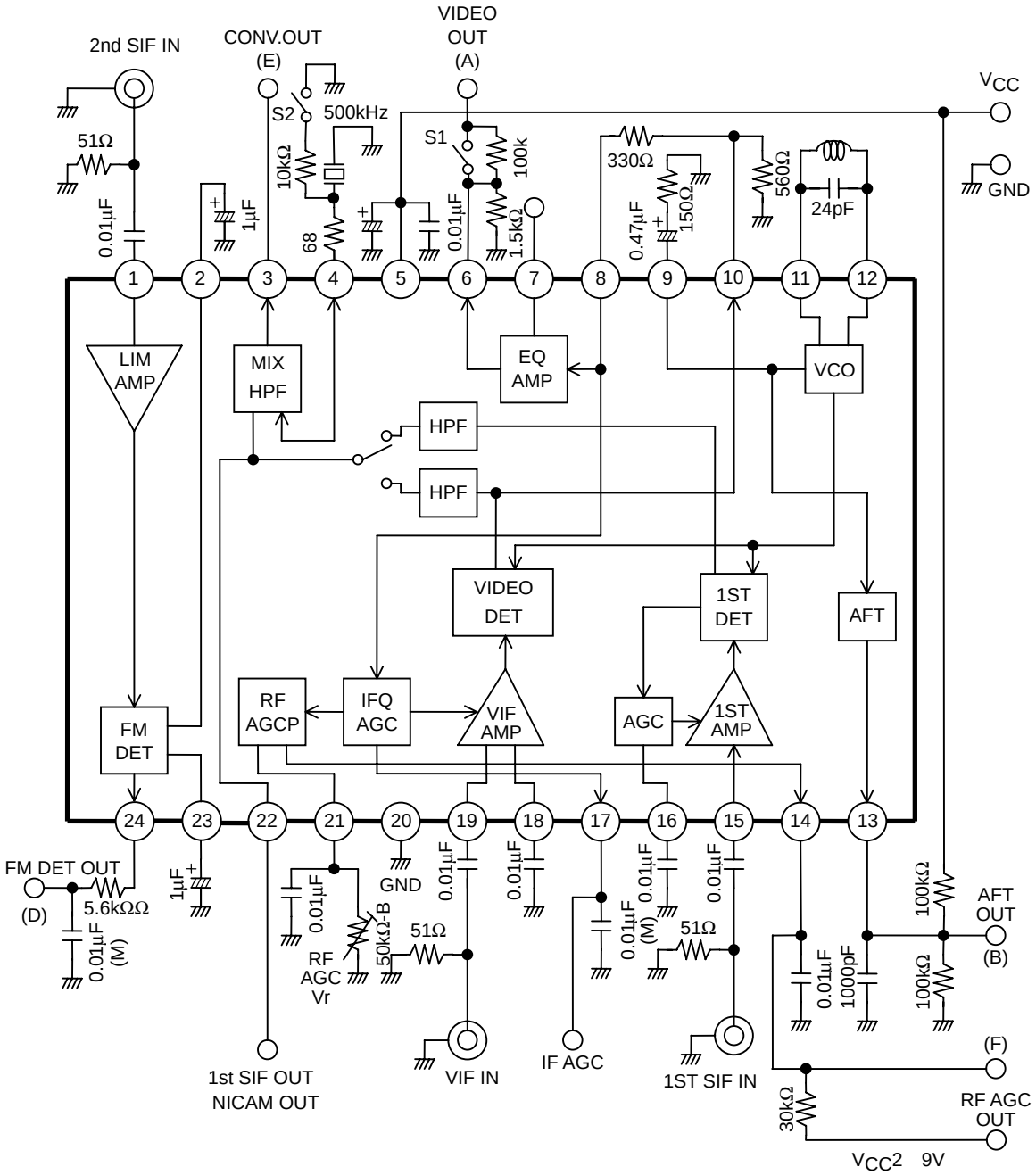




Pin Assignment

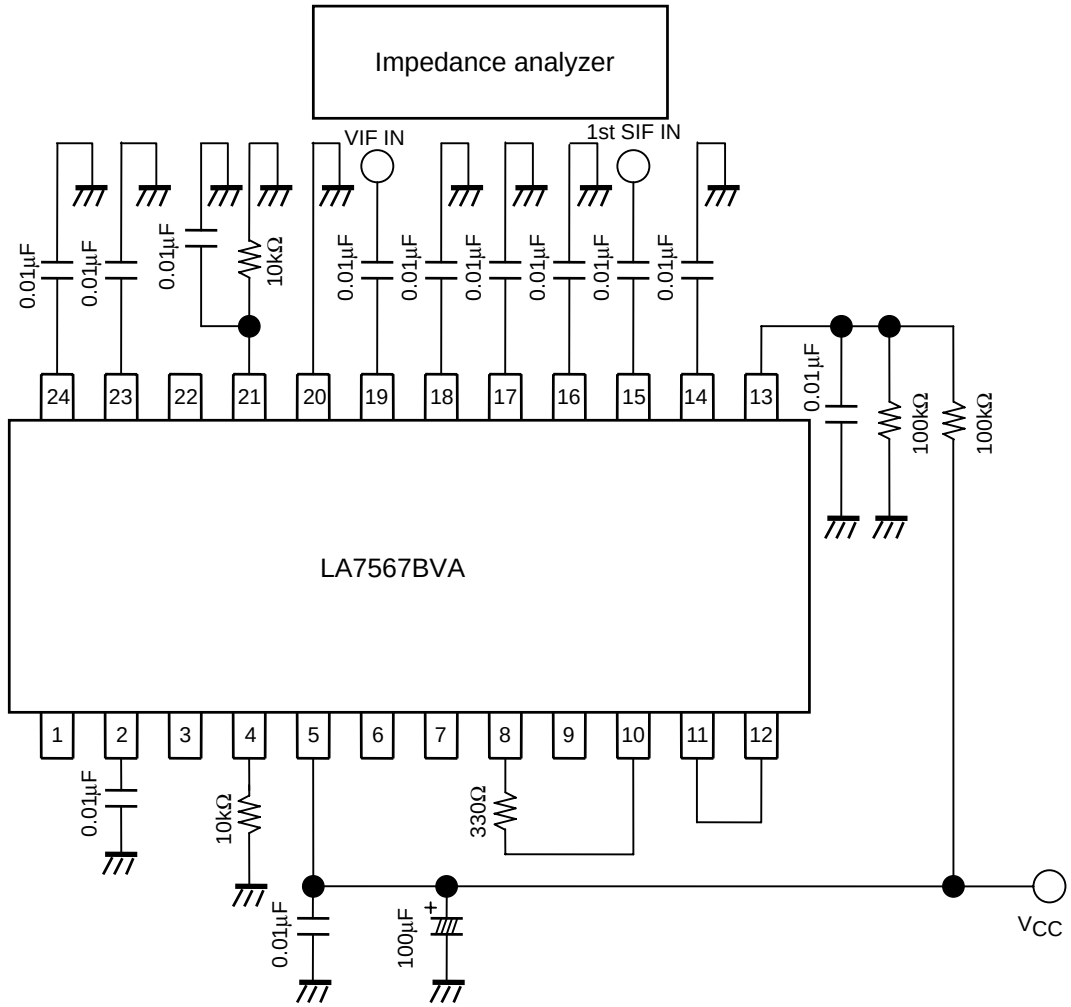


AC Characteristics Test Circuit



Test Circuits

Input Impedance Test Circuit (VIF and first SIF input impedance)



Test Conditions

V1. Circuit current . . . . . [I_5]

(1) Internal AGC
(2) Input a 38.9MHz 10mVrms continuous wave to the VIF input pin.
(3) RF AGC Vr MAX
(4) Connect an ammeter to the V_{CC} and measure the incoming current.

V2.V3. Maximum RF AGC voltage, Minimum RF AGC voltage . . . . . [V_{14H}, V_{14L}]

(1) Internal AGC
(2) Input a 38.9MHz 10mVrms continuous wave to the VIF input pin.
(3) Adjust the RF AGC Vr (resistor value max.) and measure the maximum RF AGC voltage. (F)
(4) Adjust the RF AGC Vr (resistor value min.) and measure the minimum RF AGC voltage. (F)

V4. Input sensitivity. . . . . [V_I]

(1) Internal AGC
(2) fp = 38.9MHz 400Hz 40% AM (VIF input)
(3) Turn off the S1 and put 100kΩ through.
(4) VIF input level at which the 400Hz detection output level at test point A becomes 0.64Vp-p.

V5. AGC range . . . . . [G_R]

(1) Apply the V_{CC} voltage to the external AGC IF AGC (pin 17).
(2) In the same manner as for the V4 (input sensitivity),measure the VIF input level at which the detection output level becomes 0.64Vp-p .....Vi1.
(3) $G_R = 20\log \frac{Vi1}{Vi}$ dB

V6. Maximum allowable input . . . . . [V_I max]

(1) Internal AGC
(2) fp = 38.9MHz 15 kHz 78% AM (VIF input)
(3) VIF input level at which the detection output level at test point A is video output (Vo) ±1dB

V7. No-signal video output voltage . . . . . [V_6]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) Measure the DC voltage of VIDEO output (A).

V8. Sync. signal tip voltage. . . . . [V_{6tip}]

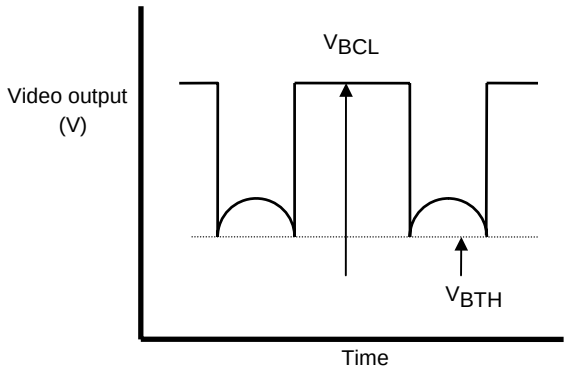
(1) Internal AGC
(2) Input a 38.9MHz 10mVrms continuous wave to the VIF input pin.
(3) Measure the DC voltage of VIDEO output (A).

V9. Video output level . . . . . [V_O]

(1) Internal AGC
(2) fp = 38.9MHz 15kHz 78% AM Vi = 10mVrms (VIF input)
(3) Measure the peak value of the detection output level at test point A. . . . . Vp-p

V10.V11. Black noise threshold level and clamp voltage . . . . . [V_{BTH}, V_{BCL}]

(1) Apply DC voltage to the external AGC, IF AGC (pin 17) and adjust the voltage.
(2) fp = 38.9MHz 400Hz 40% AM10mVrms (VIF input)
(3) Adjust the IF AGC (pin 17) voltage to operate the noise canceller.
Measure the V_{BTH}, V_{BCL} at test point A.

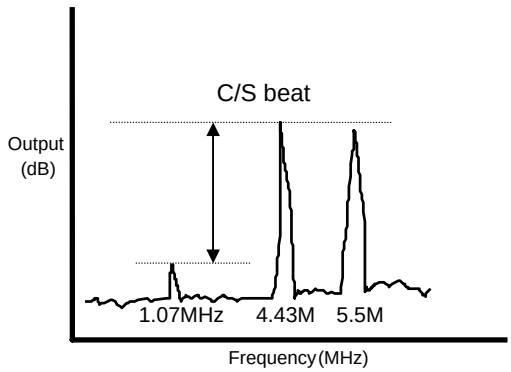


V12. Video S/N . . . . . [S/N]

(1) Internal AGC
(2) fp = 38.9MHz CW = 10mVrms (VIF input)
(3) Measure the noise voltage at test point A in RMS volts through a 10kHz to 4MHz band-pass filter.
.....Noise voltage (N)
(4) $S/N = 20 \log \frac{\text{Video portion (Vp-p)}}{\text{Noise voltage (Vrms)}} = 20 \log \frac{1.12\text{Vp-p}}{\text{Noise voltage (Vrms)}}$ (dB)

V13. C/S beat . . . . . [I_{CS}]

(1) Apply DC voltage to the external AGC IF AGC (pin 17) and adjust the voltage.
(2) fp = 38.9MHz CW;10mVrms
fc = 34.47MHz CW;10mVrms-10dB
fs = 33.4MHz CW;10mVrms-10dB
(3) Adjust the IF AGC (pin 17) voltage so that the output level at test point A becomes 1.3Vp-p.
(4) Measure the difference between the levels at 4.43MHz and 1.07MHz.



V14. Frequency characteristics . . . . . [f_C]

(1) Apply DC voltage to the external AGC IF AGC (pin 17) and adjust the voltage.
(2) SG1 : 38.9MHz continuous wave 10mVrms
SG2 : 38.8MHz to 32.9MHz continuous wave 2mVrms
Add the SG1 and SG2 signals using a T pat and adjust each SG signal level so that the above-mentioned levels are reached and input the added signals to the VIF IN.
(3) First set the SG2 frequency to 38.8MHz, and then adjust the IF AGC voltage (V17) so that the output level at test point A becomes 0.5Vp-p..... V1
(4) Set the SG2 frequency to 32.9MHz and measure the output level.....V2
(5) Calculate as follows:

$$f_C = 20\log \frac{V2}{V1} \text{ (dB)}$$

V15.V16. Differential gain, differential phase . . . [D_G, D_P]

(1) Internal AGC
(2) fp = 38.9MHz ALP 50% 87.5% modulation video signal Vi = 10mVrms
(3) Measure the DG and DP at test point A

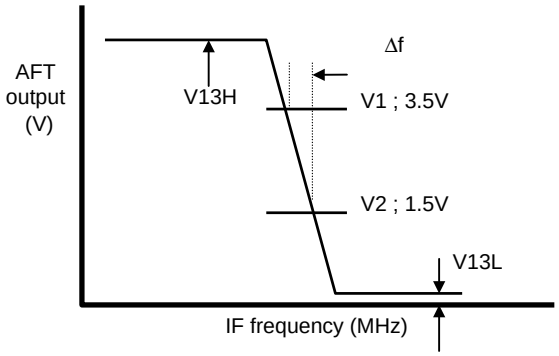
V17. No signal AFT voltage. . . . . [V_{13}]

(1) Internal AGC
(2) Measure the DC voltage at the AFT output (B).

V18.V19.V20. Maximum minimum AFT output voltage, AFT detection sensitivity . . . . [V_{13H}, V_{13L}, S_f]

(1) Internal AGC
(2) fp = 38.9MHz ±1.5MHz Sweep = 10mVrms (VIF input)
(3) Maximum voltage: V_{13H}, minimum voltage: V_{13L}
(4) Measure the frequency deviation at which the voltage at test point B changes from V1 to V2.
.....Δf

$$Sf = \frac{2000(mV)}{\Delta f\,(kHz)}\ mV/kHz$$



V21.V22. VIF input resistance, Input capacitance. . . . . [R_i, C_i]

(1) Referring to the input impedance Test Circuit, measure Ri and Ci with an impedance analyzer.

V23.V24. APC pull-in range. . . . . [f_{pu}, f_{pl}]

(1) Internal AGC
(2) fp = 33MHz to 44MHz continuous wave;10mVrms
(3) Adjust the SG signal frequency to be higher than fp = 38.9MHz to bring the PLL to unlocked state.
Note: GThe PLL is assumed to be in unlocked state when a beat signal appears at test point A.
(4) When the SG signal frequency is lowered, the PLL is brought to locked state again. .....(f1)
(5) Lower the SG signal frequency to bring the PLL to unlocked state.
(6) When the SG signal frequency is raised, the PLL is brought to locked state again. .....(f2)
(7) Calculate as follows:
f_{pu} = f1 - 38.9MHz
f_{pl} = f2 - 38.9MHz

V25. AFT tolerance frequency . . . . . [ΔFa1]

(1) Internal AGC
(2) SG1 : 37.9MHz to 40.9MHz variable continuous wave 10mVrmns
(3) Adjust the SG1 signal frequency so that the AFT output DC voltage (test point B) becomes 2.5V; that SG1 signal frequency is f1.
(4) External AGC (Adjust the V17.)
(5) Apply 5V to the IFAGC (pin 17) and then pick up the VCO oscillation frequency from GND, etc. and measure the frequency (f2)
(6) Calculate as follows:
AFT tolerance frequency ΔFa1 = f2 - f1(kHz)

V26.V27. VCO Maximum variable range(U, L) . . . [d_{fu}, d_{fl}]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) Pick up the VCO oscillation frequency from the VIDEO output (A), GND, etc. and adjust the VCO coil so coil that the frequency becomes 38.9MHz.
(3) fl is taken as the frequency when 1V is applied to the APC pin (pin 9). In the same manner, fu is taken as the frequency when 5V is applied to the APC pin (pin 9).
d_{fu} = fu - 38.9MHz
d_{fl} = fl - 38.9MHz

V28. VCO control sensitivity . . . . . [β]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) Pick up the VCO oscillation frequency from the VIDEO output (A), GND, etc. and adjust the VCO coil so that the frequency becomes 38.9MHz.
(3) f1 is taken as the frequency when 3.0V applied to the APC pin (pin 9). In the same manner, f2 is taken as the frequency when 3.4V is applied to the APC pin (pin 9).

$$\beta = \frac{f2 - f1}{400} \left(\text{kHz}/\text{mV}\right)$$

V29. Synchronization ratio . . . . . [V_S]

(1) Internal AGC
(2) fp = 38.9MHz 87.5% 10STEP B/W
Vi = 10mVrms
(3) Measure the output amplitude at the measuring point A . . . . . Vvideo
(4) Measure the pedestal voltage (DC) at the measuring point A . . . . . Vped
V_S = (Vped-V6tip)/Vvideo × 100 (%)

F1. First SIF conversion gain . . . . . [V_G]

(1) Internal AGC
(2) fp = 38.9MHz CW; 10mV (VIF input)
fs = 33.4MHz CW; 500μV (First SIF input) V1
(3) Detection output level at test point C (Vrms) V2 (5.5MHz)
(4) $V_G = 20\log \frac{V2}{V1}$ dB

F2. 5.5MHz output level . . . . . [S_O]

(1) Internal AGC
(2) fp = 38.9MHz CW; 10mV (VIF input)
fs = 33.4MHz CW; 10mV (First SIF input) V1
(3) Detection output level at test point C (5.5MHz) . . . . . S_O (mVrms)

F3. First SIF maximum input. . . . . [$S_i$max]

(1) Internal AGC
(2) fp = 38.9MHz CW;10mV (VIF input)
fs = 33.4MHz CW;variable (First SIF input)
(3) Input level at which the detection output at test point C (5.5MHz) becomes So ±2dB.....$S_i$max

F4. F5. First SIF input resistance, input capacitance . . . . [R_i(SIF1), C_i(SIF1)]

(1) Using an input analyzer, measure Ri and Ci in the input impedance measuring circuit.

S1. SIF limiting sensitivity. . . . . [V_{Ii}(lim)]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) fs = 5.5MHz fm = 400Hz ΔF = ±30kHz (SIF input)
(3) Set the SIF input level to 100mVrms and then measure the level at test point D.....V1
(4) Lower the SIF input level until V1-3dB occurs. Measure the input level at that moment.

S2. S4. FM detection output voltage, distortion factor . . . [V_O(FM, THD)]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) fs = 5.5MHz fm = 400Hz ΔF = ±30kHz
(SIF input Vi = 100mVrms)
(3) Assign the level at test point D to the FM detection output voltage and measure the distortion factor.

S3. AM rejection ratio . . . . . [AMR]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) fs = 5.5MHz fm = 400Hz AM = 30%
(SIF input Vi = 100mVrms)
(3) Measure the output level at test point D.....VAM
(4) $AMR = 20\log \frac{VO(DET)}{VAM}$ dB

S5. SIF S/N . . . . . [S/N]

(1) External AGC (V17 = V_{CC})
(2) fs = 5.5MHz NO MOD Vi = 100mVrms
(3) Measure the output level at test point D.....Vn
(4) $S/N = 20\log \frac{VO(DET)}{Vn}$ dB

C1. Converter conversion gain. . . . . V_G(SIF)

(1) Internal AGC
(2) fp = 38.9MHz CW; 10mV (VIF input)
fs = 33.4MHz CW; 316μV (First SIF input)
(3) Measure the 6MHz component at test point E (MIX output). V1
(4) Measure the 5.5MHz component at test point F (NICAM output). V2
(5) V_G mix $= 20\log \frac{V1}{V2}$ dB

C2. SIF converter maximum output level . . . . . [V_{max}]

(1) Internal AGC
(2) fp = 38.9MHz CW; 10mV (VIF input)
fs = 33.4MHz CW; 10mV (First SIF input)
(3) Measure the 6MHz component at test point E (MIX output). .....V_{max}(dBμV)

C3. Carrier suppression ratio (V_{GR}(5.5))

(1) Internal AGC
(2) fp = 38.9MHz CW; 10 mV (VIF input)
fs = 33.4MHz CW; 316 μV (First SIF input)
(3) Measure the 6MHz component at test point E (MIX output). .....V6 (dBμV)
(4) Measure the 5.5MHz component at test point E (MIX output). .....V5.5 (dBμV)
(5) Perform the following calculation.
Carrier suppression ratio V_{GR}(5.5)(dB) = V6 - V5.5

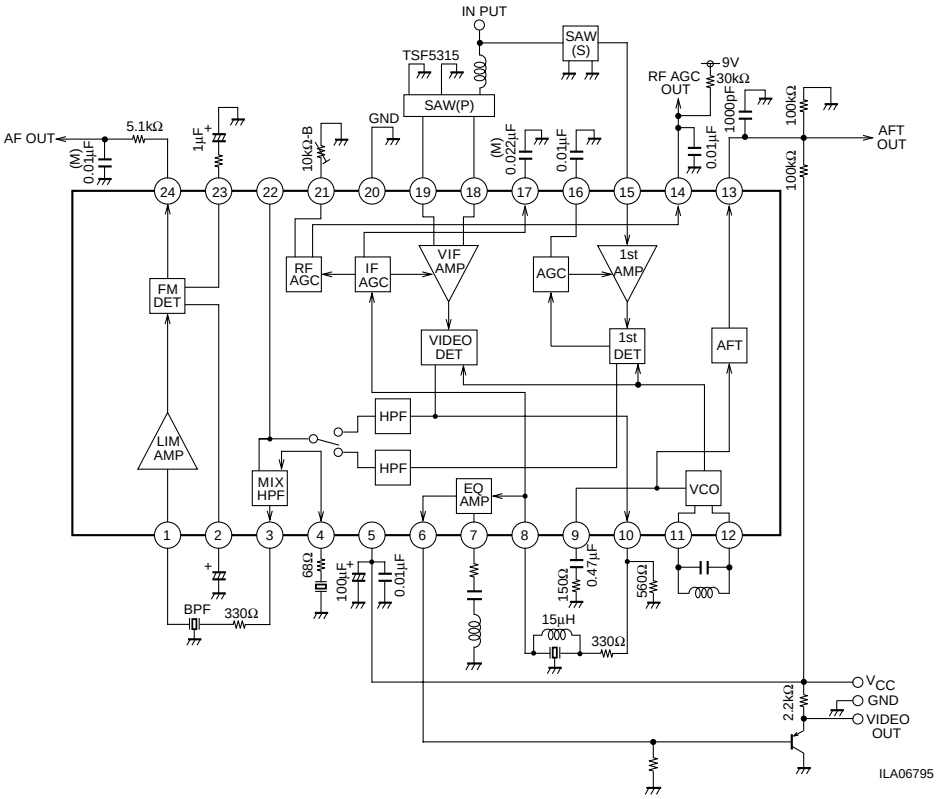
C5. OSC leakage (OSC_{leak})

(1) Internal AGC
(2) fp = 38.9MHz CW; 10mV (VIF input)
fs = 33.4MHz CW; 316μV (First SIF input)
(3) Measure the 6MHz component at test point E (MIX output). .....V6(dBμV)
(4) Measure the 500kHz component at test point E (MIX output). .....V0.5(dBμV)
(5) Perform the following calculation.
Carrier suppression ratio OSC_{leak}(dB) = V6 - V0.5

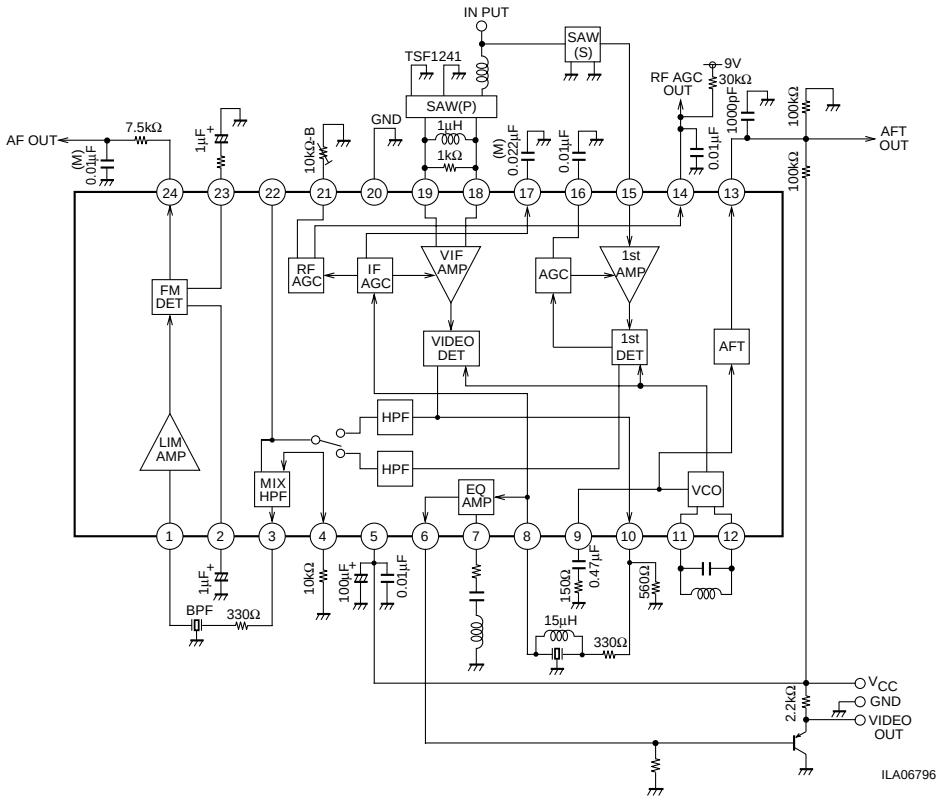
Note 1) Unless otherwise specified for VIF test, apply the V_{CC} voltage to the IF AGC and adjust the VCO coil so that oscillation occurs at 38.9MHz.
Note 2) Unless otherwise specified, the SW1 must be ON.

Application Circuits

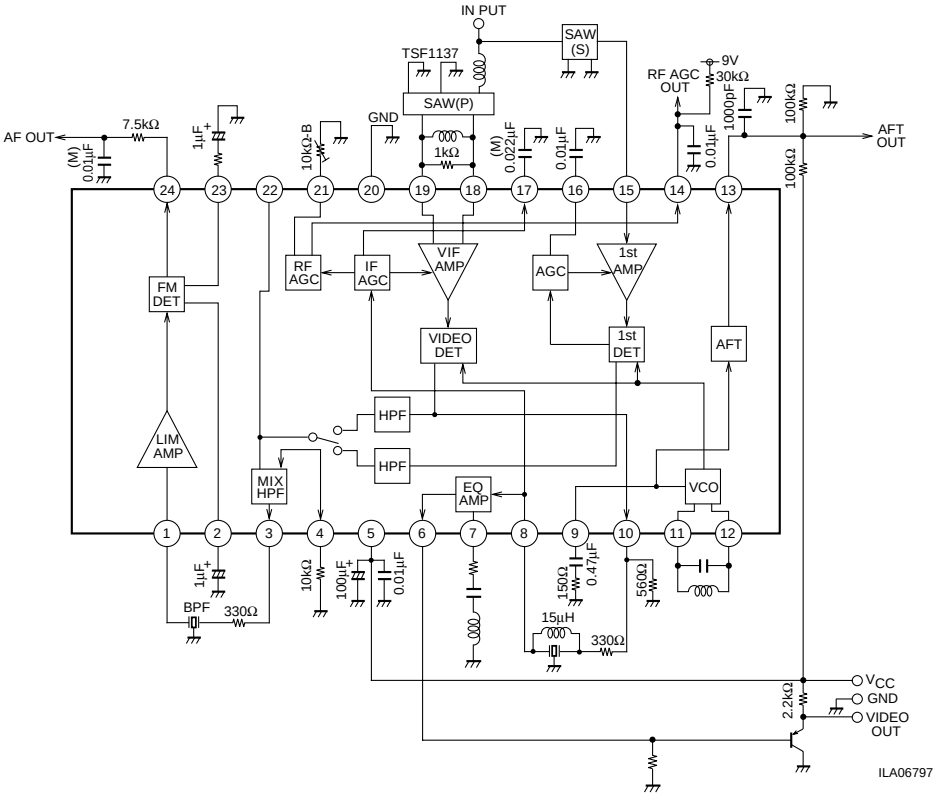
PAL SPLIT



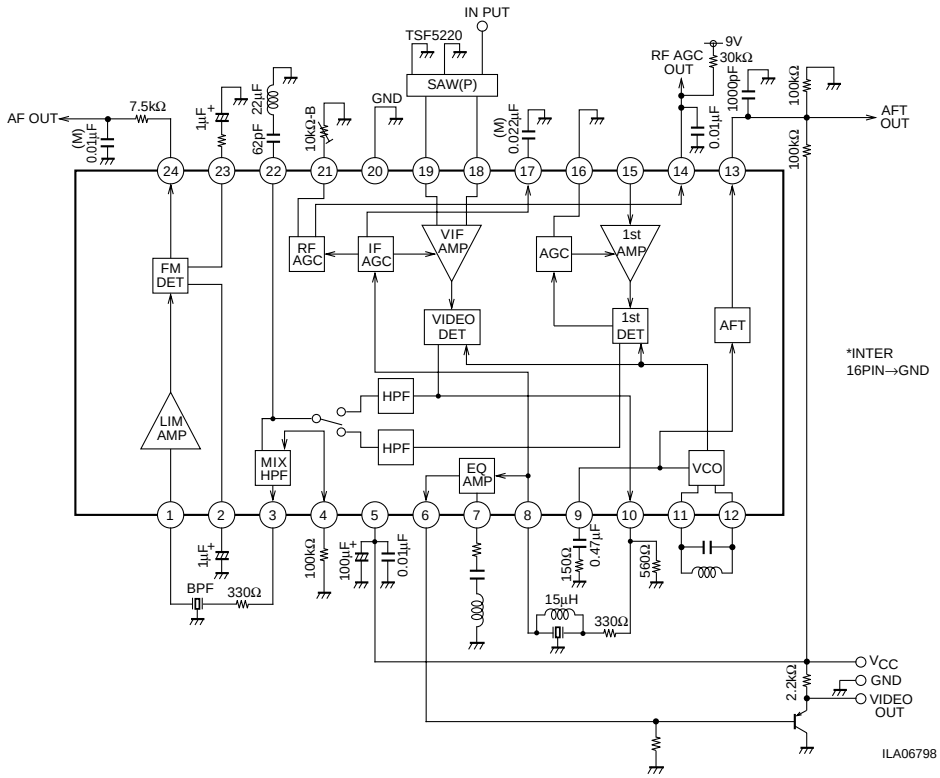
NT (US) SPLIT



JAPAN SPLIT



NT (US) INTER



Application Circuit Example

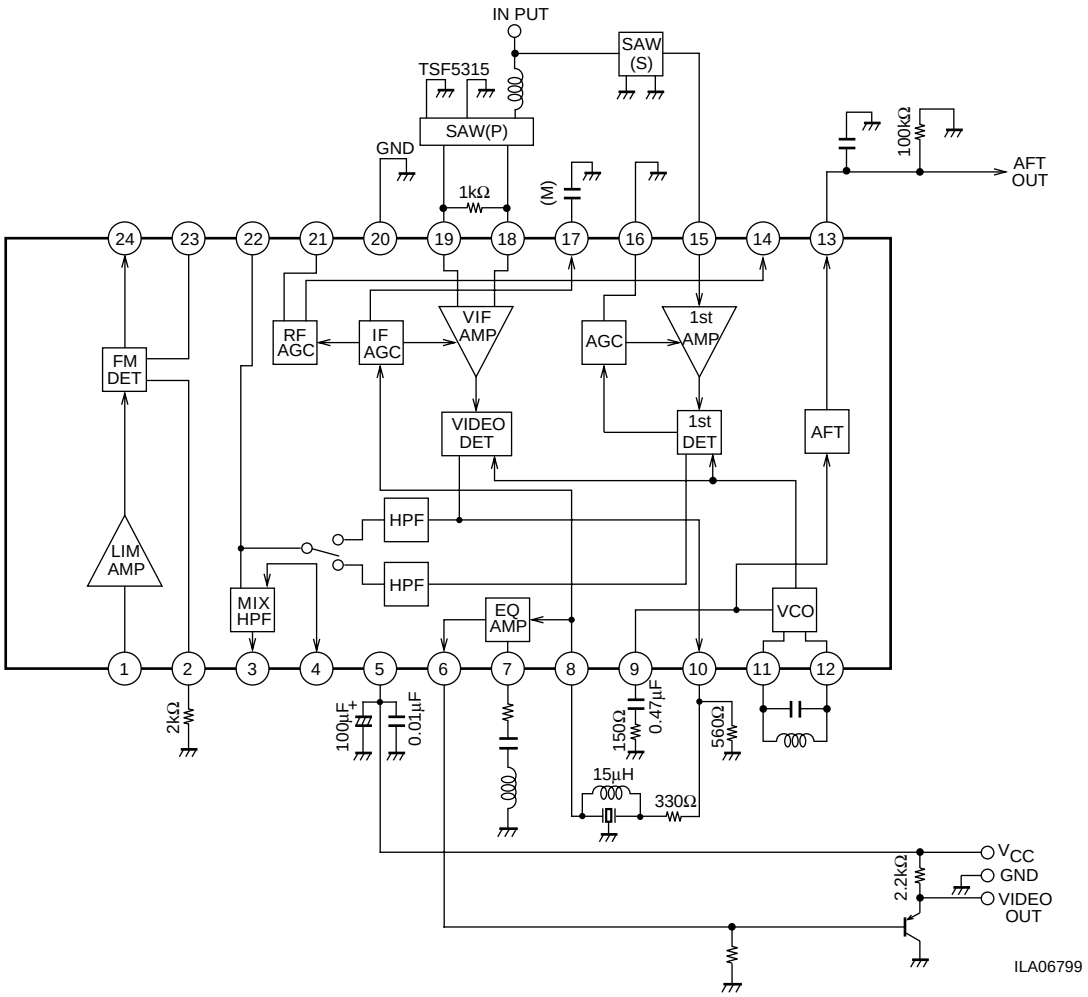
When the SIF, first SIF, AFT, and/or RF AGC are not used

(1) When the SIF circuit is not used
Leave pins 1, 23, and 24 open.
Insert a 2kΩ resistor between pin 2 and ground.

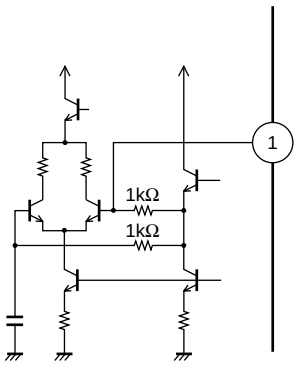
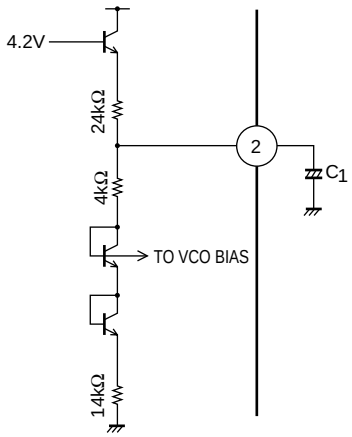
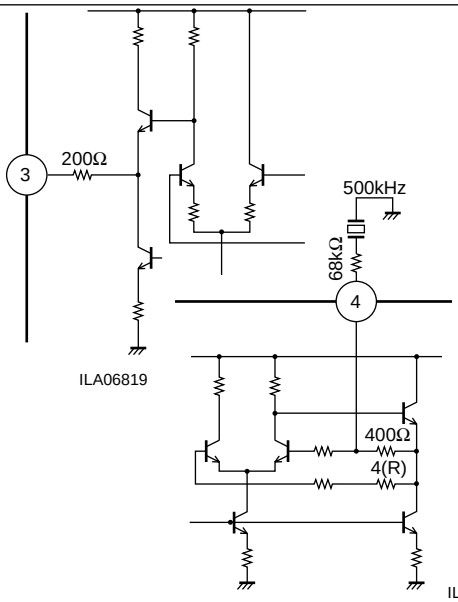
(2) When the first SIF circuit is not used
Leave pins 3, 4, 22, and 15 open.
Connect pin 16 to ground.

(3) When the AFT circuit is not used
Since there is no way to defeat the AFT circuit, insert a 100kΩ resistor and a 0.01µF capacitor in parallel between pin 13 and ground.

(4) When the RF AGC circuit is not used
Leave pins 14 and 21 open.
Insert a 0.01µF capacitor between pin 21 and ground to prevent oscillation.



Pin Descriptions

Pin No.	Pin	Description	Equivalent circuit
1	SIF INPUT	The input impedance is about 1kΩ. If interference* enters at this pin, it can cause buzzing and beating. The PCB pattern layout must be designed to minimize interface at this pin. *: Signals that can cause interface with the audio include video signals and the chroma signal. Signal such as the VIF carrier can also cause interference.	 ILA06800
2	FM power supply filter	The FM detector signal-to-noise ratio can be improved by inserting an FM detector bias line filter. If the FM detector with C1 (0.47µF or larger: the recommended value is 1µF) is not used, pin 2 must be connected to ground through a 2kΩ resistor. This stops the FM detector VCO circuit.	 ILA06801
3 4	SIF converter	Pin 3 is the SIF converter output. This signal is passed through a 6MHz bandpass filter and input to the SIF block. This is an emitter-follower output with a 200Ω series resister inserted in the output. Pin 4 is the SIF converter's 500kHz oscillator connection. Since this oscillator circuit includes an ALC, the oscillator level is low and is controlled to be a fixed level. If this circuit is not used, insert a 10kΩ resistor between pin 3 and ground. Connecting this external resistor stops the 500kHz oscillator and allows the converter to be used as an amplifier.	 ILA06819 ILA06802
5	V_{CC}	• The decoupling capacitor between V_{CC} and ground must be connected with the shortest lines possible.	

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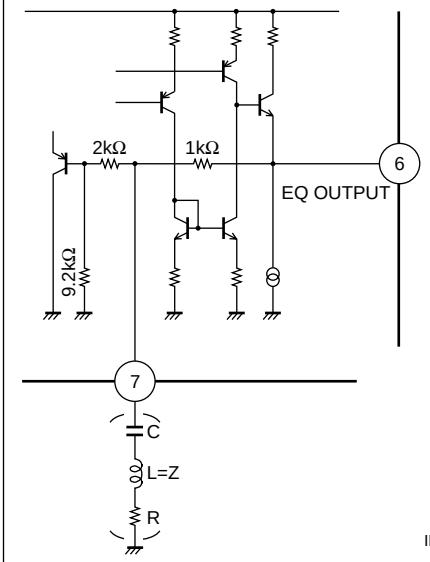
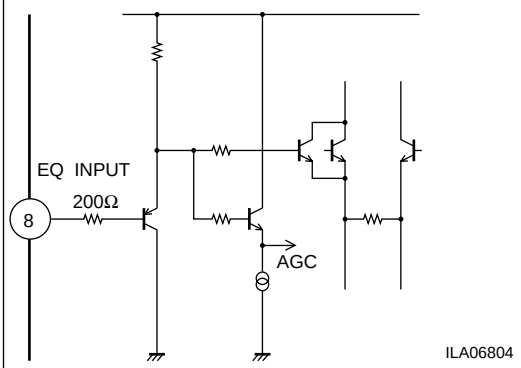
<table>
<tr><th>Pin No.</th><th>Pin</th><th>Description</th><th>Equivalent circuit</th></tr>
<tr>
<td>6
7
8</td>
<td>EQ amp</td>
<td>Equalizer circuit
This circuit corrects the video signal frequency characteristics.
Pin 8 is the equalizer amplifier input.
A 1.5Vp-p signal is input and the equalizer amplifier amplifies it to 2Vp-p.
• Equalizer amplifier design
The equalizer amplifier is designed as a voltage follower with about 2.3dB of gain. Insert an inductor, a capacitor, and a resistor in series between pin 7 and ground if frequency characteristics correction is required.
• Equation amplifier notes
If vi is the input signal and vo the output, this amplifier operates as follows.
$\frac{R1}{Z}+1\ (vi + vin) = Vo \times G$
G: Voltage follower amplifier gain
vin: Imaginary short
G: About 2.3dB
Assuming vin is close to 0:
$AV = \frac{voG}{vi} = \frac{R1}{Z} + 1$
R1 is an IC internal resistor, and is 1kΩ. Z may be chosen to match the desired characteristics. However, since the equalizer amplifier gain is at its maximum at Z's resonance point, care is required to assure that distortion does not occur.</td>
<td> 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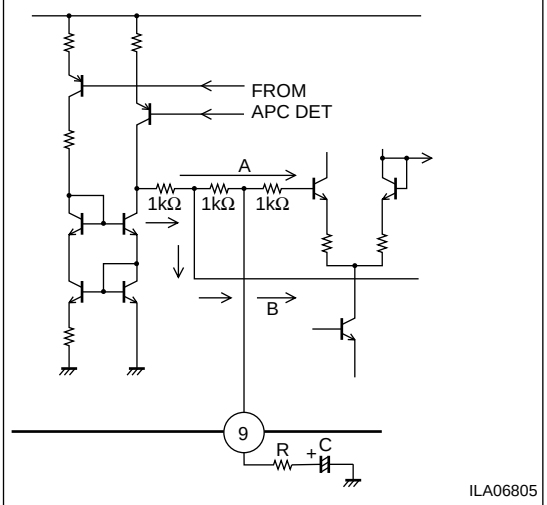
</tr>
<tr>
<td>9</td>
<td>APC FILTER</td>
<td>PLL detector APC filter connection
The APC time constant is switched internally in the IC. When locked, the VCO is controlled by the route A and the loop gain is lowered.
When unlocked and during weak field reception, the VCO is controlled by the route B and the loop gain is increased.
R = 150 to 390Ω
0.47μF is the recommended value for C.</td>
<td> 
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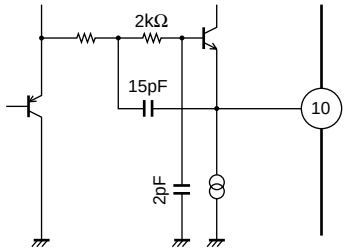
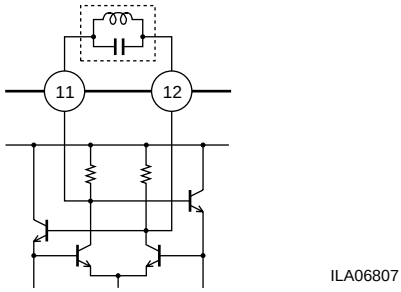
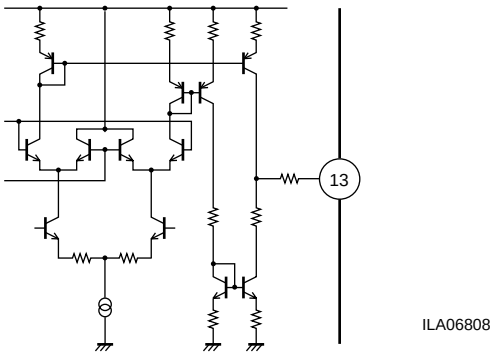
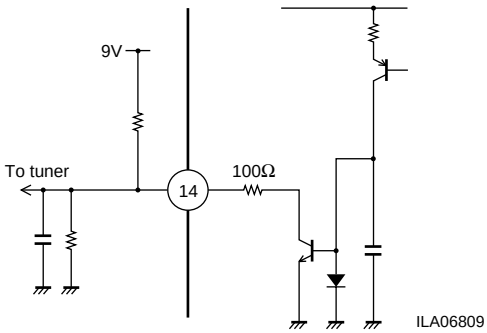
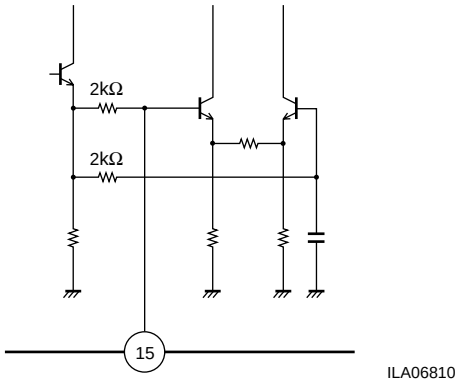
Pin No.	Pin	Description	Equivalent circuit
10	Composite video output	Video output (including the SIF carrier) pin. A resistor must be inserted between pin 10 and ground to acquire the pin circuit's drive capability. R ≥ 300Ω	
11 12	VCO tank	Video detector VCO tank circuit connection. See the coil specifications provided separately for details on this tank circuit. This is a vector synthesis VCO circuit.	
13	AFT OUTPUT	AFT output The AFT center voltage is created by an external bleeder resistor. The AFT gain is increased by increasing the value of this external bleeder resistor. The resistor value must be limited to be no more than 390Ω. This IC includes a function that controls the AFT voltage to naturally go to the center voltage during weak field reception.	
14	RF AGC OUTPUT	RF AGC output This output controls the tuner RF AGC. A 100Ω protective resistor is inserted in series with this open collector output. Determine the value of the external bleeder resistor by referring to the tuner specifications.	
15	1st SIF INPUT	First SIF input A capacitor must be used to cut the DC component of the input to this input circuit. • When a SAW filter is used: The first SIF sensitivity can also be increased by inserting an inductor between the SAW filter and the IC to neutralize the SAW filter output capacitance and the IC input capacitance. • If this IC is used with an intercarrier, this pin (pin 15) may be left open.	

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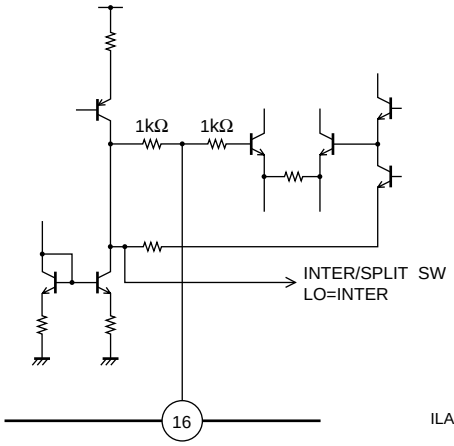
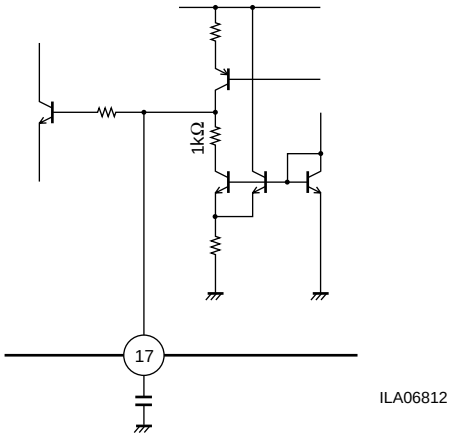
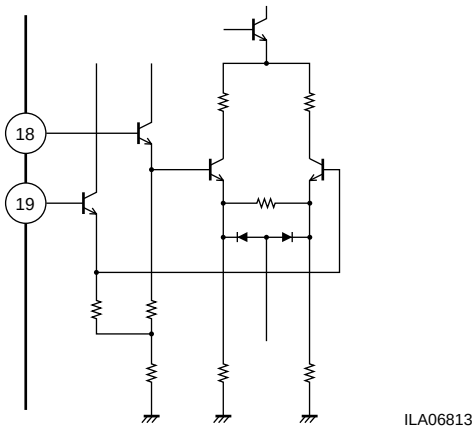
Pin No.	Pin	Description	Equivalent circuit
16	1st SIF AGC FILTER	First SIF AGC filter connection This IC adopts an average value AGC system. The first SIF conversion gain is about 30dB and the AGC range is over 50 dB. Normally, a 0.01µF capacitor should be used for the filter at this pin. • If an intercarrier is used, connect this pin to ground. An IC internal switch will be set so that the intercarrier output becomes the SIF converter input.	
17	IF AGC FILTER	IF AGC filter connection The signal which is peak detected by the internal AGC detector is converted to the AGC voltage at pin 17. Furthermore, this IC includes a second AGC filter (lag-lead filter) used to create the dual time constants internally in the IC. Use a 0.022µF capacitor as this external capacitor. However, this capacitor value must be adjusted according to the sag, AGC peak, and other characteristics.	
18 19	VIF input	VIF amplifier input This input circuit is a balanced input and the input impedance corresponds to the following values. R = 1.5kΩ C = 3pF	
20	GND		

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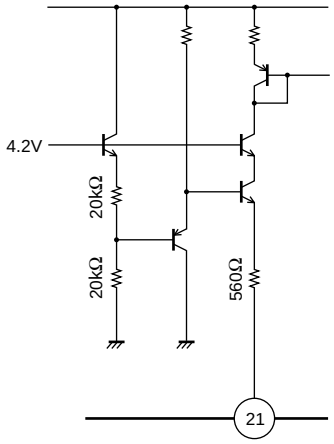
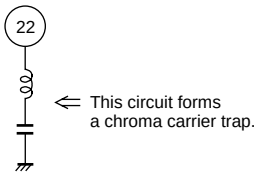
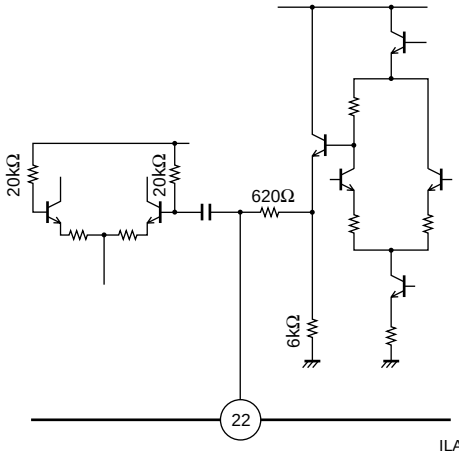
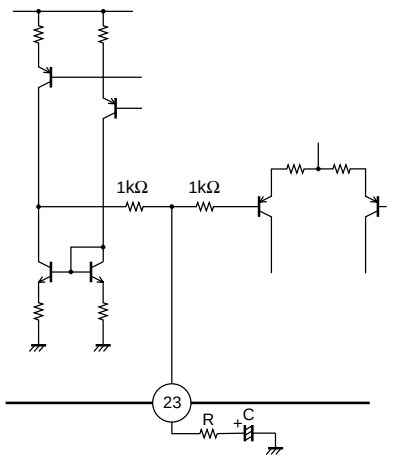
Pin No.	Pin	Description	Equivalent circuit
21	RF AGC VR	RF AGC VR connection This pin sets the tuner RF AGC operating point. The FM output and the video output can be muted at the same time by connecting this pin to ground.	
22	NICAM output	First SIF output The input circuit includes a 600Ω resistor in the emitter-follower output. If an intercarrier is used, the buzz characteristics can be improved by forming a chroma carrier trap on this pin. 	
23	FM filter	Connection for the filter that holds the FM detector output voltage fixed. Normally, a 1µF electrolytic capacitor is used. If there are problems with the low band (around 50Hz) frequency characteristics, this capacitor value should be increased. The FM detector output level can be reduced and the FM dynamic range increased by inserting a resistor between pin 23 and ground in series with the capacitor 0.	
24	FM Detector output	Audio FM detector output There is an internal 300Ω resistor in series with this emitter-follower output. • Stereo applications Certain stereo decoder input applications have a low input impedance, and this can cause distortion in the left and right signals and degrade the stereo characteristics. If that is the case, add a resistor between pin 24 and ground. $R1 \geq 5.1k\Omega$ • Mono applications Form an external deemphasis circuit at this pin. $T = 2 \times C \times R$