Ordering number : ENA0258

SANYO Semiconductors
DATA SHEET

LA79200V — Monolithic Linear IC For extention of I²C-BUS compatible microcomputer I/O port

Overview

This LA79200V is a for extention of I²C-BUS compatible microcomputer I/O port.

Functions

- 8 bit Expanded I/O port with LED Driver
- 2 bit DAC×2

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_1 max		7.0	V
Allowable power dissipation	Pd max	Ta ≤ 65°C *	300	mW
Operating temperature	Topr		-10 to +65	°C
Storage temperature	Tstg		-55 to +150	°C

* Mounted on a board : 114.3×76.1×1.6mm³, glass epoxy.

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_1		5.0	V
Operating supply voltage range	V_1 op		4.5 to 5.5	V

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Electrical Characteristics at Ta = 25°C, V_1 = 5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Circuit voltage, current]						
Supply current	I_1	V_1=5V	7.2	8.0	8.8	mA
Supply voltage	V_1		4.5	5.0	5.5	V
[SCL input/SDA input output]						
LOW level input voltage	ViL		0		0.8	V
HIGH level input voltage	ViH		3.5		5.0	V
DATA saturation voltage	VDAsat				0.35	V
[I/O s]						
LOW level input voltage	VIOiL		0		0.8	V
HIGH level input voltage	VIOiH		3.5		5.0	V
LOW level saturation voltage	VIOsat				0.35	V
[Slave address select]						
LOW level input voltage	VAiL		0		0.8	V
[D/A output]						
D/A LOW level output voltage	VDAL		0		0.3	V
D/A MID1 level output voltage	VDAM1		1.7	2	2.3	V
D/A MID2 level output voltage	VDAM2		2.7	3	3.3	V
D/A HIGH level output voltage	VDAH		3.8	4.1	4.4	V

Notes

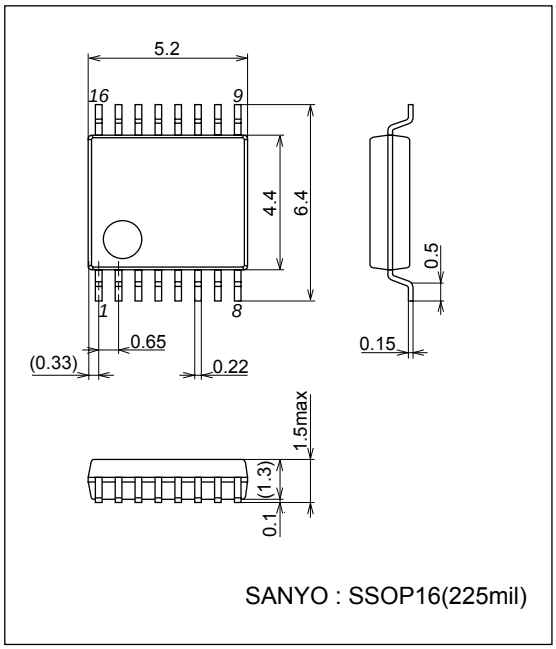
(1) Write “Hi” in the register of each port with IIC Bus when using each port as an input.

(2) Clock rate of IIC Bus can be used at 400kHz or less.

Package Dimensions

unit : mm

3178B



SANYO : SSOP16(225mil)

Test Conditions at Ta = 25°C, V_{CC} = V_1 = 5.0V

Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
[Circuit voltage, current]					
Supply current (pin 1)	I_1	(1)	IC Add: 0111 1100 Sub Add: 0000 0000 Data Add: 0000 0000	Apply a voltage of 5.0V to pin 1 and measure the incoming DC current (mA).	Initial
[SCL input/SDA input output]					
LOW level input voltage	ViL	15 16	IC Add: 0111 1100 Sub Add: 0000 0000 Data Add: 0000 0000	Measure the DC voltage at LOW level of the signal entered in pins 15 and 16.	Initial
HIGH level input voltage	ViH	15 16	IC Add: 0111 1100 Sub Add: 0000 0000 Data Add: 0000 0000	Measure the DC voltage at HIGH level of the signal entered in pins 15 and 16.	Initial
DATA pin saturation voltage	VDAsat	16	IC Add: 0111 1101	Allow 3.3mA to flow through DATA pin and measure the DC voltage when ACK is returned.	Initial
[I/O s]					
LOW level input voltage	VIOiL	5 to 8 10 to 13	IC Add: 0111 1100 Sub Add: 0000 0000 Data Add: 0000 0000	Measure the DC voltage of pins 5 to 8 and 10 to 13.	Initial
HIGH level input voltage	VIOiH	5 to 8 10 to 13	IC Add: 0111 1100 Sub Add: 0000 0000 Data Add: 1111 1111	Measure the DC voltage of pins 5 to 8 and 10 to 13.	PEX0:1 PEX1:1 PEX2:1 PEX3:1 PEX4:1 PEX5:1 PEX6:1 PEX7:1

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Parameter	Symbol	Test point	Input signal	Test method	Bus conditions
LOW level saturation voltage	VIOsat	5 to 8, 10 to 13	IC Add: 0111 1100 Sub Add: 0000 0000 Data Add: 0000 0000	Measure the DC voltage when 3.3mA is allowed to flow through pin 13.	Initial
[D/A output]					
D/A output voltage H	VDAH	2, 3	IC Add: 0111 1100 Sub Add: 0000 0001 Data Add: 0000 0000	Measure the DC voltage of pins 5 to 8 and 10 to 13.	Initial
D/A output voltage MID2	VDAM2	2, 3	IC Add: 0111 1100 Sub Add: 0000 0001 Data Add: 0100 0100	Measure the DC voltage of pins 5 to 8 and 10 to 13.	DA.OUTPUT_1:1 DA.OUTPUT_2:1
D/A output voltage MID1	VDAM1	2, 3	IC Add: 0111 1100 Sub Add: 0000 0001 Data Add: 1000 1000	Measure the DC voltage of pins 5 to 8 and 10 to 13.	DA.OUTPUT_1:2 DA.OUTPUT_2:2
D/A output voltage L	VDAL	2, 3	IC Add: 0111 1100 Sub Add: 0000 0001 Data Add: 1100 1100	Measure the DC voltage of pins 5 to 8 and 10 to 13.	DA.OUTPUT_1:3 DA.OUTPUT_2:3

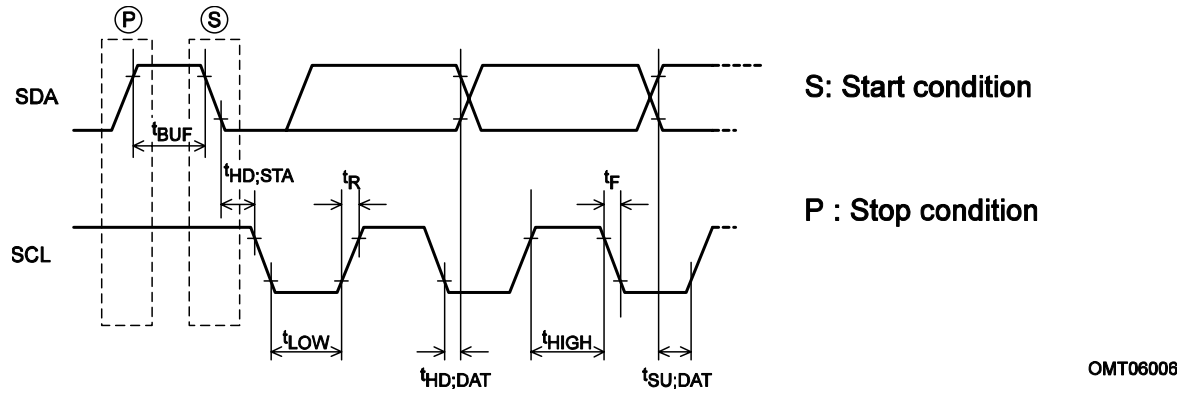
IIC input/output conditions at Ta = 25°C, V_{CC} = 5V

Parameter	Symbol	Standard		High speed		Unit
		min	max	min	max	
SCL Frequency	FSCL	0	100	0	400	kHz
BUS free time between stop - start	t_{BUF}	4.7		1.3		μs
HOLD time of start, restart condition	$t_{HD;STA}$	4.0		0.6		μs
L time of SCL	t_{LOW}	4.7		1.3		μs
H time of SCL	t_{high}	4.0		0.6		μs
Set-up time of restart condition	$t_{SU;STA}$	4.7		0.6		μs
HOLD time of SDA	$t_{HD;DAT}$	0		0	0.9	μs
Set-up time of SDA	$t_{SU;DAT}$	250		100		ns
Rising time of SDA, SCL	t_R		1000	20+0.1Cb	300	ns
Falling time of SDA, SCL	t_F		300	20+0.1Cb	300	ns

Refer to figure 1

(Note) Cb : Total capacitance of all BUS (Unit : pF)

IIC BUS INPUT Timing



IIC timing

Pin Assignment

PIN	FUNCTION	PIN	FUNCTION
1	V_{CC} 5V	16	SDA
2	DA Output 0	15	CLK
3	DA Output 1	14	ADDRESS
4	N.C.	13	I/O 0
5	I/O 7	12	I/O 1
6	I/O 6	11	I/O 2
7	I/O 5	10	I/O 3
8	I/O 4	9	GND

BUS Control Register Bit Allocation

IC Address (WRITE) : 011111A0

BUS Control Register Bit Allocation Map — 2002.12.27

Control Register Bit Allocations								
Sub Address	MSB			DATA BITS				LSB
	DA0 Bit7	DA1 Bit6	DA2 Bit5	DA3 Bit4	DA4 Bit3	DA5 Bit2	DA6 Bit1	DA7 Bit0
0000 0000	PEX7	PEX6	PEX5	PEX4	PEX3	PEX2	PEX1	PEX0
	0	0	0	0	0	0	0	0
0000 0001	DA Output 0		*		DA Output 0		*	
	0	0	*		0	0	*	

(Bits are transmitted in this order.)

BUS Control Register Bit Allocation Map

IC Address (READ) : 011111A1

Status Register Bit Allocations								
	MSB			DATA BITS				LSB
	DA0 Bit7	DA1 Bit6	DA2 Bit5	DA3 Bit4	DA4 Bit3	DA5 Bit2	DA6 Bit1	DA7 Bit0
Status 1	PEX7	PEX6	PEX5	PEX4	PEX3	PEX2	PEX1	PEX0
	*	*	*	*	*	*	*	*
Status 2	(PEX7)	(PEX6)	(PEX5)	(PEX4)	(PEX3)	(PEX2)	(PEX1)	(PEX0)
	*	*	*	*	*	*	*	*

Note

(1) "A" in the IC address is set by PIN14, Address.

(2) For the Read Status, the first 1 byte of two bytes that have been read is used.
(Attempt to read only the first 1 byte may cause failure of occurrence of the STOP condition.).

Bus Control Register Truth Table

Control Register Truth Table				
Register Name	0 HEX	1 HEX	2 HEX	3 HEX
PEX 0	Low	High		
PEX 1	Low	High		
PEX 2	Low	High		
PEX 3	Low	High		
PEX 4	Low	High		
PEX 5	Low	High		
PEX 6	Low	High		
PEX 7	Low	High		
DA OUTPUT_1	High	Mid 2	Mid 1	Low
DA OUTPUT_2	High	Mid 2	Mid 1	Low

Bus Control Register Truth Table

Status Byte Truth Table				
Register Name	0 HEX	1 HEX	2 HEX	3 HEX
PEX 0	Low	High		
PEX 1	Low	High		
PEX 2	Low	High		
PEX 3	Low	High		
PEX 4	Low	High		
PEX 5	Low	High		
PEX 6	Low	High		
PEX 7	Low	High		

BUS Initial Conditions

Initial Test Conditions	
Register	
PEX 0	0 HEX
PEX 1	0 HEX
PEX 2	0 HEX
PEX 3	0 HEX
PEX 4	0 HEX
PEX 5	0 HEX
PEX 6	0 HEX
PEX 7	0 HEX
DA OUTPUT_1	0 HEX
DA OUTPUT_2	0 HEX

BUS Control Register Descriptions

Control Register Descriptions		
Register Name	Bits	General Description
PEX 0	1	I/O PORT SW
PEX 1	1	I/O PORT SW
PEX 2	1	I/O PORT SW
PEX 3	1	I/O PORT SW
PEX 4	1	I/O PORT SW
PEX 5	1	I/O PORT SW
PEX 6	1	I/O PORT SW
PEX 7	1	I/O PORT SW
DA OUTPUT_1	2	D/A OUTPUT SW
DA OUTPUT_2	2	D/A OUTPUT SW

Test Circuit