380KHz, 18V/3A Synchronous Step-Down DC-DC Converter

General Description

The LA8509 is a current mode, synchronous step-down DC-DC converter that is designed to meet 3A output current, and utilizes PWM control scheme that switches with 380KHz fixed frequency.

The input voltage range of LA8509 is from 4.5V to 18V, and available in adjustable output voltage from 0.925V to 12V. The supply current is only 1.2mA during operation and under 1uA in shutdown.

This device provides an enable function that can be controlled by external logic signal. It also provides excellent regulation during line or load transient due to the current mode operation. Other features of current limit, soft-start, thermal shutdown protection, and short circuit protection are also included. Due to the low $R_{DS(ON)}$ of the internal power MOSFET, this device provides high efficiency step-down applications. It is available in SOP-8 package.

Features

- Continuous 3A Output Capability
- 0.925V Reference Voltage
- 4.5V to 18V Input Voltage Range
- Adjustable Output from 0.925V to 12V
- 380KHz Oscillation Frequency
- 1uA Low Shutdown Current
- 1.2mA Low Supply Current
- Current Mode for Excellent Response
- Support Low ESR Output Ceramic Capacitors
- Internal Current Limit
- Soft-Start
- Short Circuit Protection
- Thermal Shutdown Protection
- SOP-8 Package
- Meet RoHS Standard

Applications

- Broadband Communication Device
- LCD TV / Monitor
- Storage Device
- Wireless Application

Ordering Information

LA8509 1 2 3 4

1 (Package Type) => P: ESOP

2 (Number of Pins) => G: 8pin

3 (Output Voltage) => Blank: Adjustable

4 (Special Feature) => Blank: N/A

Available Part Number

LA8509PG

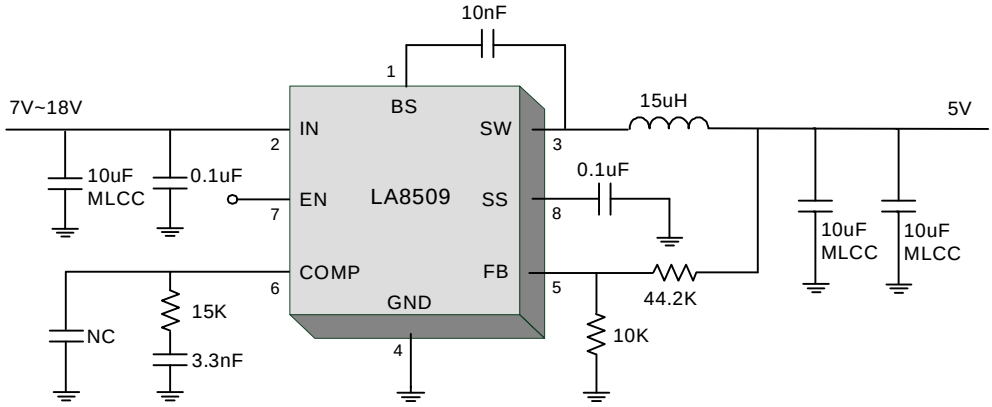
Marking Information

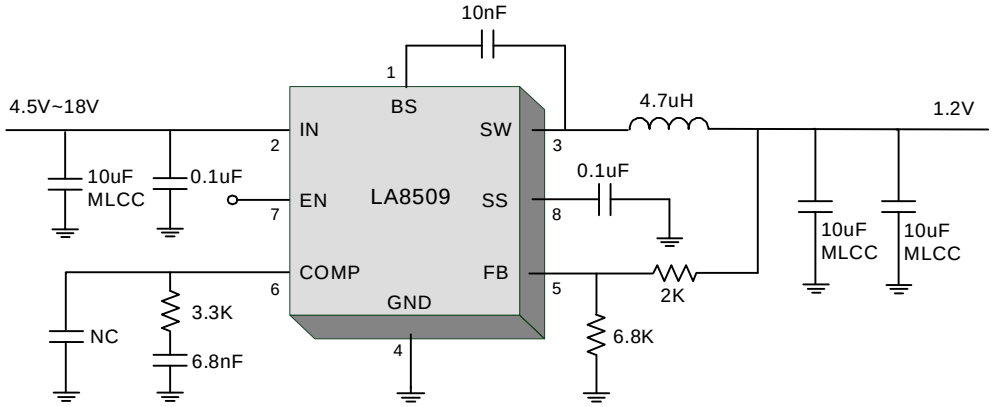
1 2 (Date Code)

For date code rule, please contact our sales representative directly

3 4 (Internal Code)

Typical Application





Quick Design Table

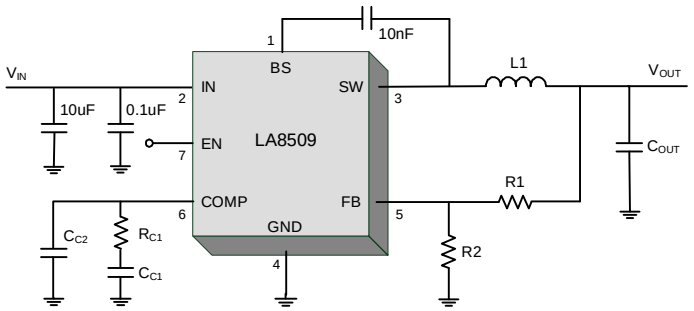
(1). Voltage Divider and Inductor Selection Table

(I_{OUT} = 3A, △I_L = 0.6A)

L1: Recommended Inductor

R1: Output Voltage Divider

R2: Output Voltage Divider



V_{OUT} / V_{IN}	1.2V	1.8V	2.5V	3.3V	5V	9V
5V	L1 : 4.7uH R1 : 2KOhm R2 : 6.8KOhm	L1 : 4.7uH R1 : 3KOhm R2 : 3.2KOhm	L1 : 6.8uH R1 : 5.1KOhm R2 : 3KOhm	L1 : 4.7uH R1 : 10KOhm R2 : 3.9KOhm		
9V	L1 : 4.7uH R1 : 2KOhm R2 : 6.8KOhm	L1 : 6.8uH R1 : 3KOhm R2 : 3.2KOhm	L1 : 6.8uH R1 : 5.1KOhm R2 : 3KOhm	L1 : 10uH R1 : 10KOhm R2 : 3.9KOhm	L1 : 10uH R1 : 44.2KOhm R2 : 10KOhm	
12V	L1 : 4.7uH R1 : 2KOhm R2 : 6.8KOhm	L1 : 6.8uH R1 : 3KOhm R2 : 3.2KOhm	L1 : 10uH R1 : 5.1KOhm R2 : 3KOhm	L1 : 10uH R1 : 10KOhm R2 : 3.9KOhm	L1 : 15uH R1 : 44.2KOhm R2 : 10KOhm	L1 : 15uH R1 : 59KOhm R2 : 6.8KOhm

(2). Output Capacitor and Compensation Component Selection Table

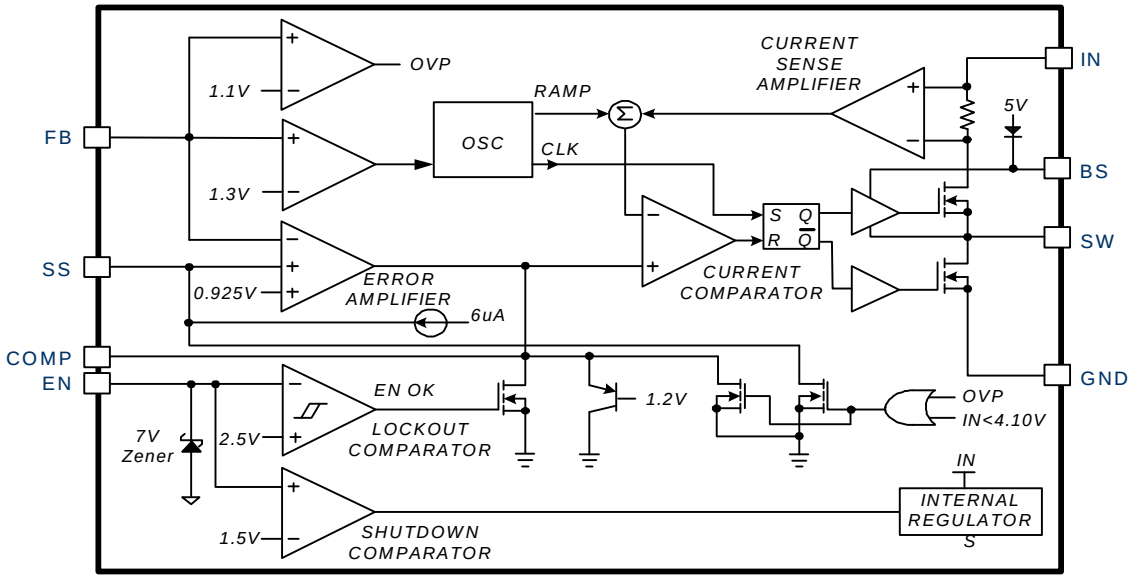
R_{C1}: Compensation Resistor

C_{C1}: 1′st Compensation Capacitor

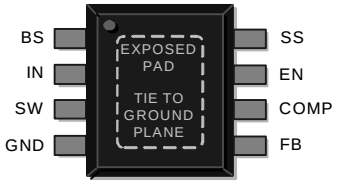
C_{C2}: 2′nd Compensation Capacitor

C_{OUT} / V_{OUT}	1.2V	1.8V	2.5V	3.3V	5V	9V
22uF ESR ≈ 5mΩ (MLCC)	R_{C1} : 1.8KOhm C_{C1} : 6.8nF C_{C2} : NC	R_{C1} : 2.5KOhm C_{C1} : 6.8nF C_{C2} : NC	R_{C1} : 3.3KOhm C_{C1} : 6.8nF C_{C2} : NC	R_{C1} : 4.7KOhm C_{C1} : 6.8nF C_{C2} : NC	R_{C1} : 6.8KOhm C_{C1} : 6.8nF C_{C2} : NC	R_{C1} : 12KOhm C_{C1} : 6.8nF C_{C2} : NC
47uF ESR ≈ 5mΩ (MLCC)	R_{C1} : 3.3KOhm C_{C1} : 6.8nF C_{C2} : NC	R_{C1} : 5.1KOhm C_{C1} : 4.7nF C_{C2} : NC	R_{C1} : 7.9KOhm C_{C1} : 3.3nF C_{C2} : NC	R_{C1} : 10KOhm C_{C1} : 3.3nF C_{C2} : NC	R_{C1} : 15KOhm C_{C1} : 3.3nF C_{C2} : NC	R_{C1} : 25KOhm C_{C1} : 3.3nF C_{C2} : NC
47uF ESR ≈ 15mΩ (SMD Polymer)	R_{C1} : 3.3KOhm C_{C1} : 4.7nF C_{C2} : NC	R_{C1} : 5.1KOhm C_{C1} : 3.3nF C_{C2} : NC	R_{C1} : 6.8KOhm C_{C1} : 3.3nF C_{C2} : NC	R_{C1} : 10KOhm C_{C1} : 2.2nF C_{C2} : NC	R_{C1} : 15KOhm C_{C1} : 2.2nF C_{C2} : NC	R_{C1} : 27KOhm C_{C1} : 1nF C_{C2} : NC
330uF ESR ≈ 300mΩ (Std. AL. E-Cap)	R_{C1} : 22KOhm C_{C1} : 2.2nF C_{C2} : 3.9nF	R_{C1} : 33KOhm C_{C1} : 2.2nF C_{C2} : 2.2nF	R_{C1} : 51KOhm C_{C1} : 2.2nF C_{C2} : 1.8nF	R_{C1} : 68KOhm C_{C1} : 2.2nF C_{C2} : 1.2nF	R_{C1} : 100KOhm C_{C1} : 2.2nF C_{C2} : 820pF	R_{C1} : 180KOhm C_{C1} : 1nF C_{C2} : 390pF
330uF ESR ≈ 50mΩ (Low ESR E-Cap)	R_{C1} : 27KOhm C_{C1} : 2.2nF C_{C2} : 680pF	R_{C1} : 39KOhm C_{C1} : 2.2nF C_{C2} : 470pF	R_{C1} : 51KOhm C_{C1} : 1nF C_{C2} : 330pF	R_{C1} : 68KOhm C_{C1} : 1nF C_{C2} : 220pF	R_{C1} : 100KOhm C_{C1} : 470pF C_{C2} : 120pF	R_{C1} : 180KOhm C_{C1} : 470pF C_{C2} : 82pF

Functional Block Diagram



Pin Configurations



Pin No.	Name	Description
1	BS	**Bootstrap. This pin provides power for the high side switch. Connect 10nF or greater from BS to SW to power the switch.**
2	IN	**Power Input. The capacitance of 0.1uF+10uF or greater must be connected from this pin to ground to bypass noise on the input of the IC.**
3	SW	**Power Switch Output. This pin is the switching node that supplies power to the output. Connect an L-C filter from SW to the output load.**
4	GND	**Ground. Connect this pin to the circuit ground.**
5	FB	**Feedback. This pin senses the feedback to regulate the output voltage. Connect FB to a voltage divider to set the output voltage.**
6	COMP	**Compensation Node. Connect a series R-C network from COMP to GND to compensate the regulation control loop.**
7	EN	**Enable Input. Drive EN HIGH to turn on the regulator, drive EN LOW to turn it off. Pull up with 100KOhm resistor for automatic startup.**
8	SS	**Soft-Start Control Input. Connect a capacitor from SS to GND to set the Soft-Start period. Leave SS unconnected if this function is not used.**

Absolute Maximum Ratings

Parameter	Rating
Input Voltage	20V
SW Voltage Range	-1V ~ V_{IN}+0.3V
BS Voltage Range	V_{SW}−0.3V ~ V_{SW}+6V
FB / EN / COMP Voltage Range	-0.3V ~ 6V
Storage Temperature Range	-65°C ~ 150°C
Junction Temperature	150°C
Lead Soldering Temperature (10 sec)	260°C

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

Recommended Operating Conditions

Parameter	Rating
Input Voltage Range	4.5V ~ 18V
Ambient Temperature Range	-40°C ~ 85°C
Junction Temperature Range	-40°C ~ 125°C

These are conditions under which the device functions but the specifications might not be guaranteed. For guaranteed specifications and test conditions, please see the *Electrical Specifications*.

Package Information

Parameter	Package	Symbol	Rating
Thermal Resistance (Junction to Case)	ESOP-8	θ_{JC}	10 °C/W
Thermal Resistance (Junction to Ambient)		θ_{JA}	50 °C/W

Electrical Specifications

V_{IN}=12V, T_A=25°C, unless otherwise noted.

Parameter	Test Condition	Min.	Typ.	Max.	Units
FB Voltage	V_{IN}=4.5V~16V	0.900	0.925	0.950	V
FB Over-Voltage Threshold			1.1		V
Oscillation Frequency			380		KHz
Short Circuit Frequency	V_{FB}=0V		120		KHz
Maximum Duty Cycle	V_{FB}=0.8V			92	%
Minimum ON Time			220		ns
High Side MOSFET $R_{DS(ON)}$			120		mΩ
Low Side MOSFET $R_{DS(ON)}$			90		mΩ
Current Limit			4.5		A
Error Amp. Voltage Gain, A_{VEA}			480		V/V
Error Amp. Transconductance, G_{EA}	ΔI_{COMP} = ±10uA		800		uA/V
Current Sense Transconductance, G_{CS}			5.2		A/V
Supply Current	V_{FB}=1V		1.2	1.5	mA
Shutdown Current	V_{EN}=0V		1	3	uA
Under-Voltage Lockout, UVLO	V_{IN} Rising	3.8	4.1	4.4	V
UVLO Threshold Hysteresis			100		mV
EN Shutdown Threshold Voltage	V_{EN} Rising	1.1	1.4	2	V
EN Shutdown Hysteresis			100		mV
EN Lockout Threshold Voltage		2.2	2.5	2.7	V
EN Lockout Hysteresis			150		mV
SW Leakage Current	V_{EN}=0V, V_{SW}=0V		0.1	10	uA
Soft-start Current, Iss	I_{SS}=0V		6		uA
Soft-start Period	C_{SS}=0.1uF		15		ms
Over Temperature Shutdown	Hysteresis=25 °C		160		°C

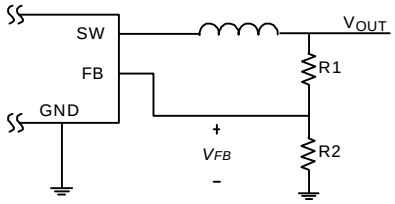
Application Information

Output Voltage Programming

LA8509 develops a band-gap between the feedback pin and ground pin. Therefore, the output voltage can be formed by R1 and R2. Use 1% metal film resistors for the lowest temperature coefficient and the best stability. Select lower resistor value to minimize noise pickup in the sensitive feedback pin, or higher resistor value to improve efficiency.

The output voltage is given by the following formula:

$$V_{OUT} = V_{FB} \times (1 + R1 / R2) \quad \text{where } V_{FB} = 0.925V$$



Under Voltage Lockout

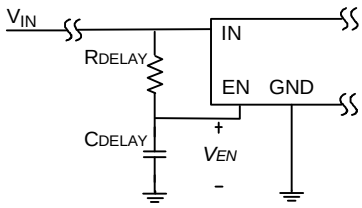
The under voltage lockout (UVLO) prevents this device from turning-on MOSFET at lower input voltage. It avoids wrong operation under undefined conditions. The threshold voltage of UVLO is approximately 4.1V.

Short Circuit Protection

When the output is shorted to ground, the protection circuit will be triggered and force the oscillation frequency down to approximately 120KHz. The oscillation frequency will return to 380KHz once the output voltage or the feedback voltage rises above 0V.

Delay Start-up

The following circuit uses the EN pin to provide a time delay between the input voltage is applied and the output voltage comes up. As the instant of the input voltage rises, the charging of capacitor C_{DELAY} pulls the EN pin low, keeping the device off. Once the capacitor voltage rises above the EN pin threshold voltage, the device will start to operate. The start-up delay time can be calculated by the following formula:

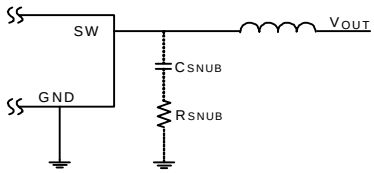


$$V_{IN} \times (1 - e^{-T/(RxC)}) > V_{EN}$$

Where T is the start-up delay time, R is R_{DELAY}, and C is C_{DELAY}.
This feature is useful in situations where the input power source is limited in the amount of current it can deliver. It allows the input voltage to rise to a higher voltage before the device starts operating.

Snubber Circuit

The simple RC snubber is used for voltage transient and ringing suppression. The high frequency ringing and voltage overshooting at the SW pin is caused by fast switching transition and resonating circuit parasitical elements in the power circuit. It maybe generates EMI and interferes with circuit performance. Reserve a snubber circuit in the PC board is preferred to damp the ringing due to the parasitical capacitors and inductors of layout. The following circuit is a simple RC snubber:



Choose the value of RC network by the following procedure:

(1) Measure the voltage ringing frequency (f_R) of the SW pin.

(2) Find a small capacitor and place it across the SW pin and the GND pin to damp the ringing frequency by half.

(3) The parasitical capacitance (C_{PAR}) at the SW pin is 1/3 the value of the added capacitance above. The parasitical inductance (L_{PAR}) at the SW pin is:

$$L_{PAR} = \frac{1}{(2\pi f_R)^2 \times C_{PAR}}$$

(4) Select the value of C_{SNUB} that should be more than 2~4 times the value of C_{PAR} but must be small enough so that the power dissipation of R_{SNUB} is kept to a minimum.
The power rating of R_{SNUB} can be calculated by following formula:

$$P\_RSNUB = C_{SNUB} \times V_{IN}^2 \times f_S$$

(5) Calculate the value of R_{SNUB} by the following formula and adjust the value to meet the expectative peak voltage.

$$R_{SNUB} = 2\pi \times f_R \times L_{PAR}$$

Thermal Considerations

Thermal protection limits total power dissipation in this device. When the junction temperature reaches approximately 160°C, the thermal sensor signals the shutdown logic turning off this device. The thermal sensor will turn this device on again after the IC's junction temperature cools by approximately 25°C. For continuous operation, do not exceed the maximum operation junction temperature 125°C.

The power dissipation across this device can be calculated by the following formula:

$$P_D = I_{LOAD}^2 \times [R_{ON\_T} \times \frac{V_{OUT}}{V_{IN}} + R_{ON\_B} \times (1 - \frac{V_{OUT}}{V_{IN}})] + \frac{1}{2} \times V_{IN} \times I_{LOAD} \times (t_r + t_f) \times f_S + V_{IN} \times I_S$$

where R_{ON_T} is the ON resistance of the high-side power MOSFET, R_{ON_B} is ON resistance of the low-side power MOSFET, fs is the 380KHz switching frequency, (tr+tf) is the switching time that is approximately 15ns, and I_S is the 1.2mA supply current.

The maximum power dissipation of this device depends on the thermal resistance of the IC package and PCB layout, the temperature difference between the die junction and ambient air, and the rate of airflow. The maximum power dissipation can be calculated by the following formula:

$$P_{D(MAX)} = \frac{(T_J - T_A)}{\theta_{JA}}$$

Where $T_J - T_A$ is the temperature difference between the die junction and surrounding environment, θ_{JA} is the thermal resistance from the junction to the surrounding environment.

The value of junction to case thermal resistance θ_{JC} is also popular to users. This thermal parameter is convenient for users to estimate the internal junction operated temperature of packages while IC operating. The operated junction temperature can be calculated by the following formula:

$$T_J = T_C + P_D \times \theta_{JC}$$

T_C is the package case temperature measured by thermal sensor. Therefore it's easy to estimate the junction temperature by any condition.

There are many factors affect the thermal resistance. Some of these factors include trace width, copper thickness, total PCB copper area, and etc. For the best thermal performance, wide copper traces and generous amounts of PCB copper should be used in the board layout. If further improve thermal characteristics are needed, double sided and multi-layer PCB with large copper areas and airflow will be recommended.

Layout Considerations

PC board layout is very important, especially for switching regulators of high frequencies and large peak currents. A good layout minimizes EMI on the feedback path and provides best efficiency. The following layout guides should be used to ensure proper operation of this device.

(1) The power charge path and discharge path which consist of the IN trace, the SW trace, the external inductor and the GND trace should be kept wide and as short as possible.

(2) The feedback path of voltage divider should be close to the FB pin and keep noisy traces away; also keep them separate using grounded copper.

(3) The input capacitors should be close to the regulator.

(4) The output capacitors should be close to the load.

Component Selection

Inductor Selection

The conduction mode of power stage depends on input voltage, output voltage, output current, and the value of the inductor. Select an inductor to maintain this device operating in continuous conduction mode (CCM). The minimum value of inductor can be determined by the following procedure.

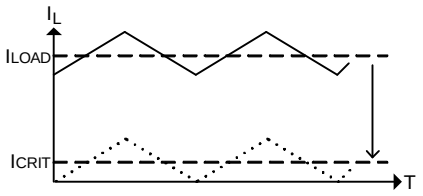
(1) Calculate the minimum duty ratio:

$$D_{(MIN)} = \frac{V_{OUT} + I_{LOAD} \times R_L + V_{DS\_B}}{V_{IN(MAX)} - V_{DS\_T} + V_{DS\_B}} = \frac{T_{ON}}{T_S}$$

Where R_L is the DC resistance of the external inductor, V_{DS_T} is the turn-on voltage of the High-Side MOSFET, V_{DS_B} is the turn-on voltage of the Low-Side MOSFET, and Ts is the switching period. This formula can be simplified to

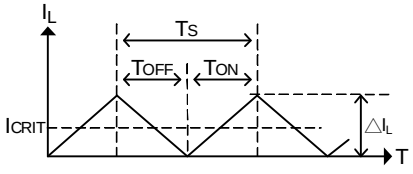
$$D_{(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)}} = \frac{T_{ON}}{T_S} \quad ; \quad 0 \le D \le 1$$

(2) Define a value of minimum current that is approximately 10%~30% of full load current to maintain continuous conduction mode, usually referred to as the critical current (I_{CRIT}).



$$I_{CRIT} = \delta \times I_{LOAD} \quad ; \quad \delta = 0.1 \sim 0.3$$

(3) Calculate the inductor ripple current ($\triangle I_L$). In steady state conditions, the inductor ripple current increase, ($\triangle I_L$+), during the ON time and the current decrease, ($\triangle I_L$-), during the OFF time must be equal.



$$\Delta I_L = 2 \times I_{CRIT}$$

(4) Calculate the minimum value of inductor use maximum input voltage. That is the worst case condition because it gives the maximum $\triangle I_L$.

$$L \ge \frac{[V_{IN(MAX)} - I_{LOAD} \times (R_{DS(ON)} + R_L) - V_{OUT}] \times D_{(MIN)}}{\Delta I_L \times fs}$$

This formula can be simplified to

$$L \ge \frac{(V_{IN(MAX)} - V_{OUT}) \times D_{(MIN)}}{\Delta I_L \times fs}$$

The higher inductance results in lower output ripple current and ripple voltage. But it requires larger physical size and price.

(5) Calculate the inductor peak current and choose a suitable inductor to prevent saturation.

$$I_{L(PEAK)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Coil inductors and surface mount inductors are all available. The surface mount inductors can reduce the board size but they are more expensive and its larger DC resistance results in more conduction loss. The power dissipation is due to the DC resistance can be calculated as below:

$$P_{D\_INDUCTOR} = I_{LOAD}^2 \times R_L$$

Output Capacitor Selection

The functions of the output capacitor are to store energy and maintain the output voltage. The low ESR (Equivalent Series Resistance) capacitors are preferred to reduce the output ripple voltage ($\triangle V_{OUT}$) and conduction loss. The output ripple voltage can be calculated as below:

$$\Delta V_{OUT} = \Delta I_L \times (ESR + \frac{1}{8 \times fs \times C_{OUT}})$$

Choose suitable capacitors must define the expectative value of output ripple voltage first.

The ESR of the aluminum electrolytic or the tantalum capacitor is an important parameter to determine the output ripple voltage. But the manufacturers usually do not specify ESR in the specifications. Assuming the capacitance is enough results in the output ripple voltage that due to the capacitance can be ignored, the ESR should be limited to achieve the expectative output ripple voltage. The maximum ESR can be calculated as below:

$$ESR \leq \frac{\Delta V_{OUT}}{\Delta I_L}$$

Choose the output capacitance by the average value of the RC product as below:

$$C_{OUT} \approx \frac{50 \sim 80 \times 10^{-6}}{ESR\_COUT}$$

If low ESR ceramic capacitor is used as output capacitor, the output ripple voltage due to the ESR can be ignored results in most of the output ripple voltage is due to the capacitance. Therefore, the minimum output capacitance can be calculated as below:

$$C_{OUT(MIN)} \geq \frac{\Delta I_L}{8 \times fs \times \Delta V_{OUT}}$$

The capacitors′ ESR and ripple current result in power dissipation that will increase the internal temperature. Usually, the capacitors′ manufacturers specify ripple current ratings and should not be exceeded to prevent excessive temperature shorten the life time. Choose a smaller inductor causes higher ripple current which maybe result in the capacitor overstress. The RMS ripple

current flowing through the output capacitor and power dissipation can be calculated as below:

$$I_{RMS} = \frac{\Delta I_L}{\sqrt{12}} = \Delta I_L \times 0.289$$

$$P_{D\_COUT} = I_{RMS}^2 \times ESR$$

The capacitor's ESL (Equivalent Series Inductance) maybe causes ringing in the low MHz region. Choose low ESL capacitors, limiting lead length of PCB and capacitor, and parallel connecting several smaller capacitors to replace with a larger one will reduce the ringing phenomenon.

Input Capacitor Selection

The input capacitor is required to supply current to the regulator and maintain the DC input voltage. Low ESR capacitors are preferred those provide the better performance and the less ripple voltage.

The input capacitors need an adequate RMS current rating. It can be calculated by following formula and should not be exceeded.

$$I_{RMS\_CIN} = I_{LOAD(MAX)} \times \sqrt{D \times (1 - D)}$$

This formula has a maximum at $V_{IN}=2V_{OUT}$. That is the worst case and the above formula can be simplified to:

$$I_{RMS\_CIN} = \frac{I_{LOAD(MAX)}}{2}$$

Therefore, choose a suitable capacitor at input whose ripple current rating must greater than half of the maximum load current.

The input ripple voltage ($\triangle V_{IN}$) mainly depends on the input capacitor's ESR and its capacitance. Assuming the input current of the regulator is constant, the required input capacitance for a given input ripple voltage can be calculated as below:

$$C_{IN} = \frac{I_{LOAD(MAX)} \times D \times (1 - D)}{fs \times (\Delta V_{IN} - I_{LOAD(MAX)} \times ESR)}$$

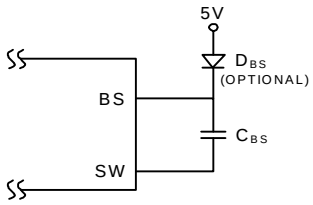
If using aluminum electrolytic or tantalum input capacitors, parallel connecting 0.1uF bypass capacitor as close to the regulator as possible. If using ceramic capacitor, make sure the capacitance is enough to prevent the excessive input ripple current.

The power dissipation of input capacitor causes a small conduction loss can be calculated as below:

$$P_{D\_CIN} = (I_{RMS\_CIN})^2 \times ESR$$

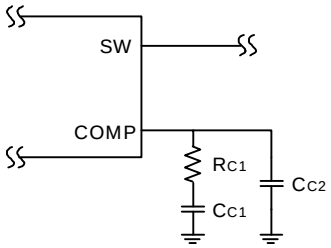
Bootstrap Capacitor and Optional Bootstrap Diode

The bootstrap capacitor (C_{BS}) provides the gate driver voltage for the high side switch. It will be charged while the high side switch is off. The recommended capacitance of C_{BS} is 10nF~1uF.
If the input voltage is lower than 5V or duty cycle is more than 65%, add an external bootstrap diode (D_{BS}) between an external 5V and BS is recommended for efficiency improvement. The D_{BS} can be a low cost one such as 1N4148 or BAT54, and the external 5V can be a 5V fixed voltage from system or 5V output of LA8509.



Loop Compensation Design

The current mode control scheme provides the faster transient response and easy to compensate because of eliminates the double pole of the output L-C filter. The system stability and transient response are controlled by compensation pin (COMP) that is the output of the transconductance error amplifier. The R-C network between COMP and GND sets pole-zero compensation to shape the close loop transfer function to get desired gain and phase.
The goal of the compensation design is to have a higher DC gain, enough phase margin, and higher bandwidth. The following figure shows the related components of the compensation loop.



With current mode, the buck power stage can be simplified to be a 1 pole and 1 zero. The compensation network provides 2 poles and 1 zero. They are determined by the following formulas:
The DC loop gain is:

$$A_{VDC} = G_{CS} \times A_{VEA} \times \frac{V_{FB}}{I_{LOAD}}$$

The pole (f_{P1}) of the buck power stage due to the output capacitor, the load current, and the output voltage is:

$$f_{P1} = \frac{I_{LOAD}}{2\Pi \times C_{OUT} \times V_{OUT}}$$

The zero (f_{Z1}) of the buck power stage due to the output capacitor and its ESR is:

$$f_{Z1} = \frac{1}{2\Pi \times C_{OUT} \times ESR}$$

The pole (f_{P2}) due to the compensation capacitor (C_{C1}) and the output resistance of the error amplifier is:

$$f_{P2} = \frac{1}{2\Pi \times C_{C1} \times (R_{C1} + \frac{A_{VEA}}{G_{EA}})} \approx \frac{G_{EA}}{2\Pi \times C_{C1} \times A_{VEA}}$$

The zero (f_{Z2}) due to the compensation capacitor (C_{C1}) and the compensation resistor (R_{C1}) is:

$$f_{Z2} = \frac{1}{2\Pi \times C_{C1} \times R_{C1}}$$

The pole (f_{P3}) due to the second compensation capacitor (C_{C2}) and the compensation resistor (R_{C1}) is:

$$f_{P3} = \frac{1}{2\Pi \times C_{C2} \times R_{C1}}$$

The system crossover frequency (f_C) is defined to be the frequency where the feedback loop has unity gain. It is also called the bandwidth of the converter. Lower bandwidth causes poor transient response while higher bandwidth could cause system unstable.

In general, set the crossover frequency to be less than 1/10 of the switching frequency is recommended.

The loop compensation design guides are as below:

(1) Choose the compensation resistor (R_{C1}) to set the crossover frequency that should be less than 1/10 of the switching frequency. The R_{C1} can be calculated by the following formula:

$$R_{C1} = f_C \times \frac{V_{OUT}}{V_{FB}} \times \frac{2\Pi \times C_{OUT}}{G_{EA} \times G_{CS}}$$

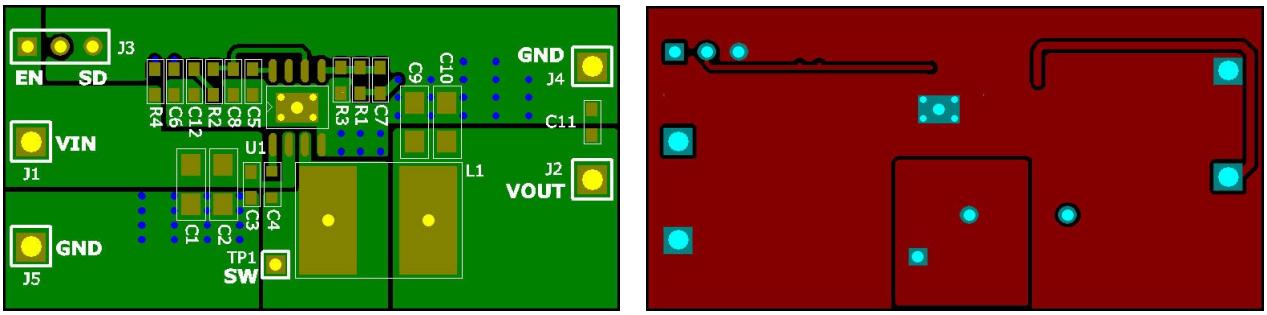
(2) Choose the compensation capacitor (C_{C1}) to achieve the desired phase margin. For applications with typical inductor values, setting the compensation zero (f_{Z2}) to be less than 1/4 of the crossover frequency provides sufficient phase margin. The C_{C1} can be calculated by the following formula:

$$C_{C1} = \frac{2}{\Pi \times R_{C1} \times f_C}$$

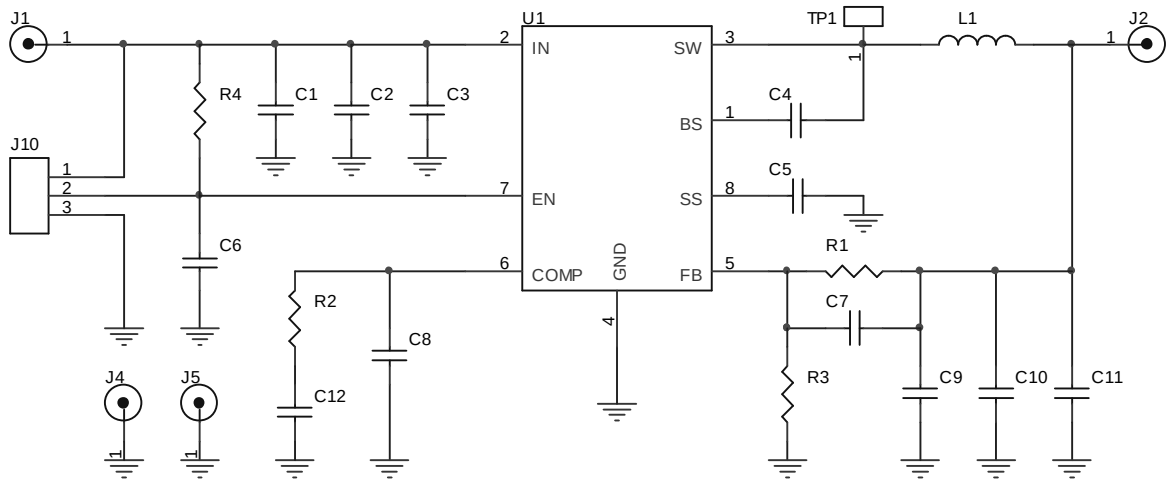
(3) The second compensation capacitor (C_{C2}) is required if the ESR zero (f_{Z1}) of the output capacitor is located at less than 1/2 of the switching frequency. If required, add the C_{C2} to set the compensation pole (f_{P3}) at location of the ESR zero (f_{Z1}). The C_{C2} can be calculated by the following formula:

$$C_{C2} = \frac{C_{OUT} \times ESR}{R_{C1}}$$

Evaluation Board Layout



Evaluation Board Schematic

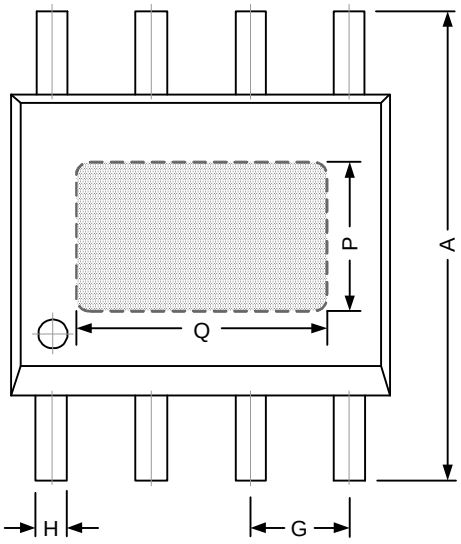


Key Components Supplier

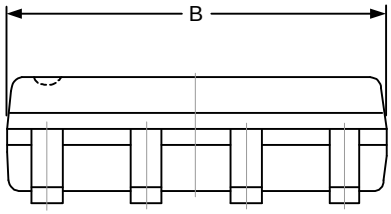
Item	Manufacturer	Website
Inductor (L)	**Chilisin**	www.chilisin.com.tw
	WE	www.we-online.com
Electrolytic Capacitor (C)	**Nippon Chemi-Con**	www.chemi-con.co.jp
	Jamicon	www.jamicon.com.tw
SMD Capacitor (C)	**Yageo**	www.yageo.com
	Taiyo Yuden	www.yuden.co.jp
SMD Resistor (R)	**Yageo**	www.yageo.com

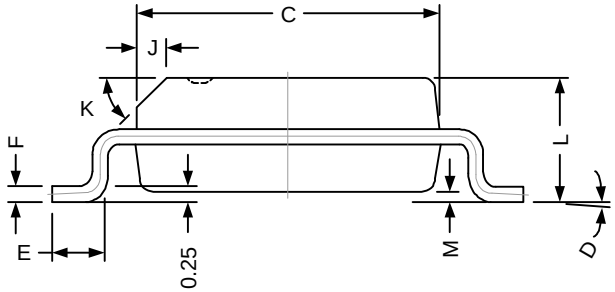
Package Outline

ESOP-8



REF.	DIMENSIONS Millimeter	
	Min.	Max.
A	5.80	6.20
B	4.80	5.00
C	3.80	4.00
D	0°	8°
E	0.40	0.90
F	0.19	0.25
M	0.10	0.25
H	0.35	0.49
L	1.35	1.75
P	2.30	2.50
Q	3.20	3.40
J	0.375 REF.	
K	45°	
G	1.27 TYP.	





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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.