Ordering number : EN7413

SANYO Semiconductors
DATA SHEET

Monolithic Linear IC

LA9703W — Front End Processor for DVD Player

Overview

The LA9703W is an RF signal-processing and servo error signal generation IC for DVD and CD playback.
A DVD player can be implemented by combining this IC with a DVD DSP product that includes a digital servo DSP.

Functions

- Generation of RF signal (with built-in RFAGC circuit).
- Generation of RF - peak detection.
- Generation of RF - bottom detection (time constant changeover).
- RF equalizer incorporated (f_O, boost variable).
- FE Amplifier (Balance Adjustment VCA Built in).
- 3-beam Tracking Error Amplifier (Balance Adjustment VCA Built in).
- Reflect Amplifier.
- DPD Circuit.
- Push-pull TE amplifier.
- Wobble detection BPF built in.
- APC Circuit (two channels).

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		6.0	V
Allowable power dissipation	Pd max	Ta≤70°C(Mounted on a board *)	500	mW
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-40 to +150	°C

* Size: 114.3×76.1×1.6 mm Material: Glass epoxy

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		5.0	V
Operating supply voltage	V_{CC} op		4.65 to 5.35	V

SANYO Semiconductor Co., Ltd.
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Electrical Characteristics at Ta = 25°C, V_{CC} (Pins 2, 29, 63) = 5.0V, GND = (Pins 8, 19, 56) = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I_{CC}	No signal	31	40.5	53	mA
Reference voltage 1	PREF	Pin 58, Load current ±2mA	2.3	2.5	2.7	V
Reference voltage 2	SREF	Pin 48 = 5V, Pin 51, Load current ±2mA	2.3	2.5	2.7	V
V_{IH} min	V_{IH}	Pin 20 to 28, Pin 30 to 31	2.3			V
V_{IL} max	V_{IL}	Pin 20 to 28, Pin 30 to 31			0.98	V
I_{IH}	I_{IH}	Pin 20 to 28, Pin 30 to 31	-10		+10	µA
I_{IL}	I_{IL}	Pin 20 to 28, Pin 30 to 31	-10		+10	µA
V_{IDAH} max	V_{IDH}	Pin 32 to 36			SREF+1	V
V_{IDAL} min	V_{IDL}	Pin 32 to 36	SREF-1			V
Customer OP1	CAOP1	Pin 1 = PREF+450mV, Pin 62	PREF+0.3	PREF+0.45	PREF+0.6	V
Customizer OP2	CAOP2	Pin 1 = PREF-300mV, Pin 62	PREF-0.45	PREF-0.3	PREF-0.25	V
RF-EQ	RFEQ	Pins 61, 59 13MHz input, Pin 23 = 5V, Pin 25 = 0V, Pin 26 = 5V, Pin 34 = SREF+1V Output gain ratio of pins 55 and 54 at input of SREF+1V to pin 33 and SREF-1V to pin 33	6	9	12	dB
RF GAIN 1 (MAX GAIN 1)	RFG1	Pins 61, 59 input, Pin 23 = 0V, Pin 25 = 5V Pin 33 = Pin 34 = SREF Pins 55, 54	30	37		dB
RF GAIN 2 (MIN GAIN)	RFG2	Pins 61, 59 input, Pin 23 = 0V, Pin 25 = 0V Pin 33 = Pin 34 = SREF Pins 55, 54		3.4	6	dB
RF GAIN 3 (AGOF GAIN)	RFG3	Pins 61, 59 input, Pin 23 = 0V, Pin 25 = 0V Pin 33 = Pin 34 = SREF Pins 55, 54	3.9	7.9	11.9	dB
RF GAIN 4 (MAX GAIN 2)	RFG4	Pins 61, 59 input, Pin 23 = 0V, Pin 25 = 0V Pin 33 = Pin 34 = SREF Pins 55, 54	17.4	24.4		dB
PH	PH	Pin 61 = 130mVp-p, Pin 59 = PREF, Pin 23 = 0V, Pin 25 = 0V, Pin 33 = Pin 34 = SREF, Pin 24 = 0V Pin 50	SREF+0.5	SREF+0.75	SREF+0.9	V
BH	BH	Pin 61 = 130mVp-p, Pin 59 = PREF, Pin 23 = 0V, Pin 25 = 0V, Pin 33 = Pin 34 = SREF, Pin 31 = 5V Pin 46	SREF-0.23	SREF-0.53	SREF-0.83	V
RREC1	RREC1	Pins A6, A7 input, Pin 25 = 0V, Pin 32 = SREF-0.75V Pin 38	-5.7	-2.7	1.7	dB
RREC2	RREC2	Pins A6, A7 input, Pin 25 = 0V, Pin 32 = SREF+0.75V Pin 38	12.5	17.5	22.5	dB
RREC3	RREC3	Pins A6, A7 input, Pin 25 = 5V, Pin 32 = SREF-0.75V Pin 38	7.2	11.2	15.2	dB
RRECOST	ROST	A6 = A7 = PREF, Pin 25 = 0V, Pin 32 = SREF Pin 38	SREF-0.3	SREF	SREF+0.3	V
FEGAIN1	FEG1	Pins A6, A7 input, Pin 25 = 0V, Pin 32 = SREF-0.75V Pin 35 = SREF, Pin 39	2.2	5.2	8.2	dB
FEGAIN2	FEG2	Pins A6, A7 input, Pin 25 = 0V, Pin 32 = SREF+0.75V Pin 35 = SREF, Pin 39	22.5	25.5	28.5	dB
FEGAIN3	FEG3	Pins A6, A7 input, Pin 25 = 5V, Pin 32 = SREF-0.75V Pin 35 = SREF, Pin 39	15.9	19.9	23.9	dB
FEOST	FOST	A6 = A7 = PREF, Pin 25 = 0V, Pin 32 = SREF Pin 35 = SREF, Pin 39	SREF-0.3	SREF	SREF+0.3	V
FEBAL1	FBAL1	Pins A6, A7 input, Pin 25 = 0V, Pin 32 = SREF Pin 35 = SREF-0.75V, Pin 39ΔGAIN	5.2	8.2	11.2	dB
FEBAL2	FBAL2	Pins A6, A7 input, Pin 25 = 0V, Pin 32 = SREF Pin 35 = SREF+0.75V, Pin 39ΔGAIN	-11.2	-8.2	-5.2	dB
TEGAIN1	TEG1	A10, A11 pin input, Pin 25 = 0V, Pin 32 = SREF-0.75V, Pin 36 = SREF, Pin 40	12.2	15.2	18.2	dB
TEGAIN2	TEG2	A10, A11 pin input, Pin 25 = 0V, Pin 32 = SREF+0.75V, Pin 36 = SREF, Pin 40	32.6	35.6	38.5	dB
TEGAIN3	TEG3	A10, A11 pin input, Pin 25 = 5V, Pin 32 = SREF-0.75V, Pin 36 = SREF, Pin 40	25.8	29.8	33.8	dB
TEOST	TOST	A10 = Pin 11 = PREF, Pin 25 = 0V, Pin 32 = SREF Pin 36 = SREF, Pin 40	SREF-0.3	SREF	SREF+0.3	V

Continued on next page.

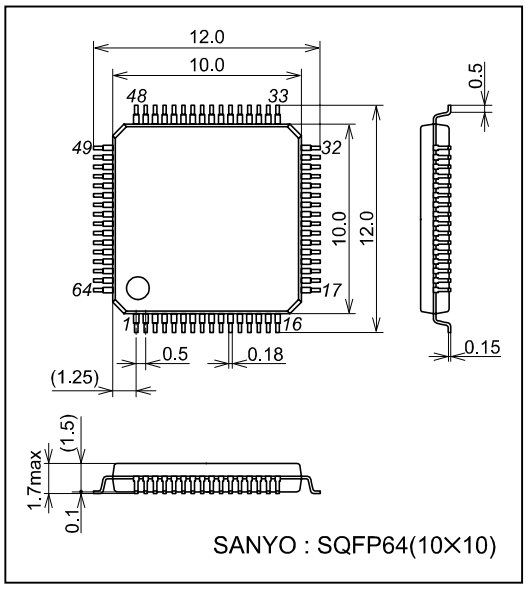
Continued from preceding page.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
TEBAL1	TBAL1	A10, A11 pin input, Pin 25 = 0V, Pin 32 = SREF Pin 36 = SREF-0.75V, Pin 40ΔGAIN	5.3	8.3	11.3	dB
TEBAL2	TBAL2	A10, A11 pin input, Pin 25 = 0V, Pin 32 = SREF Pin 36 = SREF+0.75V, Pin 40ΔGAIN	-11.3	-8.3	-5.3	dB
DPD phase difference voltage difference 1	P_D1	Differential voltage at pin 39 between inputs of Pin A1=pin A3=pin A4=pin A5=5MHz phase 0 degree, pin A2=5MHz phase 36 degrees and inputs of pin A1=pin A3=pin A4=pin A5=5MHz phase 0 degree, pin A2=5MHz phase -36 degree, R_L=6.8kΩ	0.39	0.51	0.66	V
DPD phase difference voltage difference 2	P_D2	Differential voltage at pin 39 between inputs of Pin A1 = pin A2 = pin A4 = pin A5 = 5MHz phase 0 degree, pin A3 = 5MHz phase 36 degrees and inputs of pin A1 = pin A2 = pin A4 = pin A5 = 5MHz phase 0 degree, pin A3 = 5MHz phase -36 degree, R_L = 6.8kΩ	-0.66	-0.51	-0.39	V
DPD phase difference voltage difference 3	P_D3	Differential voltage at pin 39 between inputs of Pin A1 = pin A2 = pin A3 = pin A5 = 5MHz phase 0 degree, pin A4 = 5MHz phase 36 degrees and inputs of pin A1 = pin A2 = pin A3 = pin A5 = 5MHz phase 0 degree, pin A4 = 5MHz phase -36 degree, R_L = 6.8kΩ	0.39	0.51	0.66	V
DPD phase difference voltage difference 4	P_D4	Differential voltage at pin 39 between inputs of Pin A1 = pin A2 = pin A3 = pin A4 = 5MHz phase 0 degree, pin A5 = 5MHz phase 36 degrees and inputs of pin A1 = pin A2 = pin A3 = pin A4 = 5MHz phase 0 degree, pin A5 = 5MHz phase -36 degree, R_L = 6.8kΩ	-0.66	-0.51	-0.39	V
DPD offset	DPDOF	Pin A1 = A2 = A3 = A4 = A5 = 5MHz R_L = 6.8kΩ	SREF-0.3	SREF	SREF+0.3	V
APC1 reference voltage	LDS1	Pin 20 = 0V, Pin 21 = 5V, Pin 15	150	180	200	mV
APC1 off	LDD1	Pin 21 = 0V, Pin 15	4.5	5		V
APC2 reference voltage	LDS2	Pin 20 = 5V, Pin 21 = 5V, Pin 15	3.2	3.5	3.8	mV
APC3 reference voltage	LDS3	Pin 22 = 5V, Pin 17	150	180	200	mV
APC2 off	LDD2	Pin 22 = 0V, Pin 17	4.5	5		V
BPF1	BPF1	Pin A8 = Pin A9 = 190kHz, Pin 32 = SREF-0.75V Pin 41	13.5	19	24.5	dB
BPF2	BPF2	Pin A8 = Pin A9 = 140kHz, Pin 32 = SREF-0.75V Pin 41		13.5	19.5	dB
BPF3	BPF3	Pin A8 = Pin A9 = 240kHz, Pin 32 = SREF-0.75V Pin 41		11	17	dB

Package Dimensions

unit : mm

3190A



Operational Descriptions

(1) Customer amplifier

This IC includes a built-in high-band operational amplifier. Pin 1 is the noninverting input and pin 64 is the inverting input. Pin 62 is the output.

If this circuit is not used, short pins 62 and 64, and connect pin 1 to pin 58.

(2) RF amplifier

The RF signal input differentially to pins 59 and 61 is passed through a VCA used for AGC and an equalizer and output as a differential signal from pins 54 and 55. The peak level and DC level of the differential signal output from pins 54 and 55 are detected. The AGC VCA is controlled by the detected peak signal to form an AGC loop. The time constant used for peak detection can be set with the value of the capacitor connected to pin 50. The AGC circuit can be set to a fixed gain by setting pin 23 to the high level. Also note that a DC servo is formed by adding the detected DC value to the AGC VCA front end. The DC servo band can be set with the value of the capacitor connected to pin 52.

Setting pin 25 to the high level increases the gain of the input stage amplifier for pins 59 and 61 by a factor of five.

(3) RF equalizer

The equalizer is switched by pin 26 between DVD mode (when pin 26 is high) and CD mode (when pin 26 is low). The equalizer band is set by the value of the resistor connected between pin 57 and ground. The equalizer f_O frequency can be changed by changing the pin 34 DC voltage.

The amount of boost provided by the equalizer can be changed by changing the pin 33 DC voltage.

(4) Peak hold/bottom hold

The peak hold and bottom hold envelope waveforms for the differential signal output from pins 54 and 55 is output from pins 47 and 46. When pin 24 is at the high level, the peak envelope detection time constant can be set with the value of the resistor connected between pin 49 and ground. The bottom hold band can be roughly doubled by setting pin 31 to the low level.

(5) Reflection amplifier

The current signal input to pins 9 and 10 is converted to a voltage and summed using a summation amplifier. The pit component is removed from the input signal with a low-pass filter. The summed signal is passed through the VCA that adjusts the servo gain and is output from pin 38. The VCA that adjusts the servo gain is controlled by the DC voltage applied to pin 32.

The gain is increased by another factor of 5 when pin 25 is at the high level.

(6) FE amplifier

The current signal input to pins 9 and 10 is converted to a voltage and after passing through a balance adjustment VCA, the difference is taken. That signal is then passed through a servo gain adjustment VCA and output from pin 39. The gain of the balance adjustment VCA can be adjusted by changing the DC voltage applied to pin 32.

The gain is increased by another factor of 5 when pin 25 is at the high level.

(7) TE amplifier (for 3-beam systems)

The current signal input to pins 13 and 14 is converted to a voltage and after passing through a balance adjustment VCA, the difference is taken. That signal is then passed through a servo gain adjustment VCA and, after band switching, output from pin 40. The gain of the balance adjustment VCA can be adjusted by changing the DC voltage applied to pin 36. This VCA, which adjusts the servo gain, is controlled by the DC voltage applied to pin 32. The band switching circuit consists of a low-pass filter whose frequency is 30kHz when pin 31 is at the high level and whose frequency is 200kHz when pin 31 is low. Also, when pin 30 is at the low level, the output is shunted to SREF.

The gain is increased by another factor of 5 when pin 25 is at the high level.

(8) DPD circuit

This circuit compares the phase of the pin 3 input signal to the pin 4, 5, 6, and 7 input signals and outputs the result from pin 40. The phase compared signal is output as a current signal by the pin 37 constant-current charge pump, and converted to a voltage level by the external capacitor and resistor attached to pin 37. The signal converted to a voltage is passed through a buffer amplifier and, after band limiting is applied by the band switching circuit, is output from pin 40. The charge pump is set to its off mode by a high level on pin 30. The band switching circuit consists of a low-pass filter whose frequency is 30kHz when pin 31 is at the high level and whose frequency is 200kHz when pin 31 is low. Also, when pin 30 is at the low level, pin 37 is shunted to SREF.

(9) PP amplifier

The current signal input to pins 11 and 12 is converted to a voltage and after passing through a servo gain adjustment VCA, the signal is band limited and output from pin 42. The signal output from pin 42 is input to pin 43 through a capacitor and resistor. After this input signal is amplified, it is output from pin 41. This VCA, which adjusts the servo gain, is controlled by the DC voltage applied to pin 32.

Note that pin 28 must be set to the low level if the PP amplifier is used.

(10) Wobble bandpass filter

The current signal input to pins 11 and 12 is converted to a voltage and the difference is taken. After passing through the servo gain adjustment VCA, the signal is input to the bandpass filter. The DC component of the signal that was band limited by the bandpass filter is removed with a DC cut circuit and, after being amplified by a 37dB amplifier, it is output from pin 41. The f_O frequency of the bandpass filter can be changed by changing the value of the external resistor connected between pin 45 and ground.

When the value of the pin 45 external resistor is 62kΩ, f_O will be about 200kHz. The cutoff frequency for the DC cut circuit is set by the value of the capacitor connected to pin 44. The cutoff frequency will be approximately the product of the internal resistance (18kΩ) and the value of the external capacitor.

Note that pin 28 must be set to the low level if the PP amplifier is used.

(11) APC circuit

A servo loop that holds the laser power at a fixed level is formed by inputting the monitor signal to pin 16 and connecting pin 15 to the laser driver. The threshold voltage will be 180mV when pin 20 is low and (V_{CC} - 1.5V) when pin 20 is high. The laser can be turned off by setting pin 21 to the low level.

Note that there are two APC circuit systems; the second system consists of pins 18 (monitor input), 17 (laser drive), and 22 (laser on/off). The threshold voltage is 180mV.

(12) Reference circuit

The V_{CC} level is resistor divided by two internally and that voltage is output from pin 58. The pin 58 voltage is a dedicated reference voltage for the pickup.

The pin 48 voltage level is resistor divided by two internally and that voltage is output from pin 51. The pin 51 voltage is a reference level that is supplied to the DSP and other circuits.

Pin Description

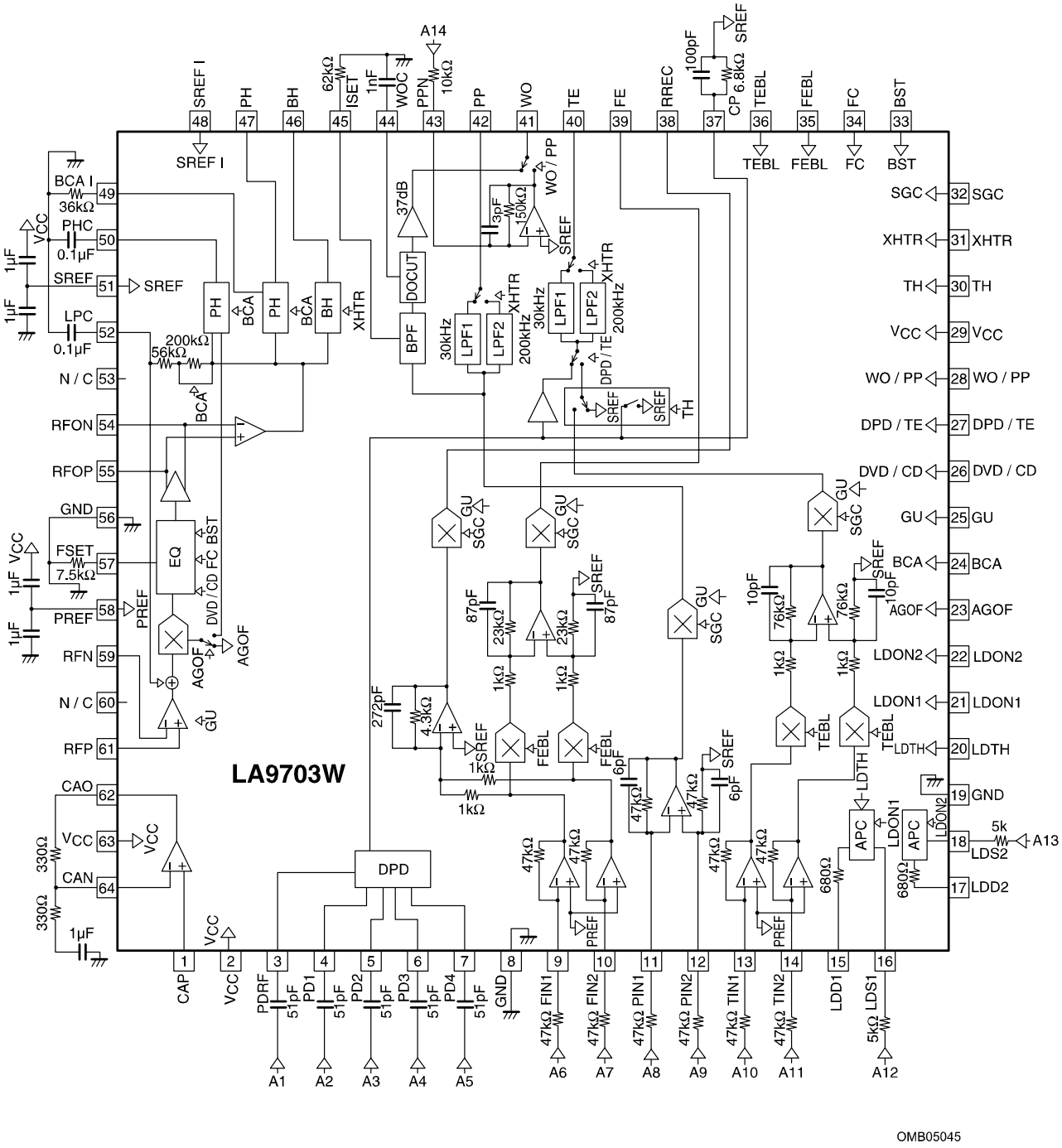
Pin No.	Pin name	Pin description
1	CAP	Customer OP amplifier + input
2	V_{CC}	Power pin (for DPD)
3	PDRF	Pickup signal input
4	PD1	Pickup signal input
5	PD2	Pickup signal input
6	PD3	Pickup signal input
7	PD4	Pickup signal input
8	GND	Ground (for DPD)
9	FIN1	Pickup signal input
10	FIN2	Pickup signal input
11	PIN1	Pickup signal input
12	PIN2	Pickup signal input
13	TIN1	Pickup signal input
14	TIN2	Pickup signal input
15	LDD1	AP1 output
16	LDS1	APC1 monitor input
17	LDD2	APC2 output
18	LDS2	PC2 monitor input
19	GND	Ground (servo system)
20	LDTH	APC1 threshold changeover (H:V_{CC}-1.5V, L: 180mV)
21	LDON1	APC1 laser ON pin (H: ON)
22	LDON2	APC2 laser ON pin (H: ON)
23	AGOF	RFAGC OFF pin (H: OFF)
24	BCA	PH discharge factor changeover (H: BCA mode)
25	GU	RF, servo signal gain-up pin (H: gain-up)
26	DVD/CD	RF-equalizer band changeover pin (H: DVD)
27	DPD/TE	TE output changeover pin (H: DPD)
28	WO/PP	WO output changeover pin (H: wobble)
29	V_{CC}	Power pin (servo system)
30	TH	Tracking hold (H: hold)
31	XHTR	Tracking, bottom band changeover (L: high band)
32	SGC	Servo gain control pin (RREC, FE, PP, TE)
33	BST	Equalizer boost control pin
34	FC	Equalizer fo control pin
35	FEBL	FE balance control pin
36	TEBL	TE balance control pin
37	CP	Pin to connect resistor and capacitor to set charge pump gain
38	RREC	Reflection output
39	FE	Focus error output
40	TE	Tracking error output
41	WO	Wobble/push-pull output pin
42	PP	Push-pull output pin
43	PPN	Pin to connect resistor to set push-pull gain
44	WOC	DC cut capacity connection pin
45	ISET	Pin to connect resistor to set BPF central frequency
46	BH	RF bottom detection output
47	PH	RF peak detection output
48	SREFI	SREF setting pin
49	BCAI	Pin to connect resistor to set the peak hold detection constant
50	PHC	Pin to connect PH detection capacitor for RF-AGC

Continued on next page.

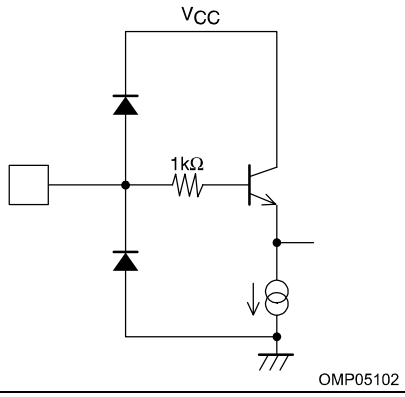
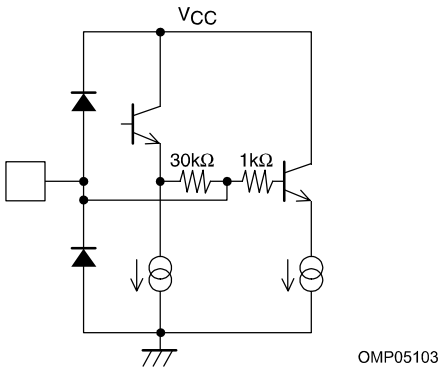
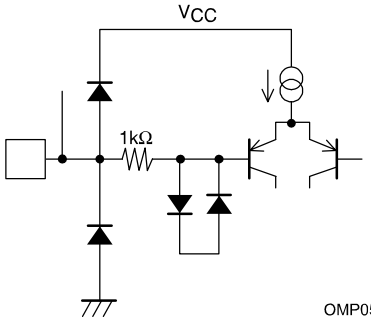
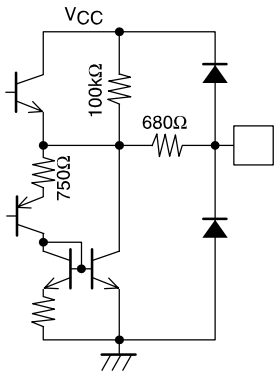
Continued from preceding page.

Pin No.	Pin name	Pin description
51	SREF	Reference voltage output for servo signal
52	LPC	Pin to connect capacitor for RF DC servo
53	N/C	N/C pin
54	RFON	RF - output
55	RFOP	RF + output
56	GND	Ground (RF system)
57	FSET	Pin to connect resistor to set equalizer for frequency
58	RREF	Reference voltage output (for pick)
59	RFN	RF signal - input
60	N/C	N/C pin
61	RFP	RF + signal
62	CAO	Customer OP amplifier output pin
63	V_{CC}	Power pin (RF system)
64	CAN	Customer OP amplifier - input pin

Block Diagram and Test Circuit

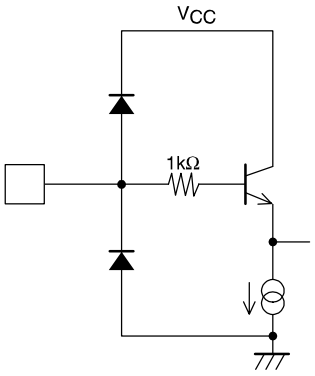
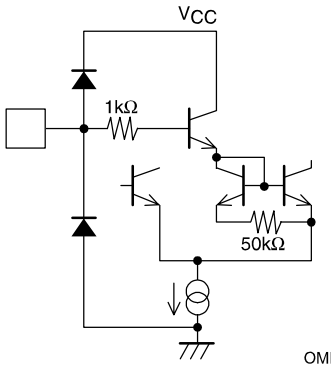
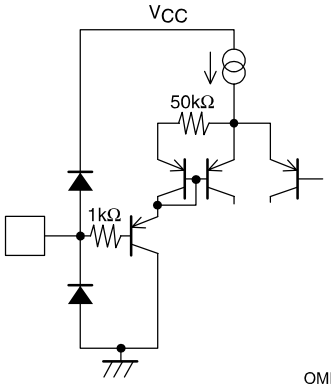
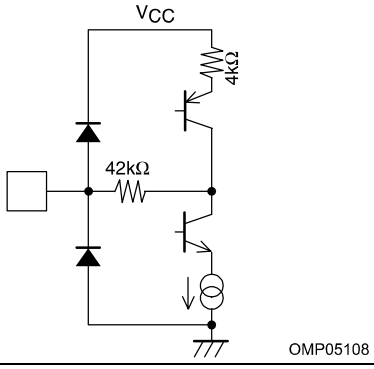


The Explanation of the Terminal

Pin No.	Pin name	Equivalent circuit
1 64	CAP CAN	
3 4 5 6 7	PDRF PD1 PD2 PD3 PD4	
9 10 11 12 13 14	FIN1 FIN2 PIN1 PIN2 TIN1 TIN2	
15 17	LDD1 LDD2	

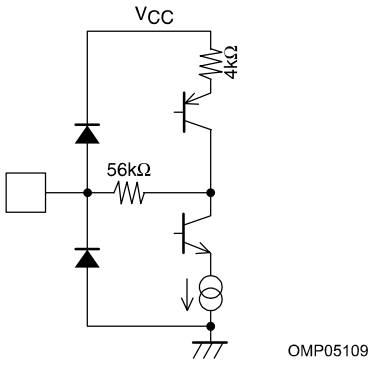
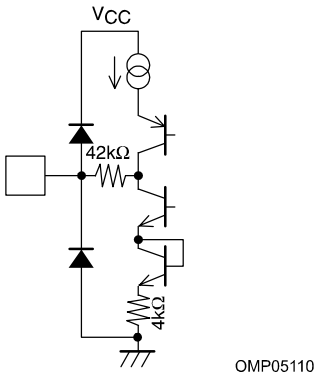
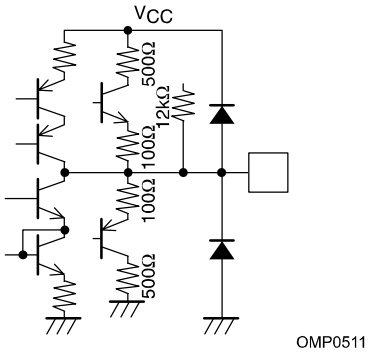
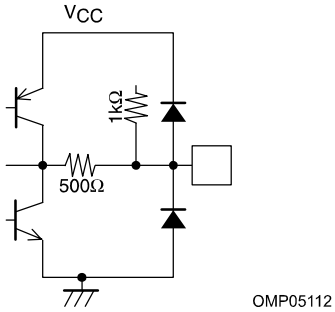
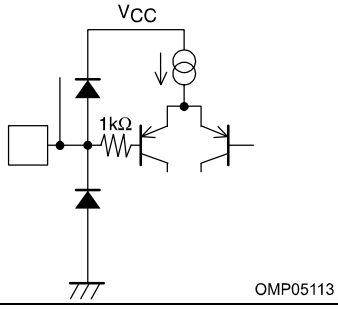
Continued on next page.

Continued from preceding page.

Pin No.	Pin name	Equivalent circuit
16 18	LDS1 LDS2	
20 21 22 24 25 27 28 30 31	LDTH LDON1 LDON2 BCA GU DPD/TE WO/PP TH XHTR	
23 26	AGOF DVD/CD	
32 33	SGC BST	

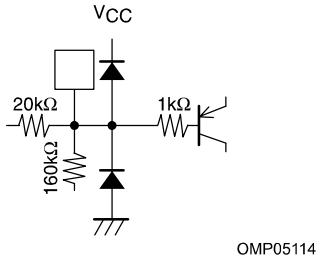
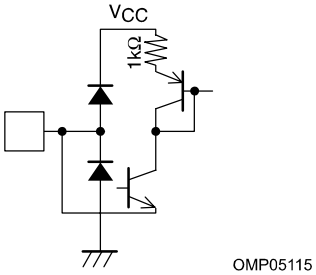
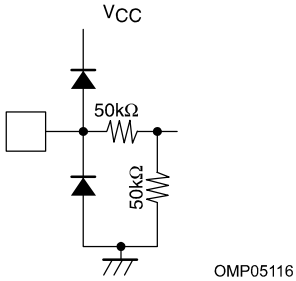
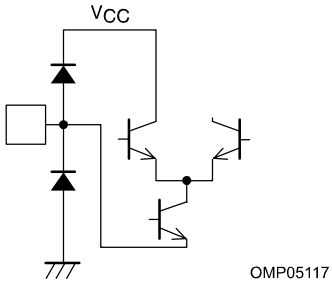
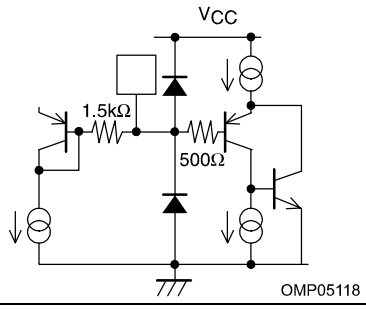
Continued on next page.

Continued from preceding page.

Pin No.	Pin name	Equivalent circuit
34	FC	
35 36	FEBL TEBL	
37	CP	
38 39 40 41 42 46 47	RREC FE TE WO PP BH PH	
43	PPN	

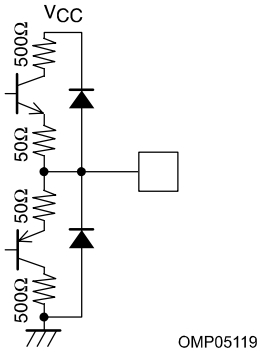
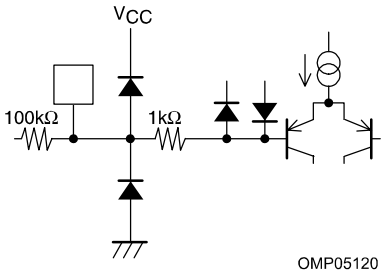
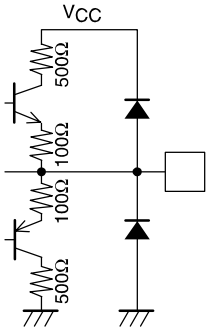
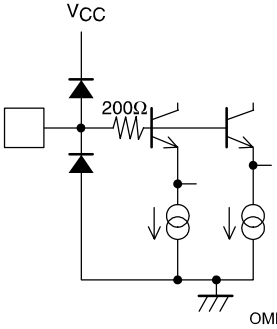
Continued on next page.

Continued from preceding page.

Pin No.	Pin name	Equivalent circuit
44	WOC	
45 57	ISET FSET	
48	SREFI	
49	BCAI	
50	PHC	

Continued on next page.

Continued from preceding page.

Pin No.	Pin name	Equivalent circuit
51 58 62	SREF PREF CAD	
52	LPC	
54 55	RFON PFOP	
59 61	RFN RFP	

Sample Application Circuit