



SANYO Semiconductors

# DATA SHEET

## LB11620GP — Monolithic Digital IC Brushless Motor Driver

### Overview

The LB11620GP is a direct PWM drive pre-driver IC that is optimal for three-phase power brushless motors. A motor driver circuit with the desired output capability (voltage and current) can be implemented by adding discrete transistors or other power devices to the outputs of this IC. Since the LB11620GP is provided in a miniature package, it is also appropriate for use with miniature motors as well.

### Features

- Three-phase bipolar drive
- Direct PWM drive (input of either a control voltage or a variable-duty PWM signal)
- Built-in forward/reverse switching circuit
- 5V regulator output (VREG pin)
- Built-in current limiter circuit (0.25V (typical) reference voltage)
- Built-in under voltage protection circuit
- Built-in automatic recovery type constraint protection circuit (ON: OFF=1: 18) with protection operating state discrimination output (RD pin)
- Hall signal pulse outputs

### Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V <sub>CC</sub> max	V <sub>CC</sub> pin	18	V
Output current	I <sub>O</sub> max	UL, VL, WL, UH, VH, WH pins	30	mA
Allowable power dissipation	P <sub>d</sub> max	*Mounted on a circuit board.	1.0	W
Operating temperature	T <sub>opr</sub>		-30 to +100	°C
Storage temperature	T <sub>stg</sub>		-55 to +150	°C

\* Mounted on a circuit board: 40.0mm×50.0mm×0.8mm, glass epoxy board.

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## Recommended Operating Ranges at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range 1-1	$V_{CC1-1}$	$V_{CC}$ pin	8 to 17	V
Supply voltage range 1-2	$V_{CC1-2}$	$V_{CC}$ pin, with $V_{CC}$ shorted to VREG	4.5 to 5.5	V
Output current	$I_O$	UL, VL, WL, UH, VH, WH pins	25	mA
5 V constant voltage output current	IREG		-30	mA
HP pin voltage	VHP		0 to 17	V
HP pin output current	IHP		0 to 15	mA
RD pin voltage	VRD		0 to 17	V
RD pin output current	IRD		0 to 15	mA

## Electrical Characteristics at $T_a = 25^\circ\text{C}$ , $V_{CC} = 12\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage 1	$I_{CC1}$			12	16	mA
<b>5V constant voltage output (VREG pin)</b>						
Output voltage	VREG		4.7	5.0	5.3	V
Line regulation	$\Delta V_{REG1}$	$V_{CC} = 8$ to $17\text{V}$		40	100	mV
Load regulation	$\Delta V_{REG2}$	$I_O = -5$ to $-20\text{mA}$		10	30	mV
Temperature coefficient	$\Delta V_{REG3}$	Design target		0		$\text{mV}/^\circ\text{C}$
<b>Low-voltage protection circuit (VREG pin)</b>						
Operating voltage	VSDL		3.5	3.7	3.9	V
Clear voltage	VSDH		3.95	4.15	4.35	V
Hysteresis	$\Delta V_{SD}$		0.3	0.45	0.6	V
<b>Output Block</b>						
Output voltage 1-1	$V_{OUT1-1}$	Low level $I_O = 400\mu\text{A}$		0.2	0.5	V
Output voltage 1-2	$V_{OUT1-2}$	Low level $I_O = 10\text{mA}$		0.9	1.2	V
Output voltage 2	$V_{OUT2}$	High level $I_O = -20\text{mA}$	$V_{CC-1.1}$	$V_{CC-0.9}$		V
Output leakage current	$I_{Oleak}$				10	$\mu\text{A}$
<b>Hall Amplifier Block</b>						
Input bias current	IHB (HA)		-2	-0.5		$\mu\text{A}$
Common-mode input voltage range 1	VICM1	When a Hall effect sensor is used	0.5		$V_{CC-2.0}$	V
Common-mode input voltage range 2	VICM2	For single-sided input bias (Hall IC application)	0		$V_{CC}$	V
Hall input sensitivity			80			$\text{mVp-p}$
Hysteresis	$\Delta V_{IN}$ (HA)		15	24	40	mV
Input voltage low $\rightarrow$ high	VSLH (HA)		5	12	20	mV
Input voltage high $\rightarrow$ low	VSHL (HA)		-20	-12	-5	mV
<b>PWM Oscillator (PWM pin)</b>						
High-level output voltage	$V_{OH}$ (PWM)		2.75	3.0	3.25	V
Low-level output voltage	$V_{OL}$ (PWM)		1.2	1.35	1.5	V
External capacitor charge current	ICHG	$V_{PWM} = 2.1\text{V}$	-120	-90	-65	$\mu\text{A}$
Oscillator frequency	f (PWM)	$C = 2000\text{pF}$		22		kHz
Amplitude	V (PWM)		1.4	1.6	1.9	Vp-p
<b>EL+ pin</b>						
Input bias current	IB (CTL)		-1		1	$\mu\text{A}$
Common-mode input voltage range	VICM		0		$V_{REG-1.7}$	V
Input voltage 1	VCTL1	Output duty 100%		3.0		V
Input voltage 2	VCTL2	Output duty 0%		1.35		V
Input voltage 1L	VCTL1L	Design target value. When $V_{REG} = 4.7\text{V}$ , 100%		2.82		V
Input voltage 2L	VCTL2L	Design target value. When $V_{REG} = 4.7\text{V}$ , 0%		1.29		V
Input voltage 1H	VCTL1H	Design target value. When $V_{REG} = 5.3\text{V}$ , 100%		3.18		V
Input voltage 2H	VCTL2H	Design target value. When $V_{REG} = 5.3\text{V}$ , 0%		1.44		V

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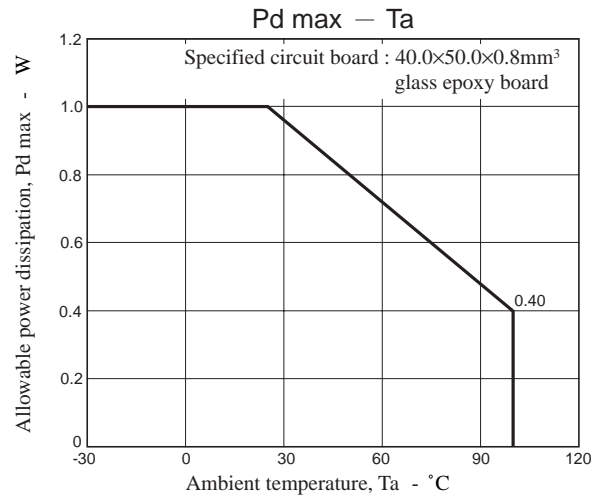
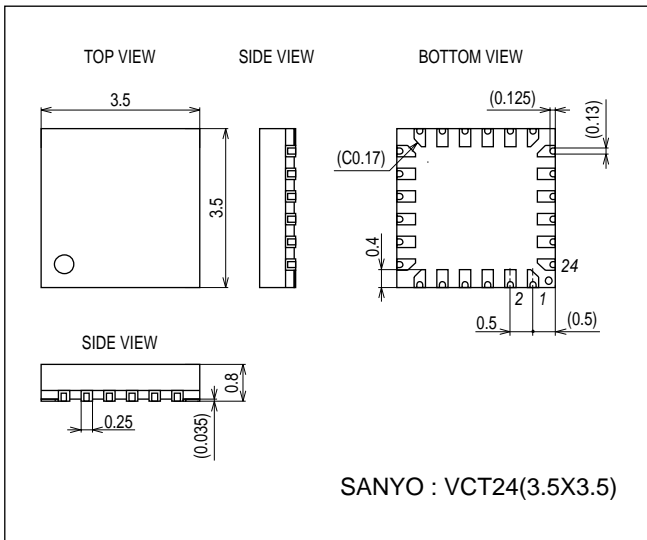
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
<b>HP pin</b>						
Output saturation voltage	VHPL	$I_O = 10\text{mA}$		0.2	0.5	V
Output leakage current	IHPleak	$V_O = 18\text{V}$			10	$\mu\text{A}$
<b>CSD oscillator (CSD pin)</b>						
High-level output voltage	$V_{OH}$ (CSD)		2.7	3.0	3.3	V
Low-level output voltage	$V_{OL}$ (CSD)		0.7	1.0	1.3	V
External capacitor charge current	ICHG1	$V_{CSD} = 2\text{V}$	-3.15	-2.5	-1.85	$\mu\text{A}$
External capacitor discharge current	ICHG2	$V_{CSD} = 2\text{V}$	0.1	0.14	0.18	$\mu\text{A}$
Charge/discharge current ratio	RCSD	Charge current /discharge current	15	18	21	Times
<b>RD pin</b>						
Low-level output voltage	VRDL	$I_O = 10\text{mA}$		0.2	0.5	V
Output leakage current	IL (RD)	$V_O = 18\text{V}$			10	$\mu\text{A}$
<b>Current limiter circuit (RF pin)</b>						
Limiter voltage	VRF	RF-GND	0.225	0.25	0.275	V
<b>PWMIN pin</b>						
Input frequency	f (PI)				60	kHz
High-level input voltage	$V_{IH}$ (PI)		2.0		VREG	V
Low-level input voltage	$V_{IL}$ (PI)		0		1.0	V
Input open voltage	$V_{IO}$ (PI)		VREG-0.5		VREG	V
Hysteresis	$V_{IS}$ (PI)		0.2	0.25	0.4	V
High-level input current	$I_{IH}$ (PI)	$V_{PWMIN} = V_{REG}$	-10	0	10	$\mu\text{A}$
Low-level input current	$I_{IL}$ (PI)	$V_{PWMIN} = 0\text{V}$	-130	-90		$\mu\text{A}$
<b>F/R pin</b>						
High-level input voltage	$V_{IH}$ (FR)		2.0		VREG	V
Low-level input voltage	$V_{IL}$ (FR)		0		1.0	V
Input open voltage	$V_{IO}$ (FR)		VREG-0.5		VREG	V
Hysteresis	$V_{IS}$ (FR)		0.2	0.25	0.4	V
High-level input current	$I_{IH}$ (FR)		-10	0	10	$\mu\text{A}$
Low-level input current	$I_{IL}$ (FR)		-130	-90		$\mu\text{A}$
<b>N1 pin</b>						
High-level input voltage	$V_{IH}$ (N1)		2.0		VREG	V
Low-level input voltage	$V_{IL}$ (N1)		0		1.0	V
Input open voltage	$V_{IO}$ (N1)		VREG-0.5		VREG	V
High-level input current	$I_{IH}$ (N1)	$V_{N1} = V_{REG}$	-10	0	10	$\mu\text{A}$
Low-level input current	$I_{IL}$ (N1)	$V_{N1} = 0\text{V}$	-130	-100		$\mu\text{A}$

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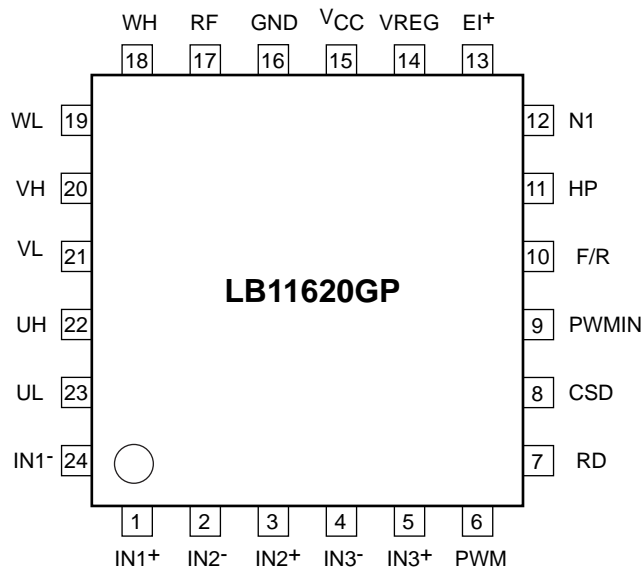
## Package Dimensions

unit : mm (typ)

3322A



## Pin Assignment



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• Three-Phase Logic Truth Table (IN = “H” indicates the state where  $IN^+ > IN^-$ )

	F/R = “L”			F/R=“H”			Output	
	IN1	IN2	IN3	IN1	IN2	IN3	PWM	
1	H	L	H	L	H	L	VH	UL
2	H	L	L	L	H	H	WH	UL
3	H	H	L	L	L	H	WH	VL
4	L	H	L	H	L	H	UH	VL
5	L	H	H	H	L	L	UH	WL
6	L	L	H	H	H	L	VH	WL

• PWMIN pin

Input state	State
High or open	Output off
Low	Output on

If the PWM pin is not used, the input must be held at the low level.

• N1 pin

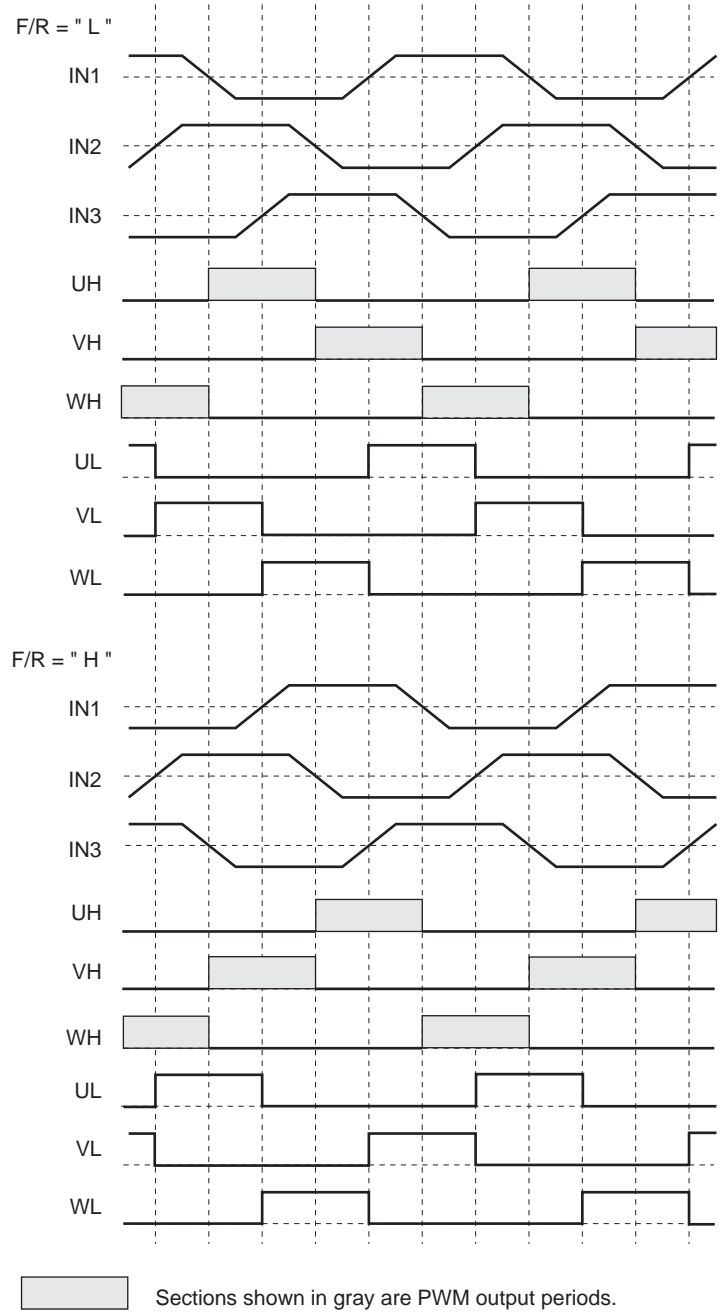
Input state	HP output
High or open	Three Hall sensor synthesized output
Low	Single Hall sensor output

### Explanation of Pin Functions

Pin No.	Pin	Description
1, 24 3, 2 5, 4	IN1 <sup>+</sup> , IN1 <sup>-</sup> IN2 <sup>+</sup> , IN2 <sup>-</sup> IN3 <sup>+</sup> , IN3 <sup>-</sup>	Hall sensor inputs from each motor phase. The logic high state indicates that $IN^+ > IN^-$ . If inputs are provided by a Hall effect sensor IC, the common-mode input range is expanded by biasing either the + or - input.
6	PWM	Functions as both the PWM oscillator frequency setting pin and the initial reset pulse setting pin. Connect a capacitor between this pin and ground.
7	RD	Lock (motor constrained) detection state output. This output is turned on when the motor is turning and off when the lock protection function detects that the motor has been stopped. This is an open collector output.
8	CSD	Sets the operating time for the lock protection circuit. Connect a capacitor between this pin and ground. Connect this pin to ground if the lock protection function is not used.
9	PWMIN	PWM pulse signal input. The output goes to the drive state when this pin is low and to the off state when this pin is high or open. To use this pin for control, a CTL amplifier input such that the TOC pin voltage goes to the 100% duty state must be provided.
10	F/R	Forward/reverse control input
11	HP	Hall signal output (HP output). This provides either a single Hall sensor output or a synthesized 3-sensor output.
12	N1	Hall signal output (HP output) selection
13	EI+	CTL amplifier + (no inverting) input. The PWMIN pin must be held at the low level to use this input for motor control
14	VREG	5V regulator output (Used as the control circuit power supply. A low-voltage protection circuit is built in.) Connect a capacitor between this pin and ground for stabilization.
15	V <sub>CC</sub>	Power supply. Connect a capacitor between this pin and ground to prevent noise and other disturbances from affecting this IC.
16	GND	Ground
17	RF	Output current detection. The current detection resistor (Rf) voltage is sensed by the RF pin to implement current detection. The maximum output current is set by RF to be $I_{OUT} = 0.25/R_f$ .
22 20 18	UH VH WH	Outputs (PWM outputs). These are push-pull outputs.
23 21 19	UL VL WL	Outputs These are push-pull outputs.

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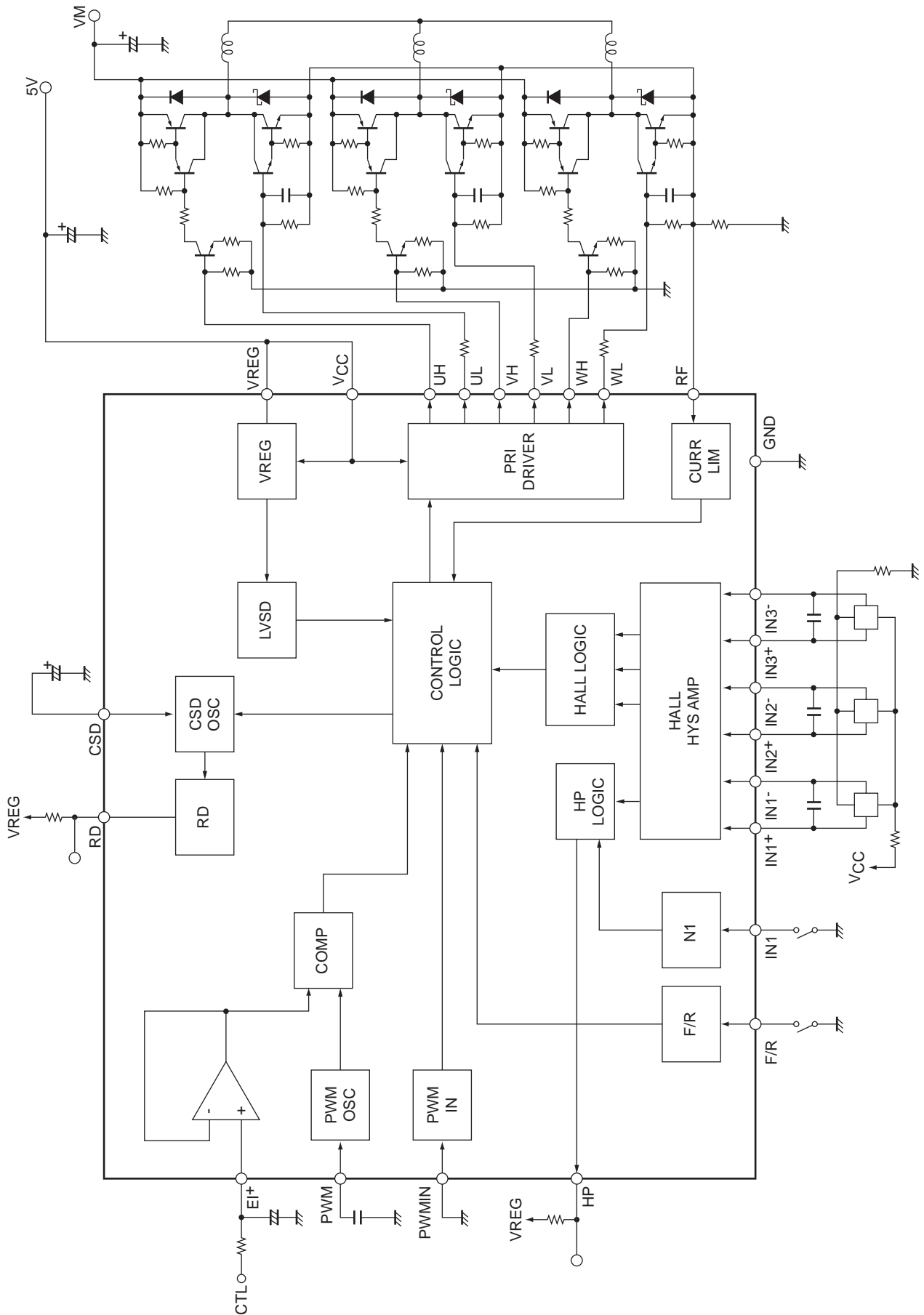
## Hall Sensor Signal Input/Output Timing Chart



**Block Diagram and Application Example 1**

Bipolar transistor drive (high side PWM)

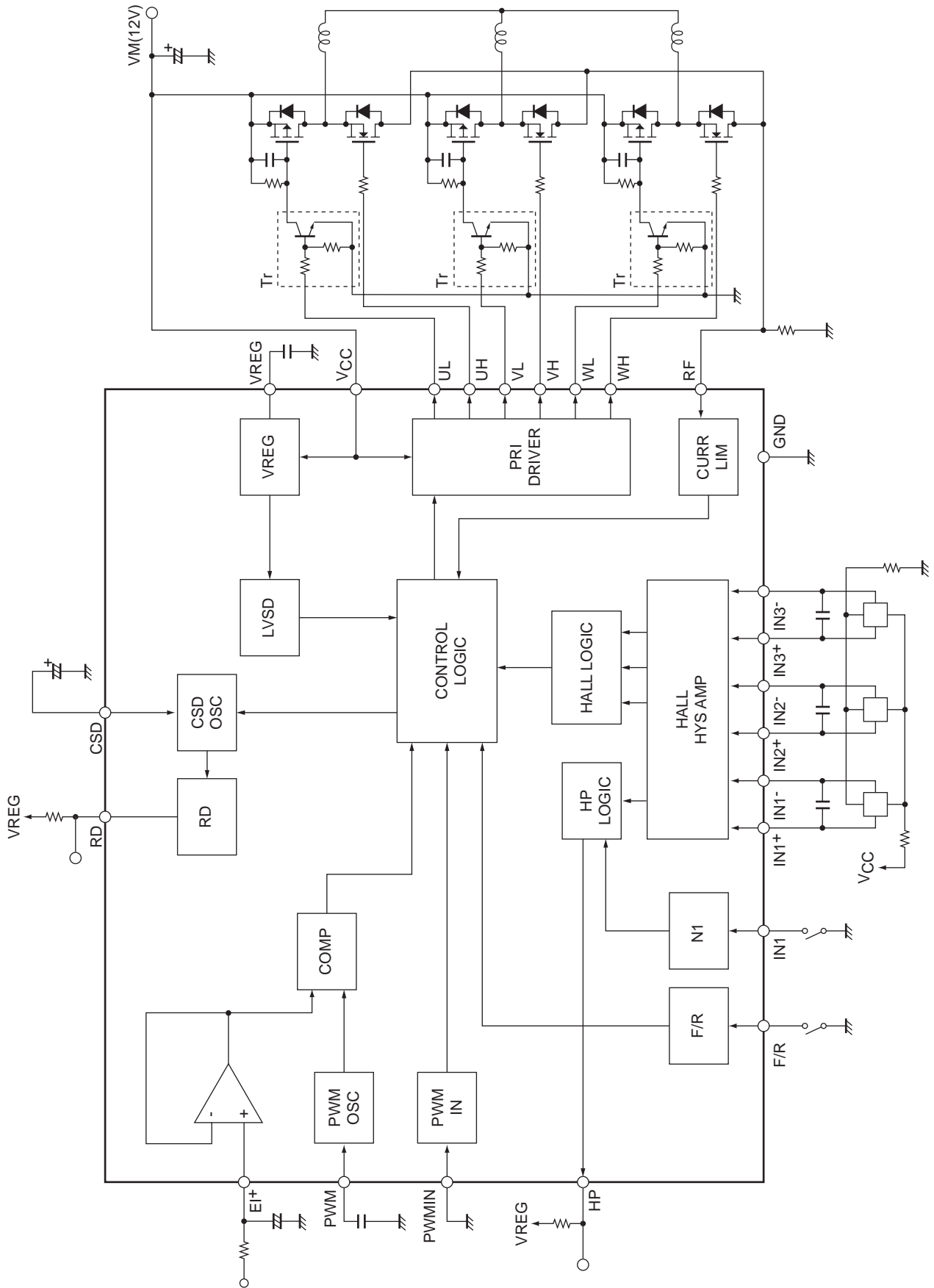
Using a 5V power supply



**Application Example 2**

54 MOS transistor drive (low side PWM)

Using a 12V single-voltage power supply

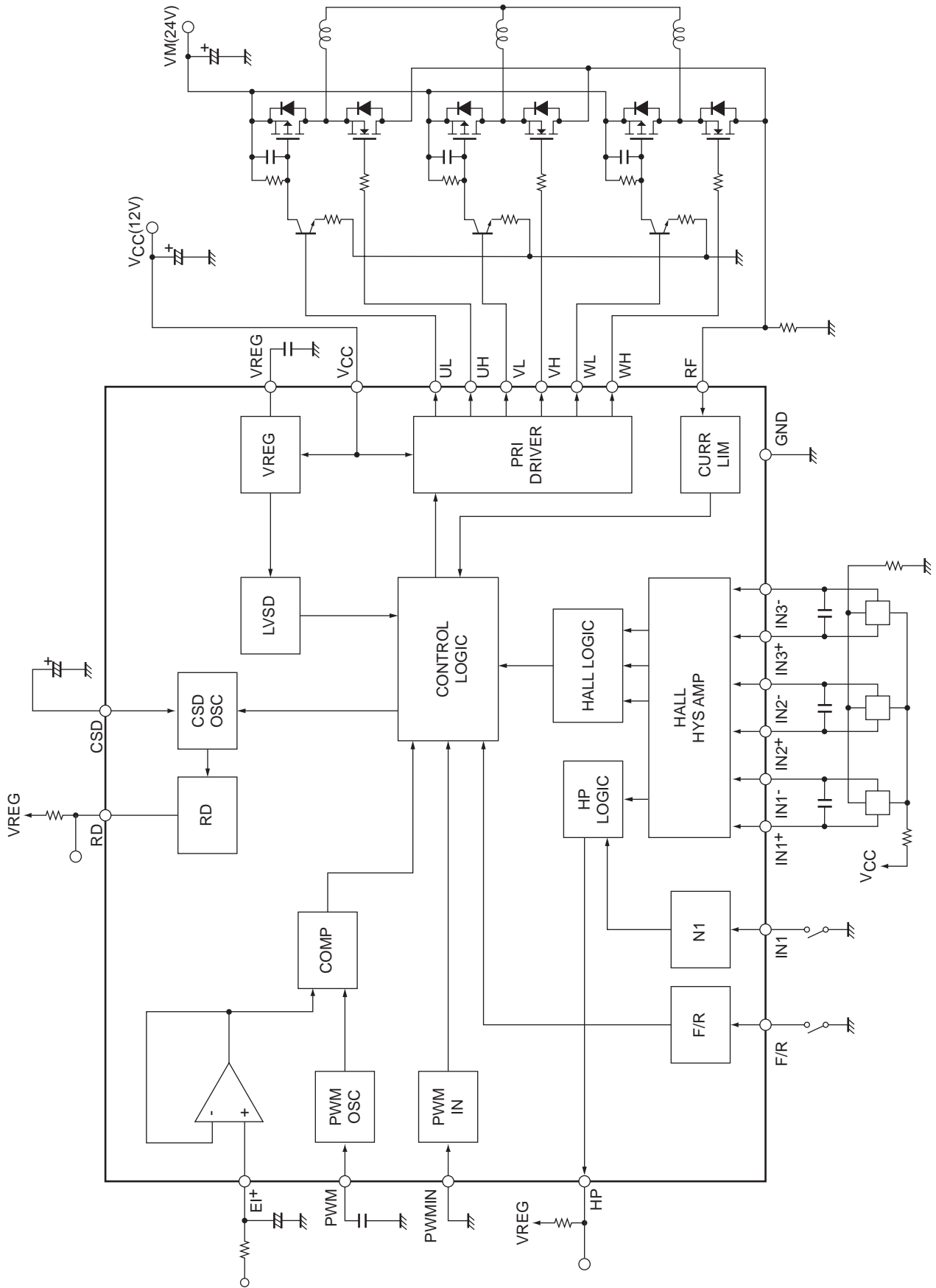




**Application Example 3**

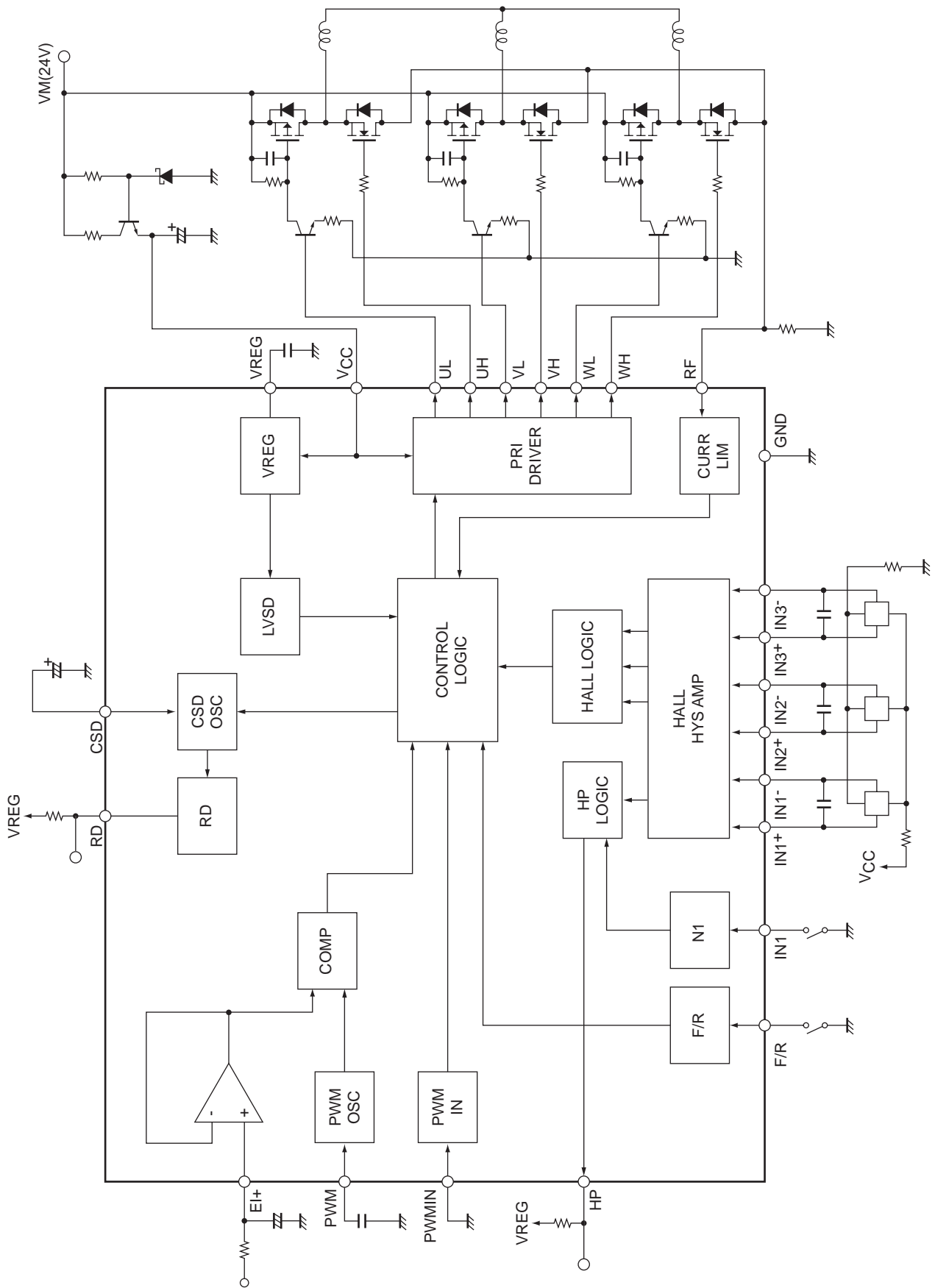
MOS transistor drive (low side PWM)

Using a  $V_{CC} = 12V$ ,  $V_M = 24V$  power supply system



**Application Example 4**

MOS transistor drive (low side PWM)  
Using a 24V single-voltage power supply



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## Pin Functions

PIN No.	PIN name	Function	Equivalent circuit
24 1 2 3 4 5	IN1- IN1+ IN2- IN2+ IN3- IN3+	Hall input pin. IN+ > IN- to "H", IN+ < IN- to "L". Connect the capacitor between IN+ and IN- when the noise of the hall signal becomes a problem.	
6	PWM	Functions as both the PWM oscillator frequency setting pin and the initial reset pulse setting pin. Connect a capacitor between this pin and ground. It is possible to set it to about 22kHz with C=2000pF.	
7	RD	Lock (motor constrained) detection state output. This output is turned on when the motor is turning and off when the lock protection function detects that the motor has been stopped.	
11	HP	Hall signal output pin. Two kinds of outputs can be selected by setting the N1 pin.	
8	CSD	Sets the operating time for the lock protection circuit. Connect a capacitor between this pin and ground. Connect this pin to ground if the lock protection function is not used.	
9	PWMIN	PWM pulse signal input. The output goes to the drive state when this pin is low and to the off state when this pin is high or open. To use this pin for control, a CTL amplifier input such that the TOC pin voltage goes to the 100% duty state must be provided.	
10	F/R	Forward/reverse control input.	
12	N1	Hall signal output (HP output) selection.	

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PIN No.	PIN name	Function	Equivalent circuit
13	EI+	CTL amplifier + (no inverting) input. The PWMIN pin must be held at the low level to use this input for motor control.	
14	VREG	Stabilizing supply output pin. (5V output) Connect a capacitor between this pin and ground for stabilization. (about 0.1μF level)	
15	VCC	Power supply. Connect a capacitor between this pin and ground to prevent noise and other disturbances from affecting this IC.	
16	GND	Ground	
17	RF	Output current sensing pin. The low resistance is connected between RF and GND. It sets it by output maximum current $I_{OUT}=0.25/R_f$ .	
18 19 20 21 22 23	WH WL VH VL UH UL	Output pin. (Driving external TR output) The duty is controlled on UH, VH, and WH side.	

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