Ordering number : ENN7257A

Monolithic Digital IC

LB11872H

Three-Phase Brushless Motor Driver for Polygonal Mirror Motors

Overview

The LB11872H is a three-phase brushless motor driver developed for driving the motors used for the polygonal mirror in laser printers and similar applications. It can implement, with a single IC chip, all the circuits required for polygonal mirror drive, including speed control and driver functions. The LB11872H can implement motor drive within minimal drive noise due to its use of current linear drive.

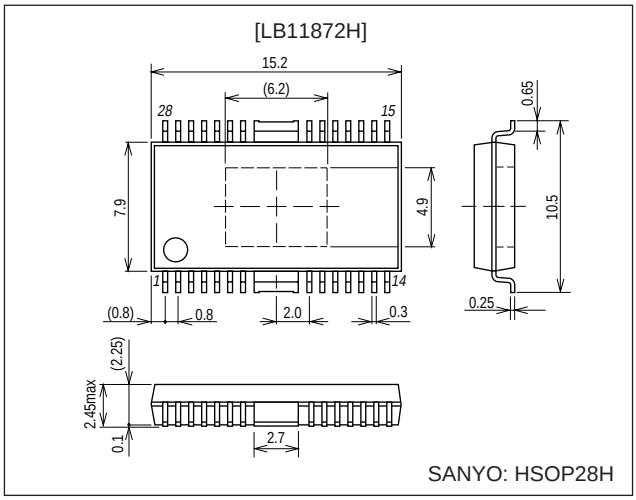
Functions and Features

- Three-phase bipolar current linear drive + midpoint control circuit
- PLL speed control circuit
- Speed is controlled by an external clock signal.
- Supports Hall FG operation.
- Built-in output saturation prevention circuit
- Phase lock detection output (with masking function)
- Includes current limiter, thermal protection, rotor constraint protection, and low-voltage protection circuits on chip.
- On-chip output diodes.

Package Dimensions

unit: mm

3233A-HSOP28H



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		30	V
Output current	I_O max	T ≤ 500 ms	1.2	A
Allowable power dissipation 1	Pd max1	Independent IC	0.8	W
Allowable power dissipation 2	Pd max2	Mounted on a PCB (114.3 × 76.1 × 1.6 mm, glass epoxy)	2.0	W
Operating temperature	Topr		–20 to +80	°C
Storage temperature	Tstg		–55 to +150	°C

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Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	V_{CC}		10 to 28	V
6.3 V regulator-voltage output current	IREG		0 to –20	mA
LD pin applied voltage	VLD		0 to 28	V
LD pin output current	ILD		0 to 15	mA
FGS pin applied voltage	VFG		0 to 28	V
FGS pin output current	IFG		0 to 10	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = VM = 24 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current 1	$I_{CC}1$	Stop mode		5	7	mA
Supply curren 2	$I_{CC}2$	Start mode		17	22	mA
[Output Saturation Voltages VAGC = 3.5 V]						
SOURCE (1)	VSAT1-1	I_O = 0.5 A, RF = 0 Ω		1.7	2.2	V
SOURCE (2)	VSAT1-2	I_O = 1.0 A, RF = 0 Ω		2.0	2.7	V
SINK (1)	VSAT2-1	I_O = 0.5 A, RF = 0 Ω		0.4	0.9	V
SINK (2)	VSAT2-2	I_O = 1.0 A, RF = 0 Ω		1.0	1.7	V
Output leakage current	I_O (LEAK)	V_{CC} = 28 V			100	µA
[6.3 V Regulator-Voltage Output]						
Output voltage	VREG		5.90	6.25	6.60	V
Voltage regulation	ΔVREG1	V_{CC} = 9.5 to 28 V		50	100	mV
Load regulation	ΔVREG2	Iload = –5 to –20 mA		10	60	mV
Temperature coefficient	ΔVREG3	Design target value		0		mV/°C
[Hall Amplifier Block]						
Input bias current	IB (HA)	Differential input: 50 mVp-p		2	10	µA
Differential input voltage range	VH_{IN}	SIN wave input	50		*600	mVp-p
Common-phase input voltage range	VICM	Differential input: 50 mVp-p	2.0		V_{CC} – 2.5	V
Input offset voltage	VIOH	Design target value	–20		20	mV
[FG Amplifier and Schmitt Block (IN1)]						
Input amplifier gain	GFG			5		deg
Input hysteresis (high to low)	VSHL			0		mV
Input hysteresis (low to high)	VSLH			–10		mV
Hysteresis width	VFGL	Input conversion	4	7	12	mV
[Low-Voltage Protection Circuit]						
Operating voltage	VSD		8.4	8.8	9.2	V
Hysteresis width	ΔVSD		0.2	0.4	0.6	V
[Thermal Protection Circuit]						
Thermal shutdown operating temperature	TSD	Design target value (junction temperature)	150	180		°C
Hysteresis width	ΔTSD	Design target value (junction temperature)		40		°C
[Current Limiter Operation]						
Acceleration limit voltage	VRF1		0.53	0.59	0.65	V
Deceleration limit voltage	VRF2		0.32	0.37	0.42	V
[Error Amplifier]						
Input offset voltage	VIO (ER)	Design target value	–10		10	mV
Input bias current	IB (ER)		–1		1	µA
High-level output voltage	V_{OH} (ER)	I_{OH} = –500 µA	VREG – 1.2	VREG – 0.9		V
Low-level output voltage	V_{OL} (ER)	I_{OL} = 500 µA		0.9	1.2	V
DC bias level	VB (ER)		–5%	1/2VREG	5%	V
[Phase Comparator Output]						
High-level output voltage	VPDH	I_{OH} = –100 µA	VREG – 0.2	VREG – 0.1		V
Low-level output voltage	VPDL	I_{OL} = 100 µA		0.2	0.3	V
Output source current	IPD+	VPD = VREG/2			–500	µA
Output sink current	IPD–	VPD = VREG/2	1.5			mA

Note*: Since kickback can occur in the output waveform if the Hall input amplitude is too large, the Hall input amplitudes should be held to under 350 mVp-p.

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Lock Detection Output]						
Output saturation voltage	VLD (SAT)	ILD = 10 mA		0.15	0.5	V
Output leakage current	ILD (LEAK)	VLD = 28 V			10	µA
[FG Output]						
Output saturation voltage	VFG (SAT)	IFG = 5 mA		0.15	0.5	V
Output leakage current	IFG (LEAK)	VFG = 28 V			10	µA
[Drive Block]						
Dead zone width	VDZ	With the phase is locked	50	100	300	mV
Output idling voltage	VID				6	mV
Forward gain 1	GDF+1	With phase locked	0.4	0.5	0.6	deg
Forward gain 2	GDF+2	With phase unlocked	0.8	1.0	1.2	deg
Reverse gain 1	GDF–1	With phase locked	–0.6	–0.5	–0.4	deg
Reverse gain 2	GDF–2	With phase unlocked	–0.8	–1.0	–1.2	deg
Acceleration command voltage	VSTA		5.0	5.6		V
Deceleration command voltage	VSTO			0.8	1.5	V
Forward limiter voltage	VL1	Rf = 22 Ω	0.53	0.59	0.65	V
Reverse limiter voltage	VL2	Rf = 22 Ω	0.32	0.37	0.42	V
[CSD Oscillator Circuit]						
Oscillation frequency	f_{OSC}	C = 0.022 µF		31		Hz
High-level pin voltage	V_{CSDH}		4.3	4.8	5.3	V
Low-level pin voltage	V_{CSDL}		0.75	1.15	1.55	V
External capacitor charge and discharge current	I_{CHG}		3	5	7	µA
Lock detection delay count	CSDCT1			7		
Clock cutoff protection operating count	CSDCT2			2		
Lock protection count	CSDCT3			31		
Initial reset voltage	V_{RES}			0.60	0.80	V
[Clock Input Block]						
External input frequency	f_{CLK}		400		10000	Hz
High-level input voltage	V_{IH} (CLK)	Design target value	2.0		VREG	V
Low-level input voltage	V_{IL} (CLK)	Design target value	0		1.0	V
Input open voltage	V_{IO} (CLK)		2.7	3.0	3.3	V
Hysteresis width	V_{IS} (CLK)	Design target value	0.1	0.2	0.3	V
High-level input current	I_{IH} (CLK)	V (CLK) = VREG		140	185	µA
Low-level input current	I_{IL} (CLK)	V (CLK) = 0 V	–185	–140		µA
[S/S Pin]						
High-level input voltage	V_{IH} (S/S)		2.0		VREG	V
Low-level input voltage	V_{IL} (S/S)		0		1.0	V
Input open voltage	V_{IO} (S/S)		2.7	3.0	3.3	V
Hysteresis width	V_{IS} (S/S)		0.1	0.2	0.3	V
High-level input current	I_{IH} (S/S)	V (S/S) = VREG		140	185	µA
Low-level input current	I_{IL} (S/S)	V (S/S) = 0 V	–185	–140		µA

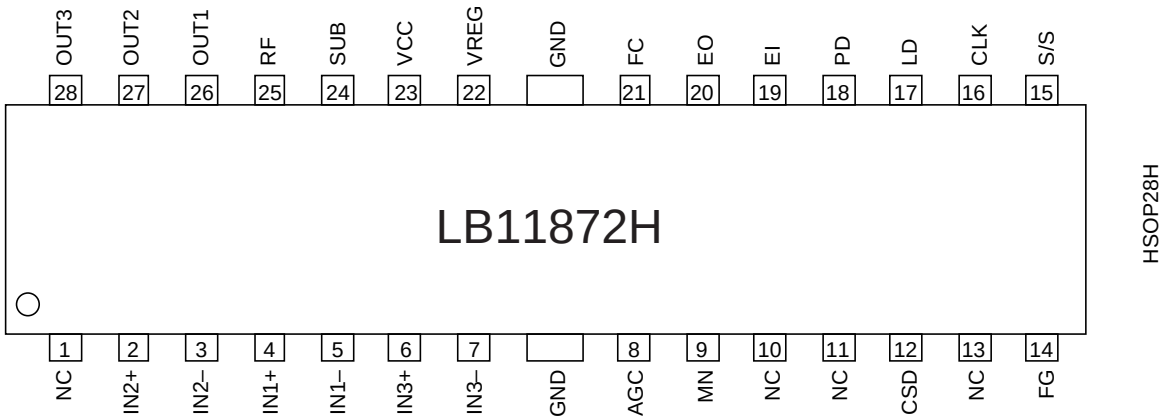
Three-Phase Logic

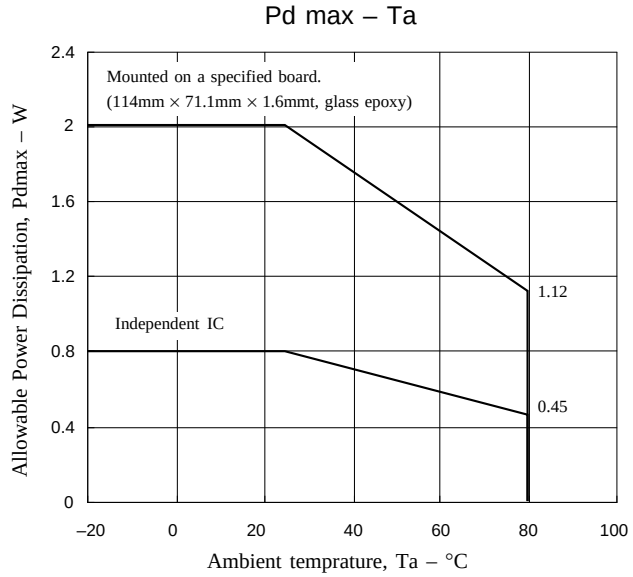
OUT1 to OUT3 (H: Source, L: Sink)

IN1	IN2	IN3	OUT1	OUT2	OUT3
H	L	H	L	H	M
H	L	L	L	M	H
H	H	L	M	L	H
L	H	L	H	L	M
L	H	H	H	M	L
L	L	H	M	H	L

For IN1 to IN3, “H” means that IN+ is greater than IN–, and “L” means IN– is greater than IN+.
For OUT1 to OUT3, “H” means the output is a source, and “L” means that it is a sink.

Pin Arrangement

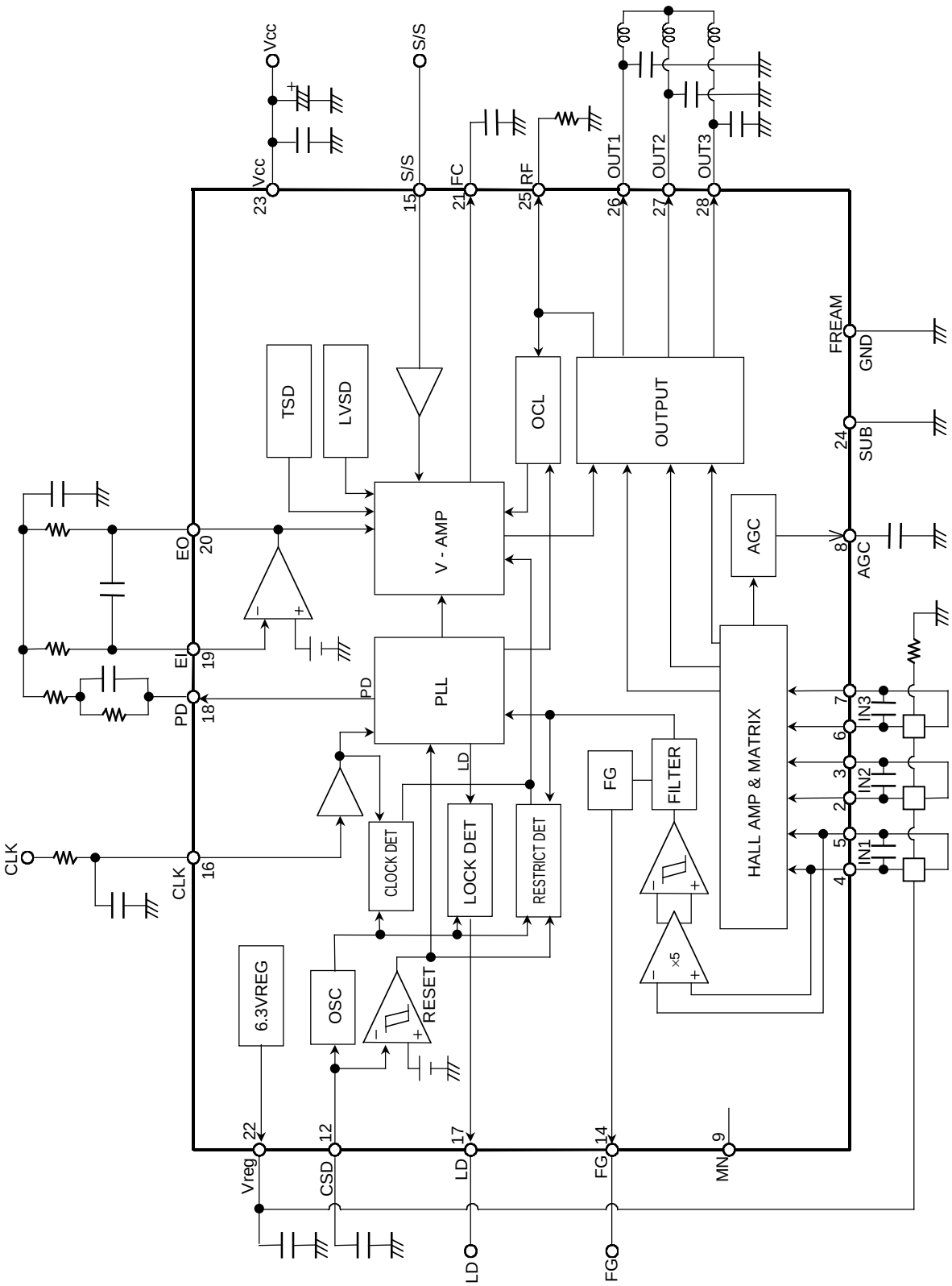




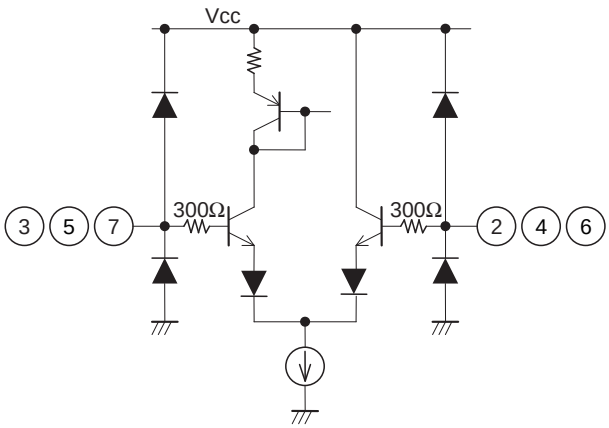
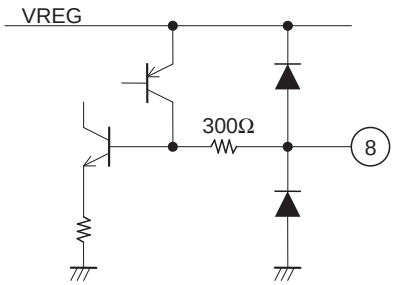
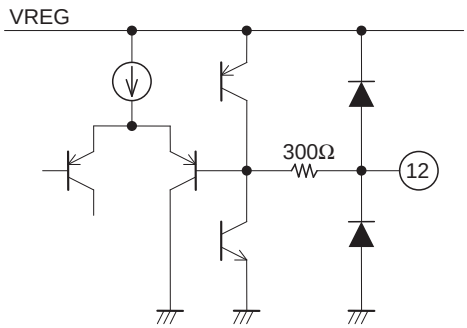
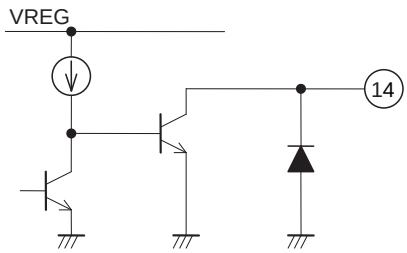
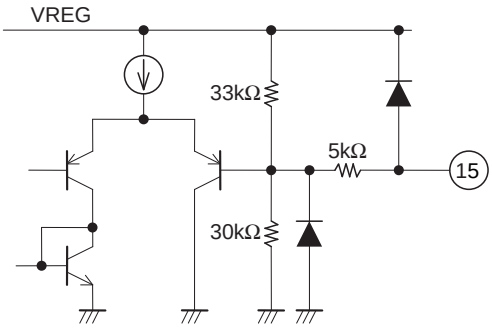
Pin Functions

Pin No.	Symbol	Pin	
FRAME	GND	GND pin	
1	NC	NC (No connection) pin	
2 to 7	IN1+ to IN3+ IN1– to IN3–	Hall sensor input pins	These pins input the Hall effect sensor signal for each phase. The logic of these inputs is that the input is “high” when VIN+ is greater than VIN–.
8	AGC	Frequency characteristics correction pin	Insert a capacitor between pin 8 and ground.
9	MN	Test pin	This pin must be left open.
10	NC		
11	NC		
12	CSD	Phase lock detection chattering prevention pin	Insert a capacitor between pin 12 and ground.
13	NC		
14	FG	FG output pin	This is an open-collector output
15	S/S	Start/stop switching pin	Low: start mode
16	CLK	Clock signal input pin	
17	LD	Phase lock detection output pin	This pin goes to the on state when the phase is locked. It is an open-collector output.
18	PD	Phase comparator output pin	
19	EI	Error amplifier input pin	
20	EO	Error amplifier output pin	
21	FC	Frequency characteristics correction pin	Insert a capacitor between pin 21 and ground.
22	VREG	Stabilized power supply output pin	Insert a capacitor between pin 22 and ground.
23	V_{CC}	Power supply pin	
24	SUB	SUBGND pin	Connect this pin to ground.
25	Rf	Output current detection pin	Insert a resistor between pin 25 and ground.
26 to 28	OUT1 to 3	Output pins	

LB11872H Equivalent Circuit Block Diagram



Pin Circuits and Functions

Pin No.	Pin	Function	Equivalent circuit
2 3 4 5 6 7	IN2+ IN2– IN1+ IN1– IN3+ IN3–	Hall effect sensor signal inputs These inputs are high when IN+ is greater than IN- and low when IN- is greater than IN+. Insert capacitors between the IN+ and IN– pins to reduce noise. An amplitude of over 50 mA p-p and under 350 mVp-p is desirable for the Hall input signals. Kickback can occur in the output waveform if the Hall input amplitude is over 350 mVp-p.	
8	AGC	AGC amplifier frequency characteristics correction. Insert a capacitor (about 0.022 µF) between this pin and ground.	
9	MN	Monitor pin This pin should be left open in normal operation.	
12	CSD	Used for both initial reset pulse generation and as the reference time for constraint protection circuits. Insert a capacitor between this pin and ground.	
14	FG	FG pulse output. This is an open-collector output.	
15	S/S	Start/stop control. Low: Start 0 to 1.0 V High: Stop 2.0 V to VREG This pin goes to the high level when open.	

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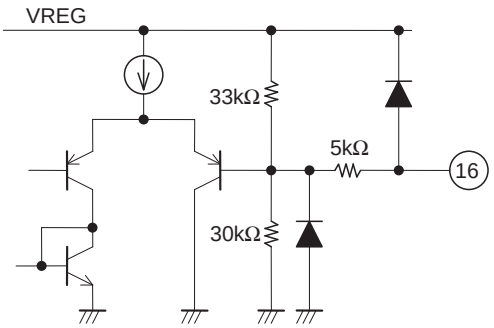
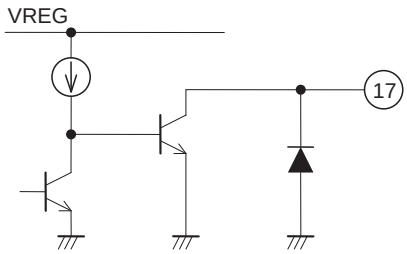
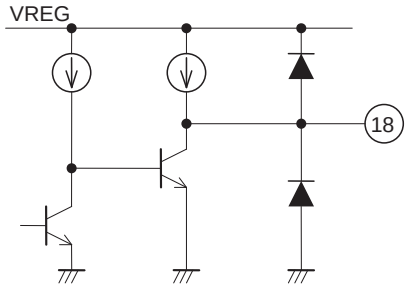
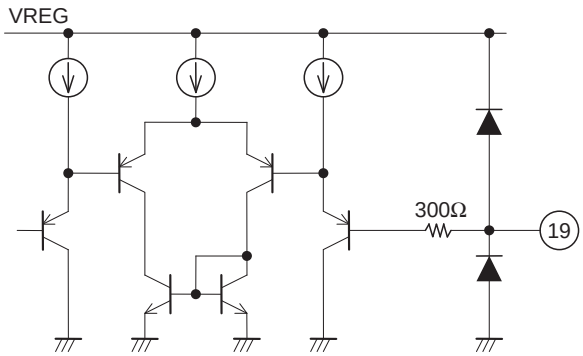
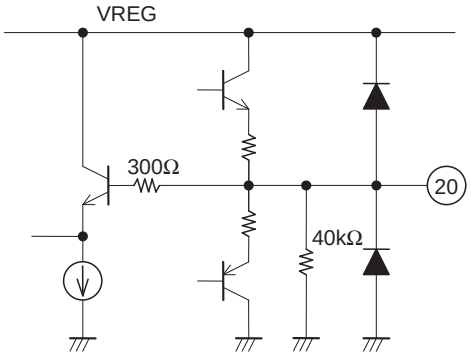
Pin No.	Pin	Function	Equivalent circuit
16	CLK	Clock input. Low: 0 to 1.0 V High: 2.0 V to VREG This pin goes to the high level when open.	
17	LD	Phase locked state detection output This output goes to the on state when the PLL locked state is detected. This is an open-collector output.	
18	PD	Phase comparator output (PLL output) This pin output the phase error as a pulse signal with varying duty.The output current increases as the duty becomes smaller.	
19	EI	Error amplifier in put pin.	
20	EO	Error amplifier output pin. The output current increases when this output is high.	

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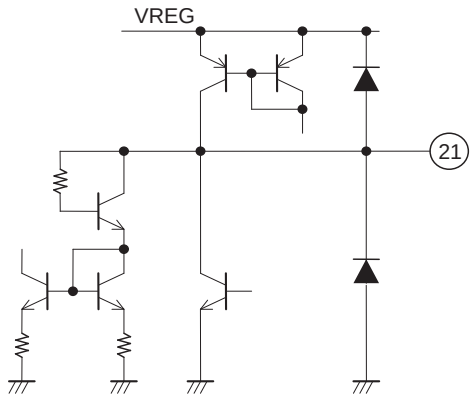
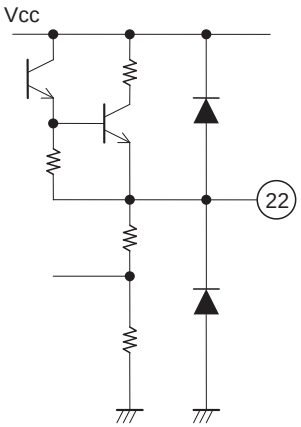
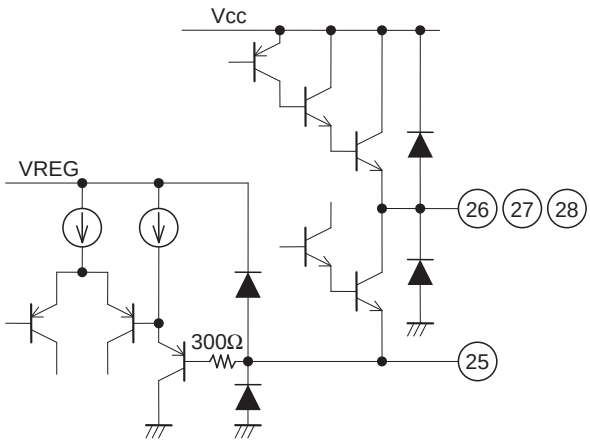
Pin No.	Pin	Function	Equivalent circuit
21	FC	Control amplifier frequency correction. Inserting a capacitor (about 5600 pF) between this pin and ground will stop closed loop oscillation in the current control system. The output current response characteristics will be degraded if the capacitor is too large.	
22	VREG	Stabilized power supply (6.3 V) Insert a capacitor (about 0.1 µF) between this pin and ground for stabilization.	
23	V_{CC}	Power supply	
24	SUB	SUB pin. Connect this pin to ground.	
25	RF	Output current detection. Insert low-valued resistors (Rf) between these pins and ground. The output current will be limited to the value set by the equation $I_{OUT} = V_L/R_F$.	
26 27 28	OUT1 OUT2 OUT3	Motor drive outputs. If the output oscillates, insert a capacitor (about 0.1 µF) between this pin and ground.	
1 10 11 13	NC	No connection (NC) pins. These pins may be used for wiring connections.	
FRAME	GND	Ground	

Overview of the LB11872H

1. Speed Control Circuit
   This IC adopts a PLL speed control technique and provides stable motor operation with high precision and low jitter.
   This PLL circuit compares the phase error at the edges of the CLK signal (falling edges) and FG signal (rising edges (low to high transitions) on the IN1 input), and the IC uses the detected error to control the motor speed.
   During this control operation, the FG servo frequency will be the same as the CLK frequency.

   f_{FG} (servo) = f_{CLK}

2. Output Drive Circuit
   To minimize motor noise, this IC adopts three-phase full-wave current linear drive. This IC also adopts a midpoint control technique to prevent ASO destruction of the output transistors.
   Reverse torque braking is used during motor deceleration during speed switching and lock pull-in. In stop mode, the drive is cut and the motor is left in the free-running state.
   Since the output block may oscillate depending on the motor actually used, capacitors (about 0.1 µF) must be inserted between the OUT pins and ground.

3. Hall Input Signals
   This IC includes an AGC circuit that minimizes the influence on the output of changes in the Hall signal input amplitudes due to the motor used. However, note that if there are discrepancies in the input amplitudes between the individual phases, discrepancies in the output phase switching timing may occur.
   An amplitude (differential) of at least 50 mVp-p is required in the Hall input signals. However, if the input amplitude exceeds 350 mVp-p, the AGC circuit control range will be exceeded and kickback may occur in the output.
   If Hall signal input frequencies in excess of 1 kHz (the frequency in a single Hall input phase) are used, internal IC heating during startup and certain other times (that is, when the output transistors are saturated) may increase. Reducing the number of magnetic poles can be effective in dealing with problem.
   The IN1 Hall signal is used as the FG signal for speed control internally to the IC. Since noise can easily become a problem, a capacitor must be inserted across this input. However, since this could result in differences between the signal amplitudes of the three phases, capacitors must be inserted across all of the three input phases.
   Although V_{CC} can be used as the Hall element bias power supply, using VREG can reduce the chances of problems occurring during noise testing and at other times. If VREG is used, since there is no longer any need to be concerned with the upper limit of the Hall amplifier common-mode input voltage range, bias setting resistors may be used only on the low side.

4. Power Saving Circuit
   This IC goes into a power saving state that reduces the current drain in the stop state. The power saving state is implemented by removing the bias current from most of the circuits in the IC. However, the 6.3 V regulator output is provided in the power saving state.

5. Reference Clock
   Care must be taken to assure that no chattering or other noise is present on the externally input clock signal. Although the input circuit does have hysteresis, if problems do occur, the noise must be excluded with a capacitor.
   This IC includes an internal clock cutoff protection circuit. If a signal with a frequency below that given by the formula below is input, the IC will not perform normal control, but rather will operate in intermittent drive mode.

   f (Hz) ≒ 0.64 ÷ C_{CSD} C_{CSD} (µF): The capacitor inserted between the CSD pin and ground.

   When a capacitor of 0.022 µF is used, the frequency will be about 29 Hz.

   If the IC is set to the start state when the reference clock signal is completely absent, the motor will turn somewhat and then motor drive will be shut off. After the motor stops and the rotor constraint protection time elapses, drive will not be restarted, even if the clock signal is then reapplied. However, drive will restart if the clock signal is reapplied before the rotor constraint protection time elapses.

6. Rotor Constraint Protection Circuit

This IC provides a rotor constraint protection circuit to protect the IC itself and the motor when the motor is constrained physically, i.e. prevented from turning. If the FG signal (edges of one type (rising or falling edges) on the IN1 signal) does not switch within a fixed time, output drive will be turned off. The time constant is determined by the capacitor connected to the CSD pin.

<time constant (in seconds)> ≒ $30.5 \times 1.57 \times C_{CSD}$ (μF)

If a 0.02 μF capacitor is used, the protection time will be about 1.05 seconds.
To clear the rotor constraint protection state, the IC must be set to the stopped state or the power must be turned off and reapplied. If there is noise present on the FG signal during the constraint time, the rotor constraint protection circuit may not operate normally.

7. Phase Lock Signal

(1) Phase lock range

Since this IC does not include a counter or similar functionality in the speed control system, the speed error range in the phase locked state cannot be determined solely by IC characteristics. (This is because the acceleration of the changes in the FG frequency influences the range.) When it is necessary to stipulate this characteristic for the motor, the designer must determine this by measuring the actual motor state. Since speed errors occur easily in states where the FG acceleration is large, it is thought that the speed errors will be the largest during lock pull-in at startup and when unlocked due to switching clock frequencies.

(2) Masking function for the phase lock state signal

A stable lock signal can be provided by masking the short-term low-level signals due to hunting during lock pull-in. However, this results in the lock state signal output being delayed by the masking time.
The masking time is determined by the capacitor inserted between the CSD pin and ground.

<masking time (seconds)> ≒ $6.5 \times 1.57 \times C_{CSD}$ (μF)

When a 0.022 μF capacitor is used, the masking time will be about 225 ms. In cases where complete masking is required, a masking time with fully adequate margin must be used.

8. Initial Reset

To initially reset the logic circuits in start mode, the IC goes to the reset state when the CSD pin voltage goes to zero until it reaches 0.63 V. Drive output starts after the reset state is cleared. The reset time can be calculated to a good approximation using the following formula.

<reset time (seconds)> ≒ $0.13 \times C_{CSD}$ (μF)

A reset time of over 100 μs is required.

9. Current Limiter Circuit

The current limit value is determined by the resistor Rf inserted between the RF pin and ground.

$I_{LIM} = V_L/Rf$ V_L = 0.59 V (typical) (during acceleration) and 0.37 V (typical) (during deceleration)

10. Power Supply Stabilization

An adequately large capacitor must be inserted between the V_{CC} pin and ground for power supply stabilization. If diodes are inserted in the power supply lines to prevent destruction of the device if the power supply is connected with reverse polarity, the power supply line levels will be even more easily disrupted, and even larger capacitors must be used.
If high-frequency noise is a problem, a ceramic capacitor of about 0.1 μF must also be inserted in parallel.

11. VREG Stabilization

A capacitor of at least 0.1 μF must be used to stabilize the VREG voltage, which is the control circuit power supply. The capacitor must be connected as close as possible to the pins.

12. Error Amplifier External Component Values

To prevent adverse influence from noise, the error amplifier external components must be located as close to the IC as possible.

13. FRAME Pin and Heat sink Area

The FRAME pin and the heat sink area function as the control circuit ground terminal. It is desirable that this ground line and the Rf resistor ground line be grounded at a single point at the ground for the electrolytic capacitor. Thermal dissipation can be improved significantly by tightly bonding the metallic surface of the back of the IC package to the PCB with, for example, a solder with good thermal conductivity.

14. CSD Pin

The capacitor connected to the CSD pin influences several operational aspects of this IC, including the rotor constraint protection time and the phase lock signal mask time. The following are possible ways of determining the value of this capacitor.

(1) If removing chattering from the phase lock state signal is most important:
Select a capacitance that can assure an adequate mask time.

(2) If startup time is more important than chattering:
Select a capacitance such that the rotor constraint protection circuit does not operate at startup time and verify that there are no problems with the clock cutoff protection circuit and initial reset time.
Operation of the rotor constraint protection circuit may hinder the study of motor characteristics in the uncontrolled state. It is possible to only operate the initial reset function and not operate the rotor constraint protection circuit by inserting a resistor (about 390 kΩ) in parallel with the capacitor between the CSD pin and ground.

15. FC Pin

The capacitor connected to the FC pin is required for current limiter loop phase compensation. If the value is too low, the output will oscillate. If the value is too large, it will be easier for currents in excess of the limit value to flow during the current limit time (time before the circuit operates) in states where the output is saturated. (This is because the control response characteristics become worse.)

16. AGC Pin

A capacitance that allows a certain amount of smoothing of the AGC pin voltage in the motor speed range used must be selected for the capacitor connected to the AGC pin. It is also desirable to use a capacitance that allows the AGC voltage to reach an essentially stabilized voltage before the initial reset is cleared. (If the capacitance is too large, the rate of change of the AGC voltage will become slower.)

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