Ordering number : ENN7113

Monolithic Digital IC

LB11891V

Three-Phase Brushless Motor Driver for Streaming Tape Drives

Overview

The LB11891V is a 3-phase brushless motor driver IC that is optimal for streaming tape drive motors and similar applications.

Functions and Features

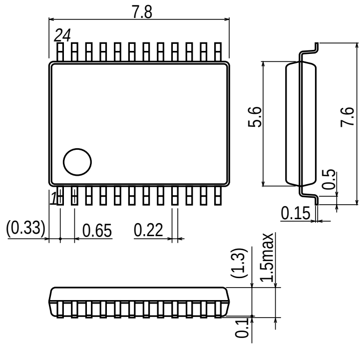
- Three-phase full-wave voltage drive (120° voltage-linear drive)
- Torque ripple correction circuit (overlap correction)
- Motor supply voltage control based speed control
- Built-in Hall sensor output FG comparator
- Fixed-phase output function
- Thermal shutdown circuit

Package Dimensions

unit: mm

3175B-SSOP24

[LB11891V]



SANYO: SSOP24 (275 mil)

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC}1$ max		10	V
	$V_{CC}2$ max		11	V
	VS max	$\leq V_{CC}2$	11	V
Maximum applied output voltage	V_O max		VS+2	V
Maximum output current	I_O max		1.0	A
Allowable power dissipation	Pd max	Independent IC	400	mW
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–55 to +150	°C

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Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{CC}1$	$V_{CC}1 \leq V_{CC}2$	2.7 to 6.0	V
	$V_{CC}2$		3.5 to 9.0	V
	VS		to $V_{CC}2$	V
Hall input amplitude	VHALL	Between the Hall sensor inputs	±20 to ±80	mVp-p

Electrical Characteristics at Ta = 25°C, $V_{CC}1$ = 3 V, $V_{CC}2$ = 4.75 V, VS = 1.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Current Drain]						
$V_{CC}1$ Current drain	$I_{CC}1$	I_{OUT} = 100 mA		5.0	9.0	mA
$V_{CC}2$ Current drain	$I_{CC}2$	I_{OUT} = 100 mA		7.0	10.0	mA
$V_{CC}1$ Quiescent current	$I_{CC}1Q$	VSTBY = 0 V		3.0	6.0	mA
$V_{CC}2$ Quiescent current	$I_{CC}2Q$	VSTBY = 0 V			100	µA
VS Quiescent current	ISQ	VSTBY = 0 V		75	100	µA
[VX1]						
High side residual voltage	VXH1	I_{OUT} = 0.2 A	0.15	0.22	0.29	V
Low side residual voltage	VXL1	I_{OUT} = 0.2 A	0.15	0.20	0.25	V
[VX2]						
High side residual voltage	VXH2	I_{OUT} = 0.5 A		0.25	0.40	V
Low side residual voltage	VXL2	I_{OUT} = 0.5 A		0.25	0.40	V
Output saturation voltage	$V_{O}sat$	I_{OUT} = 0.8 A, Sink + Source			1.40	V
Amount of overlap	O.L	RL = 39 Ω × 3, Rangle = 20 kΩ *1	73	80	87	%
Amount of overlap: difference between high and low sides	ΔO.L	(Average high side overlap amount) - (Average low side overlap amount) *1	–8		+8	%
[Hall Amplifiers]						
Input offset voltage	VHOFF	Design target value *	–5		+5	mV
Common-mode input range	VHCM	Rangle = 20 kΩ	0.95		2.1	V
I/O voltage gain	VGVH	Rangle = 20 kΩ	25.5	28.5	31.5	dB
[Standby Pin]						
High-level input voltage	VSTH		2.5			V
Low-level input voltage	VSTL				0.4	V
Input current	ISTIN	VSTBY = 3 V		25	40	µA
Leakage current	ISTLK	VSTBY = 0 V			–30	µA
[FRC Pin]						
High-level input voltage	VFRCH		2.5			V
Low-level input voltage	VFRCL				0.4	V
Input current	IFRCIN	VFRC = 3 V		20	30	µA
Leakage current	IFRCLK	VFRC = 0 V			–30	µA
[VH]						
Hall supply voltage	VHALL	IH = 5 mA, VH (+) – VH (–)	0.85	0.95	1.05	V
Minus (–) pin voltage	VH (–)	IH = 5 mA	0.81	0.88	0.95	V

*: Design target value parameters are not tested.

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Note 1. The standard for the overlap amount parameter is to report the measured value without change.

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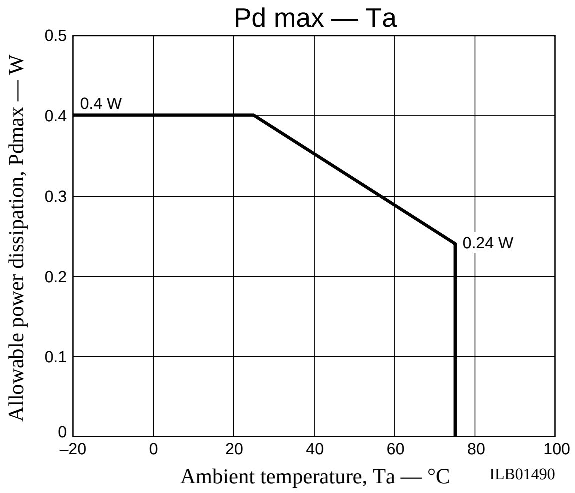
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[FG Comparator]						
Input hysteresis width 1	VFGHYS1			+10		mV
Input hysteresis width 2	VFGHYS2			–10		mV
Low-level output voltage	VFGOL	When the sink current is 0.5 mA		0.2	0.4	V
High-level output voltage	VFGOH	Pulled up through 10 kΩ internally	$V_{CC}1 - 0.5$			V
Allowable output current	IFGOL				2	mA
[Lock Pin]						
High-level voltage	VLOH		2.5			V
Low-level voltage	VLOL				0.4	V
Input current	VLOIN	VLOCK = 3 V		25		µA
Leakage current	VLOLK	VLOCK = 0 V			–30	µA
[TSD]						
Thermal shutdown circuit (TSD) operating temperature	T-TSD	Design target value*		180		°C
TSD temperature hysteresis	ΔTSD	Design target value*		20		°C

*: Design target value parameters are not tested.



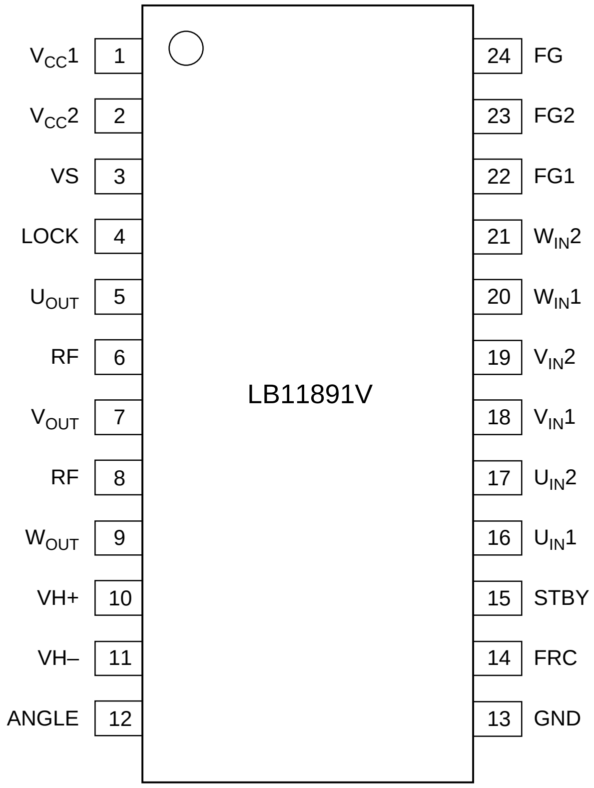
Truth Table

	Source → Sink	Hall inputs			FRC	LOCK
		U	V	W		
1	V → W	H	H	L	H	L
	W → V				L	
	V → U				H	H
	U → V				L	
2	U → W	H	L	L	H	L
	W → U				L	
	V → W				H	H
	W → V				L	
3	U → V	H	L	H	H	L
	V → U				L	
	U → W				H	H
	W → U				L	
4	W → V	L	L	H	H	L
	V → W				L	
	U → V				H	H
	V → U				L	
5	W → U	L	H	H	H	L
	U → W				L	
	W → V				H	H
	V → W				L	
6	V → U	L	H	L	H	L
	U → V				L	
	W → U				H	H
	U → W				L	

Note: The “H” entry in the FRC and LOCK columns indicates a voltage of 2.50 V or higher, and the “L” entry indicates a voltage of 0.4 V or lower. (When $V_{CC}1$ is 3 V)

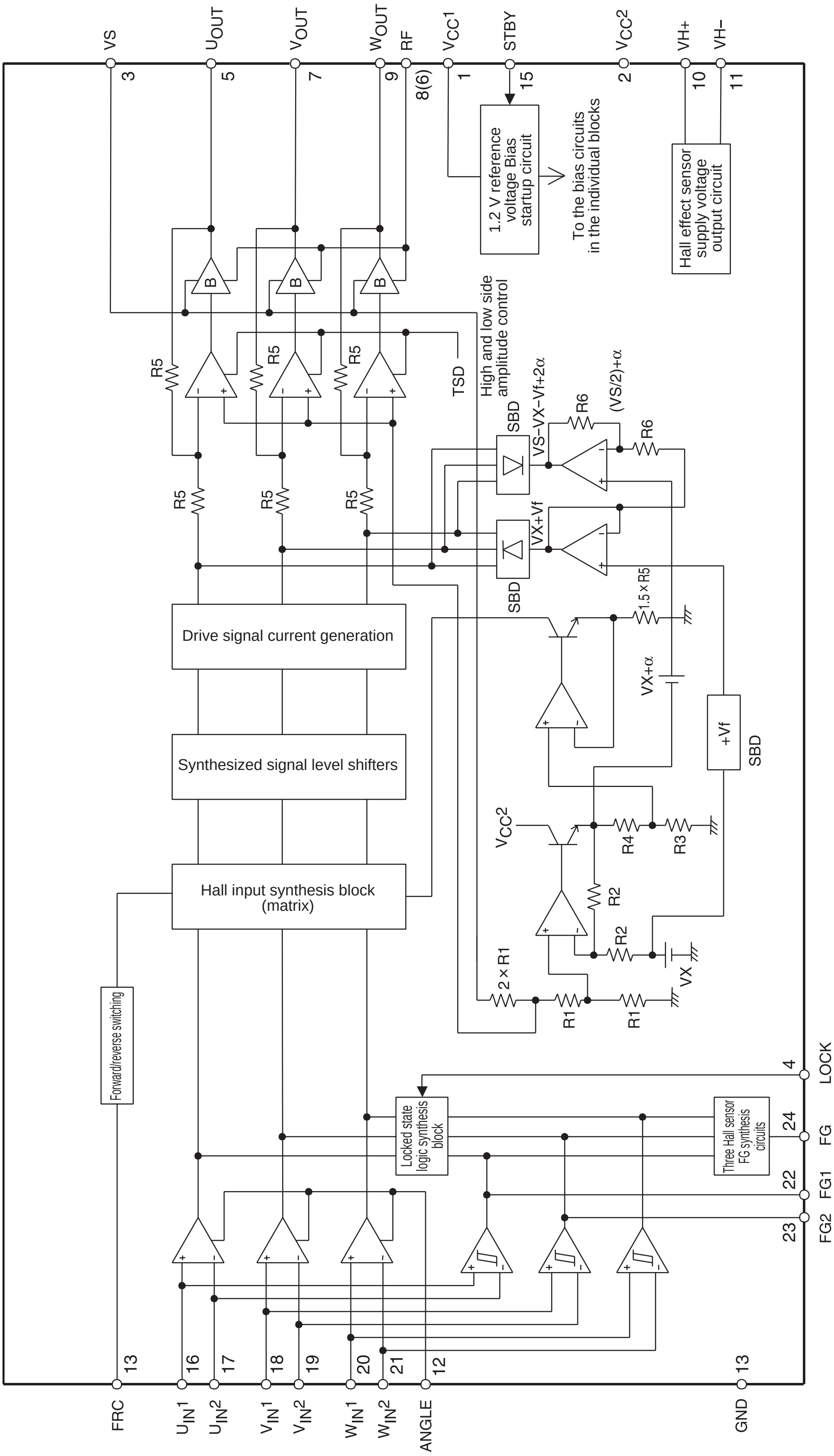
Note: For the Hall sensor inputs, the input “H” state is a state where the + input is at least 0.02 V higher than the - input, and the input “L” state is a state where the + input is at least 0.02 V lower than the – input.

Pin Assignments

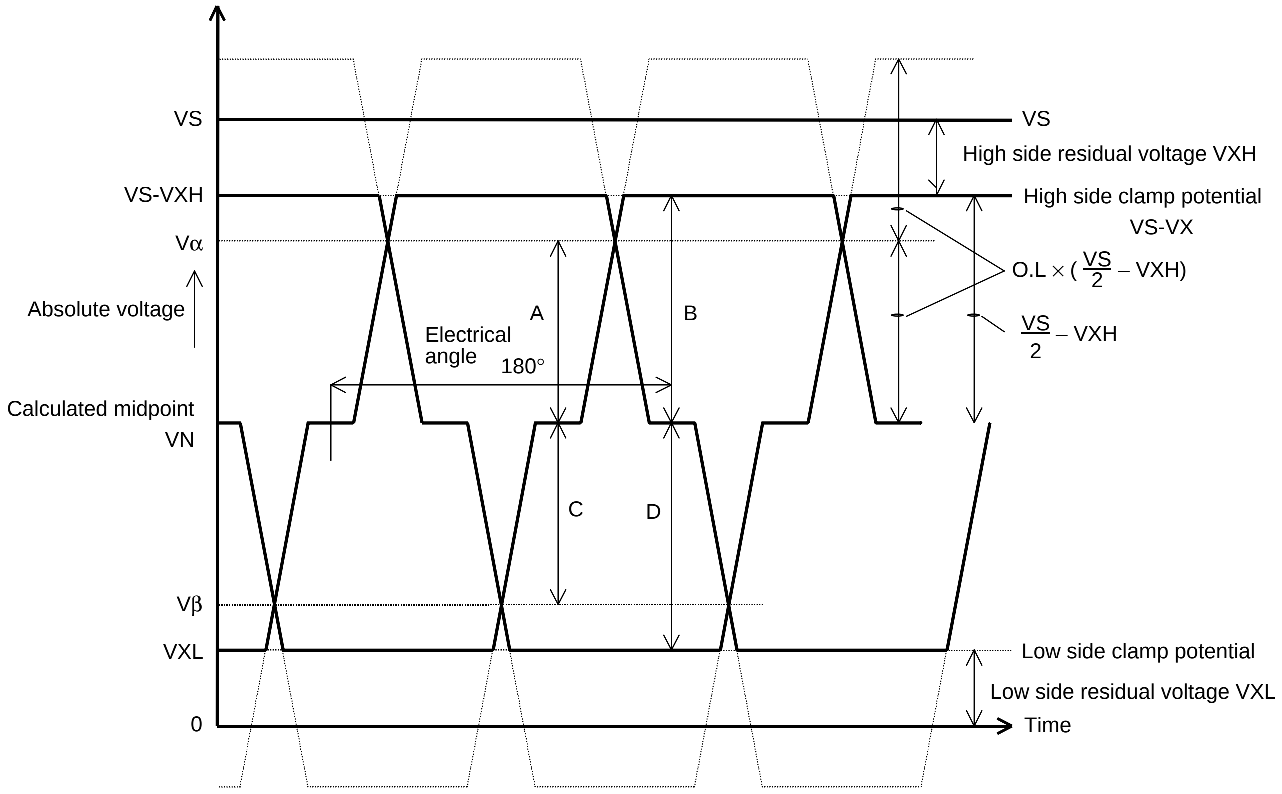


Top view

Block Diagram



Overlap Creation and Calculations



Overlap Creation

For the voltages generated in the control block, if the midpoint is taken as the reference, one side will be $2 \times \text{O.L.} \times \left(\frac{1}{2}\text{VS} - \text{VX}\right)$.

Therefore, the waveform crossover will be $\text{O.L.} \times \left(\frac{1}{2}\text{VS} - \text{VX}\right)$ from the midpoint.

Since that waveform is clamped at $\left(\frac{1}{2}\text{VS} - \text{VX}\right)$ referenced to the midpoint,

the overlap will be: $\frac{A}{B} \times 100 = \text{O.L.} \times 100$ [%] .

Overlap Calculation

(1) High side overlap

The calculated midpoint is $\text{VN} = \frac{(\text{VS} - \text{VXH} - \text{VXL})}{2} + \text{VXL} = \frac{\text{VS} - \text{VXH} - \text{VXL}}{2}$

Since A = α – VN and B = VS – VXH – VN, the high side overlap can be calculated as follows.

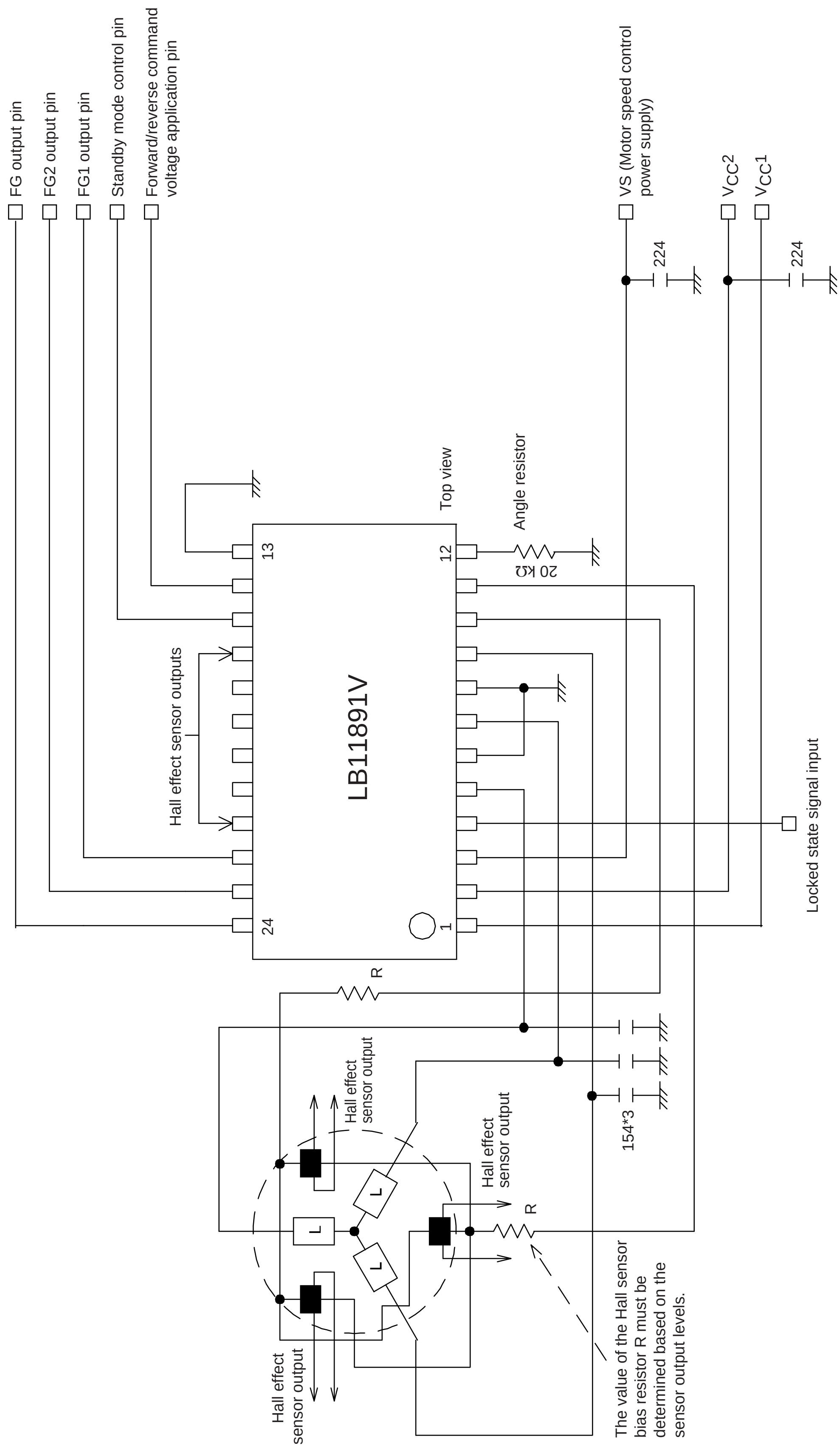
$$\text{Overlap} = \frac{A}{B} = \frac{\text{V}\alpha - ((\text{VS} - \text{VXH} + \text{VXL})/2)}{\text{VS} - \text{VXH} - ((\text{VS} - \text{VXH} + \text{VXL})/2)} \times 100 = \frac{2\text{V}\alpha - ((\text{VS} - \text{VXH}) - \text{VXL})}{(\text{VS} - \text{VXH} - \text{VXL})} \times 100 \ [\%] .$$

(2) Low side overlap

Since C = VN – Vβ and D = VN – VXL, the low side overlap can be calculated as follows.

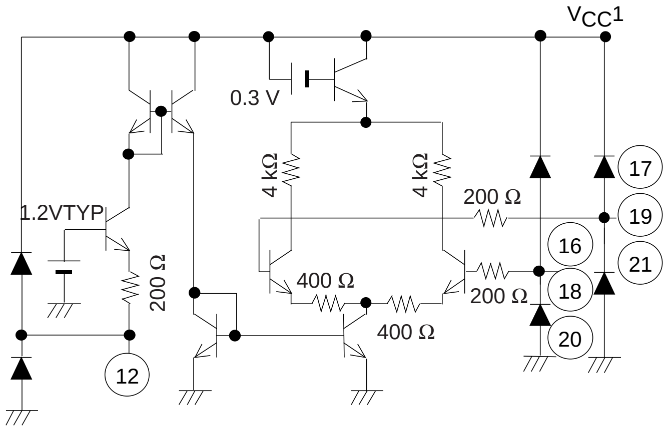
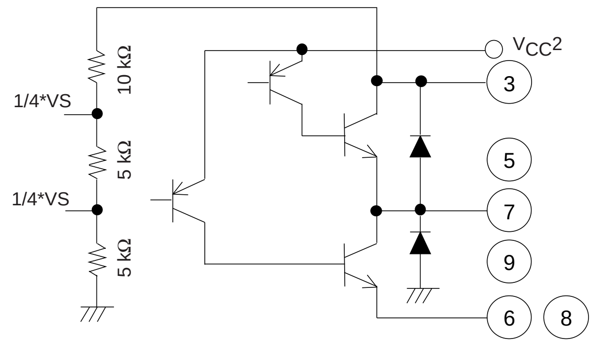
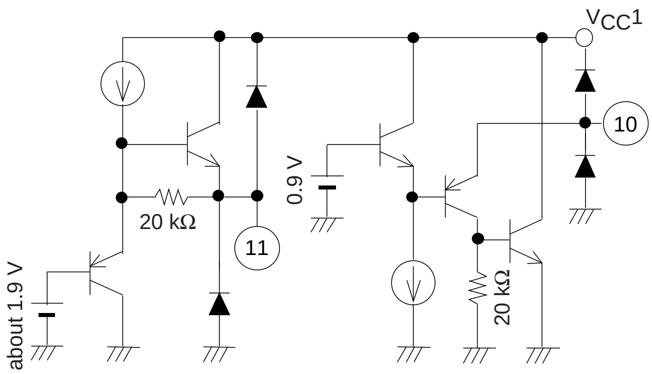
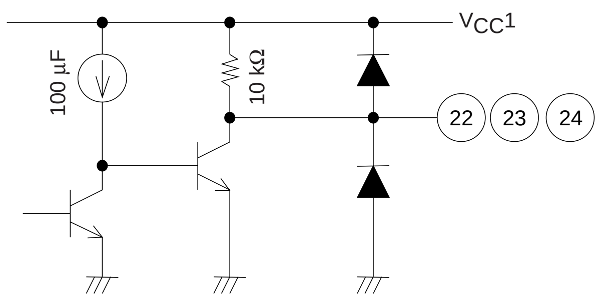
$$\text{Overlap} = \frac{C}{D} = \frac{((\text{VS} - \text{VXH} + \text{VXL})/2) - \text{V}\beta}{((\text{VS} - \text{VXH} + \text{VXL})/2) - \text{VXL}} \times 100 = \frac{(\text{VS} - \text{VXH}) + \text{VXL} - 2\text{V}\beta}{(\text{VS} - \text{VXH}) - \text{VXL}} \times 100 \ [\%] .$$

Application Circuit Example



Note: The component values shown in this application circuit example are examples only, and no guarantees, explicit or implicit, are made regarding their characteristics.

Pin Functions and Equivalent Circuits

Pin No.	Symbol	Voltage	Function	Equivalent circuit
16 17 18 19 20 21	$U_{IN}1$ $U_{IN}2$ $V_{IN}1$ $V_{IN}2$ $W_{IN}1$ $W_{IN}2$	0 to $V_{CC}1$	Capstan motor driver U, V, and W phase Hall effect sensor inputs. The logic high state indicates that IN1 > IN2.	
12	ANGLE		Controls the gain from the Hall inputs to the output. The gain is controlled by the resistor inserted between this pin and ground.	
3	VS	0 to $V_{CC}2$	Power supply that determines the amplitude of the output to the capstan motor. This voltage must be lower than $V_{CC}2$.	
5 7 9 6, 8	U-OUT V-OUT W-OUT Rf		Capstan motor driver U, V, and W phase outputs.	
10	VH+		The Hall effect sensor element bias voltage supply. A voltage of 0.85 V (typical) is generated between the VH+ and VH– pins. (When IH is 5 mA)	
11	VH–			
22	FG1		Comparator output for $U_{IN}1$ and $U_{IN}2$.	
23	FG2		Comparator output for $V_{IN}1$ and $V_{IN}2$.	
24	FG		Three-phase synthesized output for the U, V, and W phase comparator output.	

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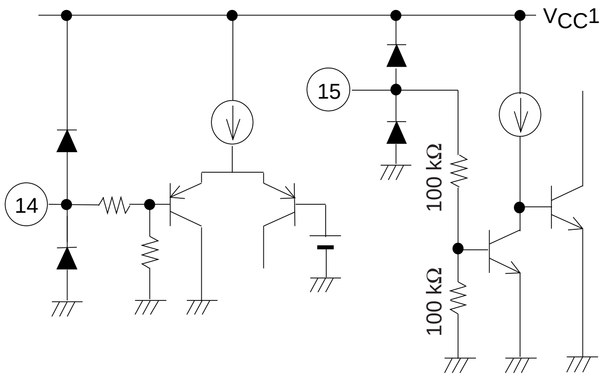
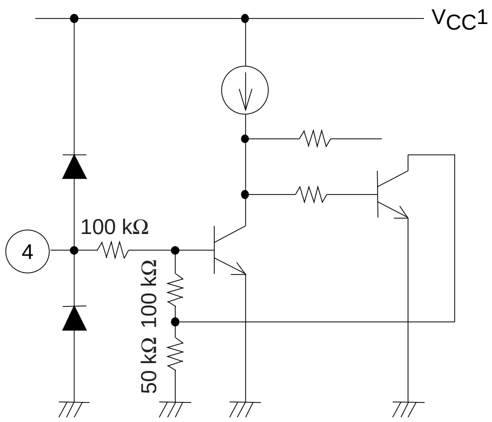
Pin No.	Symbol	Voltage	Function	Equivalent circuit
14	FRC	0 to $V_{CC}1$	Capstan motor forward/reverse control. This pin determines the direction (forward or reverse) of the capstan motor. (This input has hysteresis characteristics.)	
15	STBY		Selects the bias supply for all the capstan motor circuits other than the FG comparator. Setting this pin low cuts off the bias supply. Thus it functions as the standby mode control pin.	
4	LOCK	0 to $V_{CC}1$	The output phase is locked by applying a low to high trigger voltage (edge) to this pin. This prevents the motor from turning due to the application of an external load in the motor stopped state.	
2	$V_{CC}2$	3.5 to 6 V	Power supply used for the source side pre-driver voltage and the coil waveform detection comparator.	
1	$V_{CC}1$	2.7 to 6 V	Power supply used for voltages other than the motor voltage, the source side pre-driver voltage, and the coil waveform detection comparator.	
13	GND		Ground used for all systems other than the output system.	

This catalog provides information as of January, 2004. Specifications and information herein are subject to change without notice.