

# SANYO Semiconductors DATA SHEET

An ON Semiconductor Company

## LB11988V — Monolithic Digital IC Fan Motor Driver

#### **Overview**

The LB11988V is a motor driver IC optimal for driving the DC fan motors.

#### Features

- 3-Phase full-wave current-linear drive system.
- Current limiter circuit built in.
- Output stage upper/lower over-saturation prevention circuit built in.
- Forward/backward rotation direction setting circuit built in.
- FG amplifier built in.
- Thermal shutdown circuit built in.

#### Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>CC</sub> max		24	V
	VS max		24	V
Maximum output current	I <sub>O</sub> max		1.3	А
Allowable power dissipation	Pd max	Independent IC	0.5	W
Operating temperature range	Topr		-30 to +75	°C
Storage temperature range	Tstg		-55 to +150	°C

#### Allowable Operating Range at $Ta = 25^{\circ}C$

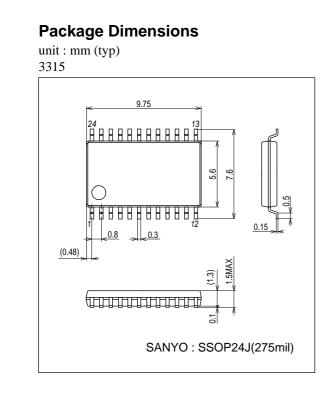
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	VS		5 to 22	N
	V <sub>CC</sub>		7 to 22	v
Hall input amplitude	VHALL	Between hall inputs	±30 to ±80	mVo-p

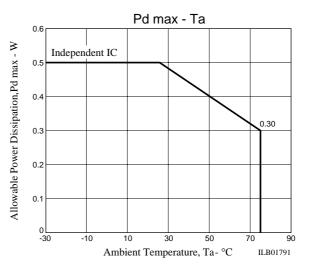
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## **Electrical Characteristics** at Ta = 25 °C, $V_{CC} = 12V$ , VS = 12V

Deveryor	Symbol	O an dition a	Ratings			
Parameter		Conditions	min	typ	max	unit
V <sub>CC</sub> supply current	ICC	R <sub>L</sub> = 560Ω (Y)		15	24	mA
Output						
Output saturation voltage	V <sub>O</sub> sat1	$I_O = 500$ mA, Rf = 0.5 $\Omega$ , Sink+Source (with saturation prevention)		2.1	2.6	Ň
	V <sub>O</sub> sat2	$I_{O}$ = 1.0A, Rf = 0 $\Omega$ , Sink+Source (with saturation prevention)		2.6	3.5	V
Output leakage current	lOleak				1.0	mA
Hall amplifier						
Input offset voltage	Voff(HALL)		-6		+6	mV
Input bias current	lb(HALL)	V <sub>IN</sub> , W <sub>IN</sub>		1	3	μA
Common-mode input voltage	Vcm(HALL)		3		V <sub>CC</sub> -3	V
FR	•					
Threshold voltage	VFRTH		4		8	V
Input bias current	lb(FR)		-5			μA
Current limit						
LIM pin current limit level	ILIM	Rf = $0.5\Omega$ , Hall input logic fixed (U, V, W = H, H, L)		1		A
Saturation						
Saturation prevention circuit lower set voltage	V <sub>O</sub> sat(DET)	$R_L = 560\Omega$ (Y), $Rf = 0.5\Omega$ Voltage between each OUT and RF		0.28		V
FG Amplifier						
Output "High" voltage	Vfgoh(SH)		11.8			
Output "Low" voltage	Vfgol(SH)				0.3	V
Hysteresis width	Vhys			23		mV
TSD operating temperature	T-TSD	Design target value*		170		°C

\*: T-TSD is not measured because it stands for design target.



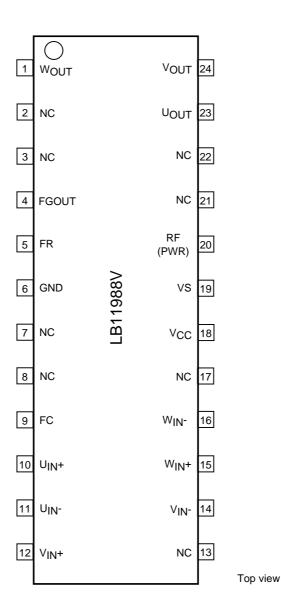


### **Truth Table and Control Function**

	Source $\rightarrow$ Sink	Hall Input			FR
		U	V	W	ГК
1	$V \rightarrow W$	н			Н
1	$W\toV$	п	н	L	L
0	$U\toW$		L	L	Н
2	$W\toU$	Н			L
0	$U\toV$		L	н	Н
3	$V\toU$	н			L
4	$W\toV$	L	L	н	н
4	$V\toW$	L			L
-	$W \rightarrow U$		Н	н	Н
5	$U\toW$	L			L
6	$V\toU$	L	н	L	Н
0	$U\toV$	L		L	L

- Note: "H" in the FR column represents a voltage of 8V or more. "L" represents a voltage of 4V or less. (At V<sub>CC</sub>=12V)
- Note: "H" under the Hall Input columns represents a state in which "+" has a potential which is higher by 0.01V or more than that of the "-" phase inputs. Conversely "L" represents a state in which "+" has a potential which is lower by 0.01V or more than that of the "-" phase inputs.
- Note: Since a 180° energized system is used as a drive system, other phases than the sink and source are not OFF.

## **Pin Assignment**



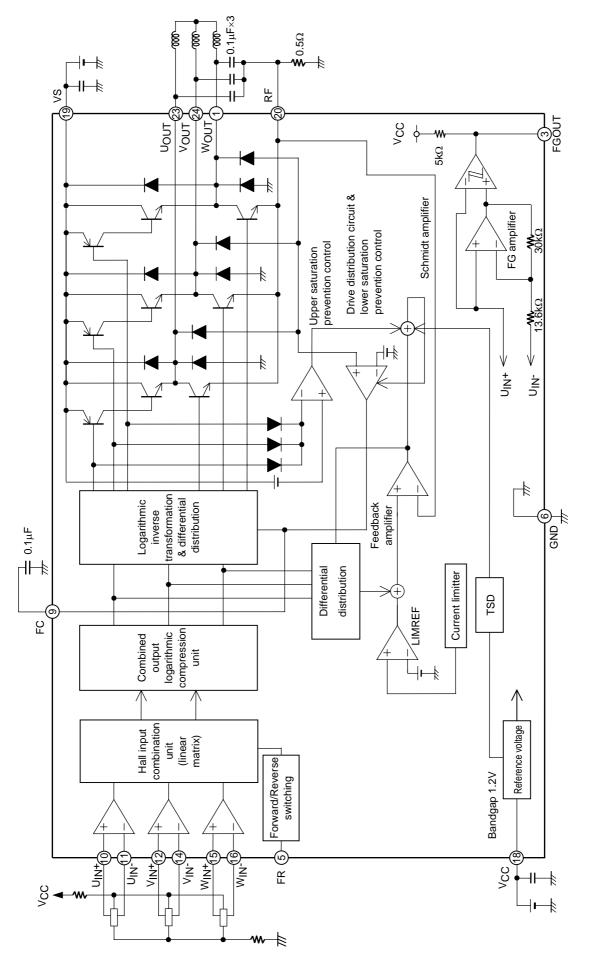
## **Pin Functions**

Pin Name	Pin No.	Pin Functions	Input/Output Equivalent Circuit
GND	6	GND for others than the output transistor. Minimum potential of output transistor is at RF pin.	
U <sub>IN</sub> +, U <sub>IN</sub> -	10,11	U-phase Hall device input pin; logic "H" presents IN+>IN-	Each (+) input 10 Each (-) input 11 Each (-) input
V <sub>IN</sub> +, V <sub>IN</sub> -	12,14	V-phase Hall device input pin; logic "H" presents IN+>IN-	$\begin{array}{c} 12 \\ 15 \\ 15 \\ 200\Omega \end{array}$
W <sub>IN</sub> +,W <sub>IN</sub> -	15,16	W-phase Hall device input pin; logic "H" presents IN+>IN-	
U <sub>OUT</sub>	23	U-phase output pin.	
VOUT	24	V-phase output pin.	
WOUT	1	W-phase output pin. (Built-in spark killer diode)	(19) VS VCC
RF	20	Output current detection pin. Connecting Rf between this pin and GND activates current limiting circuit. Then the lower over-saturation prevention circuit is activated in accordance with this pin voltage. Since the over-saturation prevention level is set with this voltage, the lower over-saturation prevention effect may deteriorate in the high current range if the Rf value is reduced to an extremely low level.	Each OUT 23(24) 1 Lower oversaturation prevention circuit block
VS	19	Power supply pin for supplying power to output section in IC.	
FR	5	Forward/Reverse switching pin.	FR 5
FC	9	Frequency characteristics compensation pin for over-saturation prevention circuit loop.	vcc giget g g g g g g g g g g g g g g g g g g

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Pin Name	Pin No.	Pin Functions	Input/Output Equivalent Circuit
V <sub>CC</sub>	18	Power supply pin for supplying power to all circuits expect output section in IC; this voltage must be stabilized so as to eliminate ripple and noise.	
FGOUT	3	FG amplifier output pin. Resistive load provided internally.	VCC SHOL THE SHOL THE SHOL THE SHOL THE SHOL SHOL THE SHOL SH

**Block Diagram** 



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