Ordering number : EN4355

Monolithic Digital IC

No. 4355

LB1817M

FDD Spindle Motor Driver

Overview

The LB1817M is the ideal IC for applications requiring a 5 V, low-profile FDD spindle motor driver.

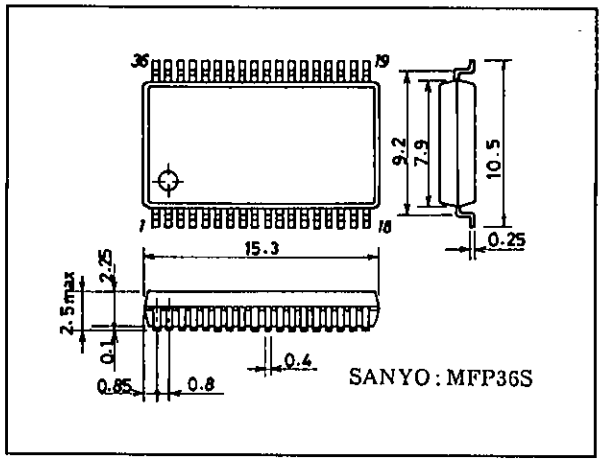
Functions and Features

- Three phase total wave linear driver (external PNP)
- Low saturation voltage
- On-chip digital speed control
- Start/stop circuit ("L" level active)
- Rotation speed switching
- Current limiter circuit
- On-chip index processing circuit
- Index timing supports adjustments using VR
- AGC circuit
- Temperature protection circuit

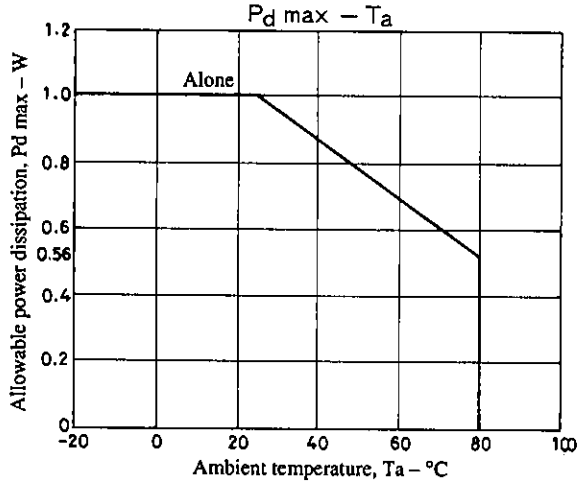
Package Dimensions

unit : mm

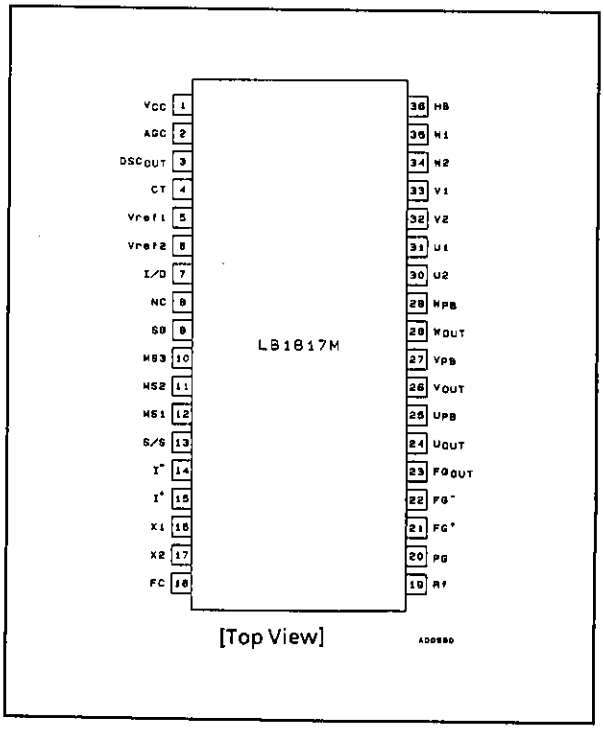
3129-MFP36S



Allowable power dissipation vs. ambient temperature



Pin Assignment



Specifications

Absolute Maximum Ratings at Ta = 25°C

				unit
Maximum supply voltage	V_{CC} max		7.0	V
Maximum output current	I_{CC} max1	t≤0.5sec	1.5	A
Steady maximum output current	I_O max2		1.0	A
Allowable power dissipation	Pd max	IC alone	1	W
Operating temperature	**Topr**		–20 to +80	°C
Storage temperature range	Tstg		–40 to +150	°C

Allowable Operating Conditions at Ta = 25°C

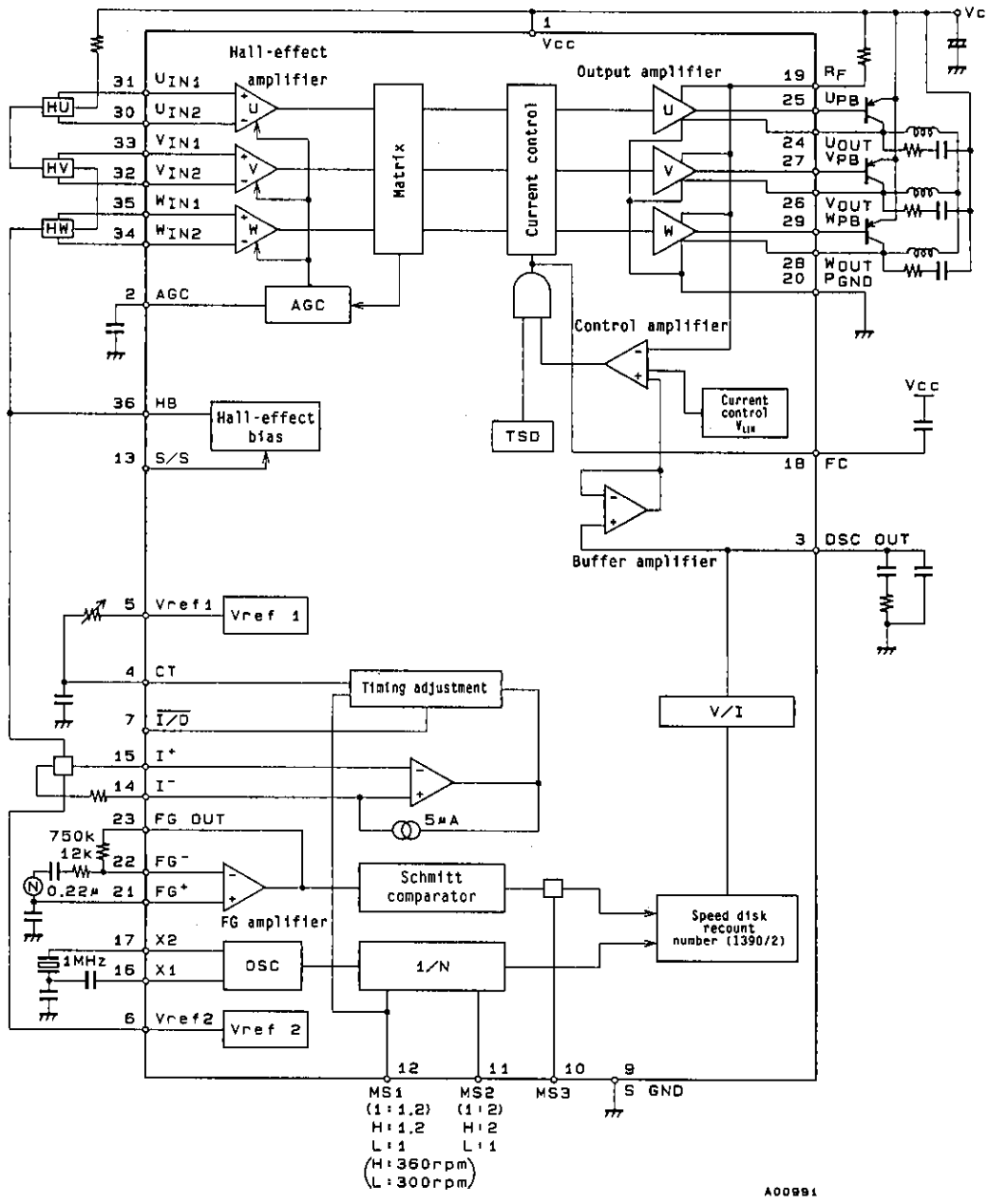
			unit
Supply voltage	V_{CC}	4.2 to 6.5	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 5V

			min	typ	max	unit	note
Current consumption	I_{CCO}	S/S = 5V (Standby)		70	100	μA	
	I_{CC}	S/S = 0V (Steady)		25	35	mA	
MS1 bias current	I_{MS1}	V_{MS1} = 5V		180	270	μA	
MS1 "L" level input voltage	V_{MS1L}		0		0.8	V	
MS1 "H" level input voltage	V_{MS1H}		2.0		V_{CC}	V	
MS2 bias current	I_{MS2}	V_{MS2} = 5V		90	135	μA	
MS2 "L" level input voltage	V_{MS2L}		0		0.8	V	
MS2 "H" level input voltage	V_{MS2H}		2.0		V_{CC}	V	
MS3 bias current	I_{MS3}	V_{MS3} = 5V		90	135	μA	
MS3 "L" level input voltage	V_{MS3L}		0		0.8	V	
MS3 "H" level input voltage	V_{MS3H}		2.0		V_{CC}	V	
S/S bias current	$I_{S/S}$				20	μA	
S/S "L" level voltage	$V_{S/SL}$		0		0.8	V	
S/S "H" level voltage	$V_{S/SH}$		2.0		V_{CC}	V	
Hall-effect bias amplifier input current	I_{HB}				15	μA	
In-phase input voltage range	Vh		2.0		V_{CC} – 0.7	V	
Differential input voltage range	Vdif		50		200	mVp-p	
Input offset voltage	Vho				±10	mV	*
Hall-effect output voltage	V_H	I_H = 5mA	0.5	0.8	1.1	V	
Leak current	I_{HL}	S/S = 5V			±10	μA	
Output saturation voltage	Vsat	I_O = 0.8A		0.45	0.64	V	
Output leak current	I_{OL}				1.0	mA	
Current limiter	I_{lim}	R_F = 3kΩ, ROUT = 100Ω	6.3	7.5	8.7	mA	
Control amplifier voltage gain	G_C		–7.5	–5.5	–3.5	dB	
Voltage gain phase differential	$\triangle G_C$				±1	dB	
V/I conversion source current	I+		19	28	37	μA	
V/I conversion sink current	I–		–19	–28	–37	μA	
V/I conversion current ratio	I+/I–		0.8	1.0	1.2		
DSC buffer input current	I_{DSC}				1.0	μA	
FG amplifier input voltage	V_{FG}	f_{FG} = 300Hz	2		20	mVp-p	
FG amplifier voltage gain	G_{FG}	Open loop		60		dB	*
FG amplifier input offset	V_{FGO}				±10	mV	*
FG amplifier internal reference voltage	V_{FGB}		2.2	2.5	2.8	V	
FG schmitt hysteresis width	△Vsh1	"H" → "L"		25		mV	*
	△Vsh2	"L" → "H"		25		mV	*
Speed disk recount number	N			1390/2			
Disk operation frequency	F_D				1.1	MHz	*
Oscillation range	F_{OSC}				1.1	MHz	*
Oscillation frequency error	$\triangle F_{OSC}$				±0.2	%	
Index output "L" level voltage	V_{IDL}	I_O = 2mA			0.4	V	
Index output leak current	I_{IDL}				±10	μA	
Index amplifier in-phase input voltage range	V_I		0.2		V_{CC} –0.7	V	
Index amplifier differential input voltage range	V_{DIF}	Hysteresis width<25mA	25		100	mV	
Index amplifier hysteresis setting current	I_{HYS}		2.9	4.2	5.5	μA	
Timing adjustment "H" level	V_{TH}	MS1 = L	1.15	1.26	1.35	V	
Timing adjustment "L" level	V_{TL}	MS1 = L	0.4	0.52	0.6	V	
Timing adjustment ratio	T_{HL}	V_{TH} (MS1 = L)/V_{TH} (MS1 = H)		1.148			
Reference voltage	V_{REF1}		2.20	2.50	2.80	V	
	V_{REF2}		1.85	2.15	2.45	V	
Excessive heat protected operating temperature	TSD		150	180		°C	*
Hysteresis width	△TSD			10		°C	*

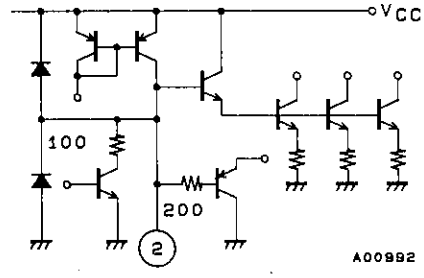
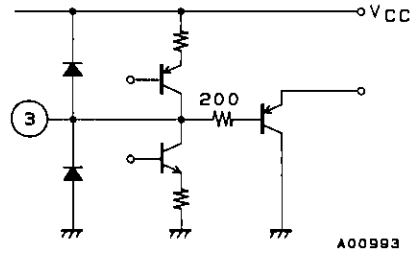
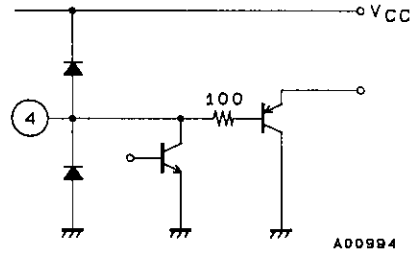
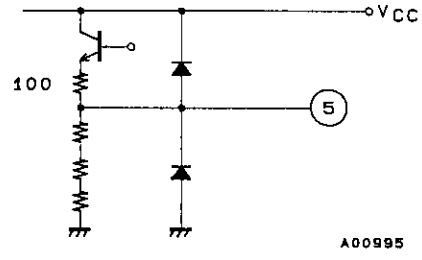
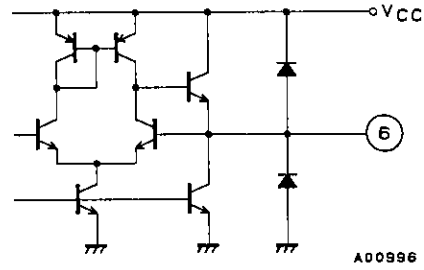
Note: Marked values (*) are guaranteed by the design itself and therefore do not require measurement.

Block Diagram



Unit (resistance: Ω, capacitance: F)

Pin Description

Pin Number	Pin Symbol	Pin Voltage	Equivalent Circuit	Pin Description
1	V_{CC}			• Power supply voltage pin. Voltage must be stable and free of ripple noise interference.
2	AGC			• AGC pin. Controls hall-effect amplifier gain in response to hall-effect input frequency. External capacitor installation.
3	DSC out			• Speed discriminator pin.
4	CT			• Timing adjustment pin. External CR for delay time constant connected.
5	Vref1	2.5V typ		• Vref1 pin. Used as external CR power supply for index timing adjustment applications.
6	Vref2	2.15V typ		• Vref2 pin. Used for sensor bias for external index applications.

Unit (resistance: Ω)

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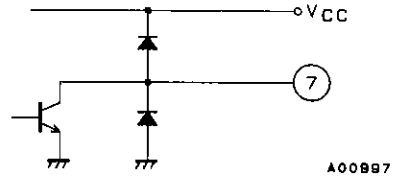
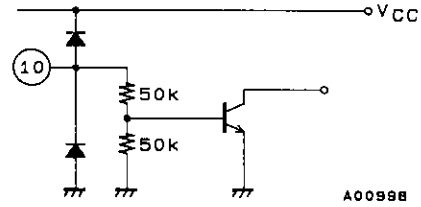
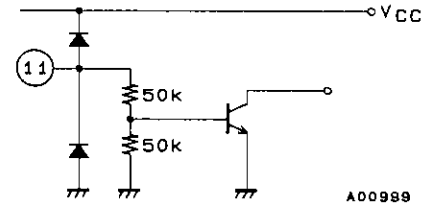
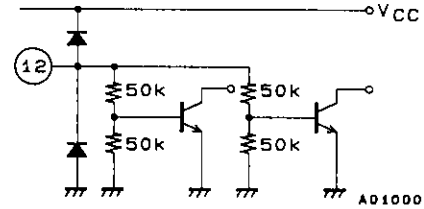
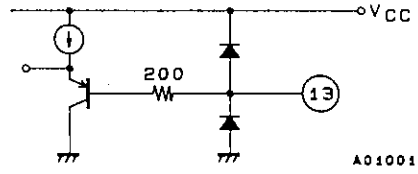
Pin Number	Pin Symbol	Pin Voltage	Equivalent Circuit	Pin Description
7	I/D			• Index pulse output pin.
8	NC			• No connection.
9	GND			• Ground pin for signal system. Grounded as with pin 20.
10	MS3	H: 2.0V min L: 0.8V max		• FG changeover pin. When operating at an "H" level, FG sets to a through state. An "L" level results in 1-step division of FG.
11	MS2	H: 2.0V min L: 0.8V max		• CLK changeover pin. When operating at an "H" level, CLK sets to a through state. An "L" level results in 1-step division of CLK.
12	MS1	H: 2.0V min L: 0.8V max		• Rotation speed changeover pin. An "H" level sets rotation speed to 360 rpm. An "L" level sets rotation speed to 300 rpm. For more details, refer to the rotation speed changeover table.
13	S/S	H: 2.0V min L: 0.8V max		• Start/stop changeover pin. "L" level active.

Unit (resistance: Ω)

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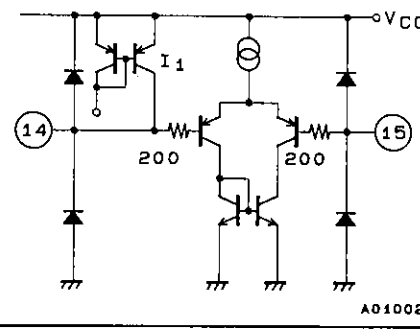
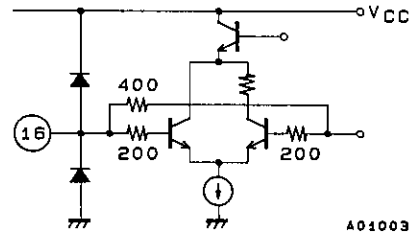
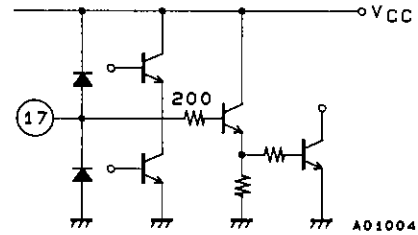
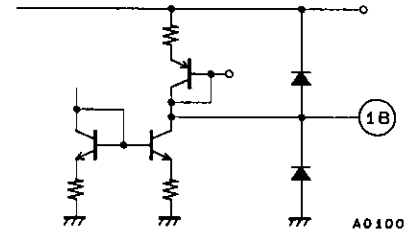
Pin Number	Pin Symbol	Pin Voltage	Equivalent Circuit	Pin Description
14 15	I− I+			• External index negative input pin. • External index positive input pin. When the I− pin is at an "H" level, I1 operates with the fixed current; at an "L" level, I1 does not flow. Hysteresis width is determined by the resistor attached externally to the I− pin.
16	X1			• Reference clock generating pin.
17	X2			
18	FC			• Frequency characteristics revision pin By installing a capacitor between this pin and V_{CC}, close-loop oscillation for the current control system halts.
19	RF			• Output current detection pin. By installing an R_f resistor between this pin and V_{CC}, output current is detected as voltage. Voltage detection at this pin activates the current limiter. Detection level is approximately 1/50 of output current.
20	PGND			• Output transistor grounding pin. Grounded as with pin 9.

Unit (resistance: Ω)

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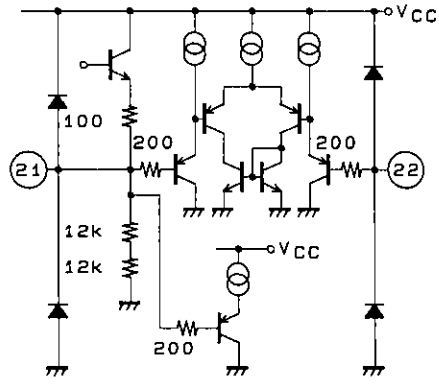
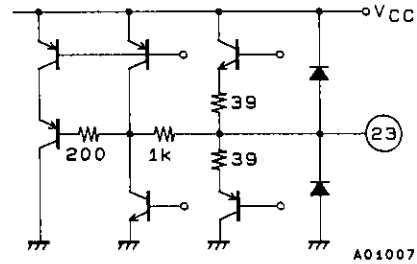
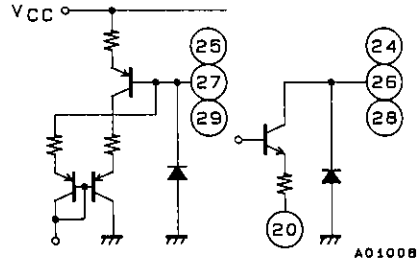
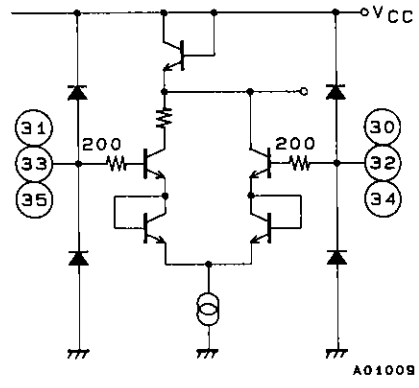
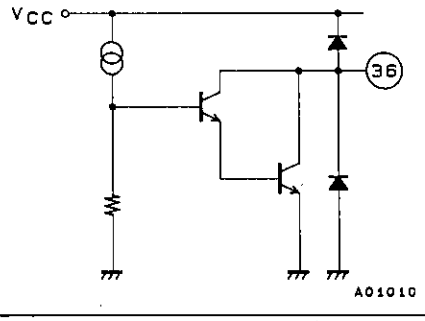
Unit (resistance: Ω)

Pin Number	Pin Symbol	Pin Voltage	Equivalent Circuit	Pin Description
21 22	FG+ FG-	2.5V typ		• FG amplifier positive pin. • FG amplifier negative pin.
23	FG out			• FG amplifier output pin.
24 25 26 27 28 29	U_{OUT} U_{PB} V_{OUT} V_{PB} W_{OUT} W_{PB}			• U-phase output pin. • Base connection pin for U-phase external PNP. • V-phase output pin. • Base connection pin for V-phase external PNP. • W-phase output pin. • Base connection pin for W-phase external PNP.
30 31 32 33 34 35	UIN2 UIN1 VIN2 VIN1 WIN2 WIN1			• U-phase hall-effect input pin. $U_{IN1} > U_{IN2}$ is established when logic is at an "H" level. • V-phase hall-effect input pin. $V_{IN1} > V_{IN2}$ is established when logic is at an "H" level. • W-phase hall-effect input pin. $W_{IN1} > W_{IN2}$ is established when logic is at an "H" level.
36	HB			• Hall-effect bias applied to minus-side pin. When stopped, switches open and hall-effect bias severs.

Truth Table

	Source → Sink	Hall-Effect Input		
		U	V	W
1	V-phase → W-phase	H	H	L
2	V-phase → U-phase	L	H	L
3	W-phase → U-phase	L	H	H
4	W-phase → V-phase	L	L	H
5	U-phase → V-phase	H	L	H
6	U-phase → W-phase	H	L	L

When an "H" level exists for hall-effect input,

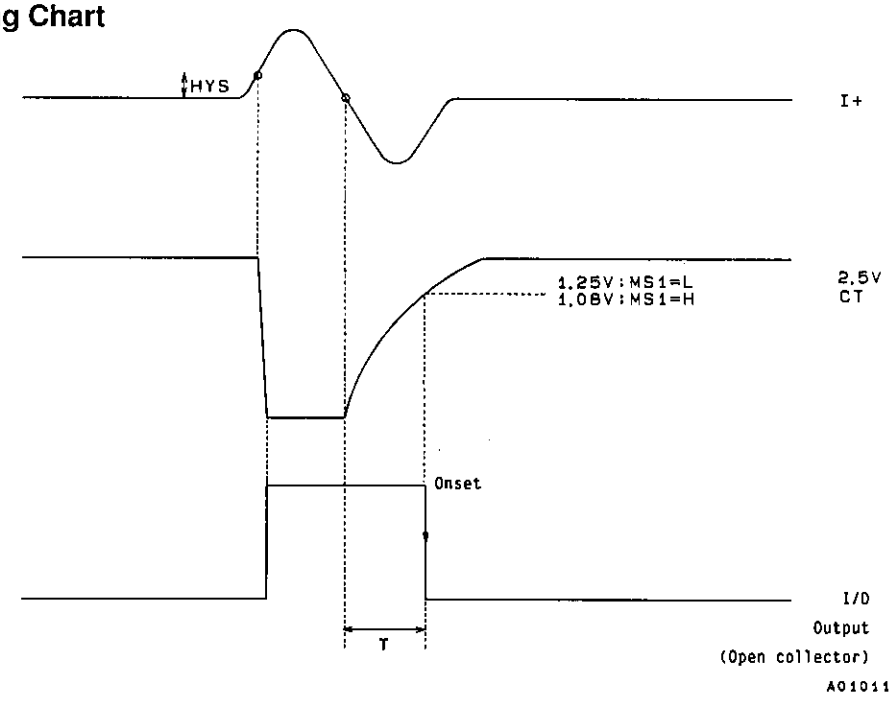
$U_{IN1} > U_{IN2}$
$V_{IN1} > V_{IN2}$
$W_{IN1} > W_{IN2}$

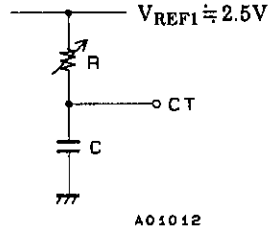
Rotation Speed Changeover Table

f_{OSC} = 1MHz

MS1	H	L	H	L	H	L	H	L
MS2	H		L		H		L	
MS3	H		L		L		H	
f_{FG} [Hz]	720	600	720	600	1440	1200	360	300

Index and Timing Chart





$T \fallingdotseq 0.693CR \cdots MS1 = L$
$T \fallingdotseq 0.836CR \cdots MS1 = H$

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