Ordering number : EN5653

Monolithic Digital IC

LB1916

CD-ROM Spindle Motor Driver

Overview

The LB1916 is a 3-phase motor driver that is optimal for driving CD-ROM spindle motors.

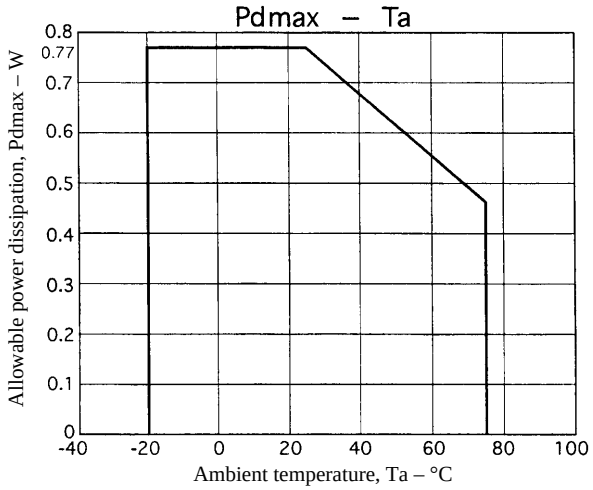
Functions and Features

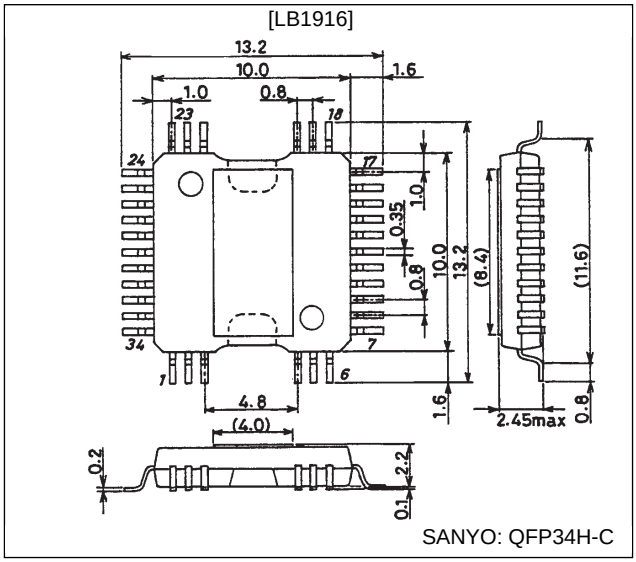
- 3-phase brushless motor driver
- 120° voltage linear drive control
- V-type input used for the control voltage
- Control gain switching supported
- Pins for system control and control of acceleration and deceleration provided.
- Start/stop pin provided.
- Hall bias circuit

Package Dimensions

unit: mm

3219-QFP34H-C





Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC}1$ max		14	V
	$V_{CC}2$ max		7.0	V
Output voltage	V_OU, V, W		13	V
Output current	I_{OUT}		1.0	A
Allowable power dissipation	Pd max	Independent IC	0.77	W
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–55 to +150	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{CC}1$		5 to 12.5	V
	$V_{CC}2$	$V_{CC}1 \geq V_{CC}2$	4.3 to 6.5	V
V_{CREF} input voltage	V_{CREF}		$V_{CC}2/2 \pm 1.0$	V

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Electrical Characteristics at Ta = 25°C, $V_{CC}1$ = 12 V, $V_{CC}2$ = 5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current drain	$I_{CC}1$	V_C = 2.5 V, V_{CREF} = 2.5 V, R_L = ∞, VS/S = 5 V, VRF = GND		17	30	mA
	$I_{CC}2$	V_C = 2.5 V, V_{CREF} = 2.5 V		7.5	10.5	mA
(I_{CC} for $V_{CC}1$)	$I_{CC}3$	V_C = 2.5 V, V_{CREF} = 2.5 V, R_L = ∞, VS/S = 0 V, VRF = GND		0.9	3	mA
[Drive Block]						
Output saturation voltage	V_O(sat)1	I_{OUT} = 0.4 A, sink + source		1.6	2.2	V
	V_O(sat)2	I_{OUT} = 0.8 A, sink + source		2.0	3.0	V
Output TRS sustainable voltage	V_O(sus)	I_{OUT} = 20 mA, *	14			V
Output center voltage	V_{OQ}	V_C = 2.5 V, V_{CREF} = 2.5 V	5.7	6.0	6.3	V
Hall amplifier input offset voltage	VH offset		–5		+5	mV
Hall amplifier input bias current	IH bias			1	5	µA
Hall amplifier common-mode input voltage range	VHch		1.3		2.2	V
Hall input/output voltage gain	VG_{HO}		38	41	44	dB
Control - output drive gain 1	$VG_{CO}1$	RZ1 = RZ2, GC1 = L, GC2 = L	23	26		dB
Control - output channel difference 1	$\Delta VG_{CO}1$	RZ1 = RZ2, GC1 = L, GC2 = L	–1.5		+1.5	dB
Control - output drive gain 2	$VG_{CO}2$	RZ1 = RZ2, GC1 = L, GC2 = H	29	32		dB
Control - output channel difference 2	$\Delta VG_{CO}2$	RZ1 = RZ2, GC1 = L, GC2 = H	–1.9		+1.9	dB
Input dead band voltage	V_{DZ}	RZ1 = RZ2, GC1 = L, GC2 = H V_O (voltage between out and OUT) = 0.1 V		±24	±50	mV
Input bias current 1	I_B SERVO	VC = 1.0 V			500	nA
S/S pin high-level voltage	VS/S H	Inputs are CMOS level, (See Note.) S/S pin Vth = V_{CC}2/2	4.0			V
S/S pin low-level voltage	VS/S L	Inputs are CMOS level, (See Note.) S/S pin Vth = V_{CC}2/2			1.0	V
Gain control 1 high-level voltage	V_{GC}1 H	Inputs are CMOS level, (See Note.) GC1 pin Vth = 2.0 V	4.0			V
Gain control 1 low-level voltage	V_{GC}1 L	Inputs are CMOS level, (See Note.) GC1 pin Vth = 2.0 V			1.0	V
Gain control 2 high-level voltage	V_{GC}2 H	Inputs are CMOS level, (See Note.) GC2 pin Vth = 2.0 V	4.0			V
Gain control 2 low-level voltage	V_{GC}2L	Inputs are CMOS level, (See Note.) GC2 pin Vth = 2.0 V			1.0	V
S/S pin input current	IS/S	Input voltage = 5 V		50	100	µA
Gain control 1 and 2 current	I_{GC}	Input voltage = 5 V		53	110	µA
Rotation output saturation voltage	V(sat)H.FG1, 2	I_O = –5 mA		0.24	0.5	V
	V(sus)H.FG1, 2	*			7	V
Hall bias voltage	VH±	I_O = 5 mA, R_H = 200 Ω	0.7	0.97	1.2	V
CTRL pin high-level voltage	VS/S H	CTRL1 and CTRL2 are common, Inputs are CMOS level, (See Note.) CTRL pin Vth = 2.5 V	4.0			V
CTRL pin low-level voltage	VS/S L	CTRL1 and CTRL2 are common, Inputs are CMOS level, (See Note.) CTRL pin Vth = 2.5 V			1.0	V
CTRL input pin	I_{CTRL}	Input voltage = 5 V		53	110	µA
Thermal shutdown operating voltage	TSD	*	150	180	210	°C
Thermal shutdown hysteresis	ΔTSD	*		15		°C

Note: Items marked with an asterisk are design target values and are not tested.

Hall Logic Truth Table

	Source → Sink	Hall input			Forward/reverse control
		U_{IN}	V_{IN}	W_{IN}	
1	W → V	H	H	L	Forward
	V → W				Reverse
2	W → U	H	L	L	Forward
	U → W				Reverse
3	V → W	L	L	H	Forward
	W → V				Reverse
4	U → V	L	H	L	Forward
	V→> U				Reverse
5	V → U	H	L	H	Forward
	U → V				Reverse
6	U → W	L	H	H	Forward
	W → U				Reverse

An input “H” state is defined as $U_{IN}1 > U_{IN}2$, $V_{IN}1 > V_{IN}2$, and the potential difference is at least 0.2 V.

When $V_C > V_{CREF}$: Forward rotation

When $V_C < V_{CREF}$: Reverse rotation

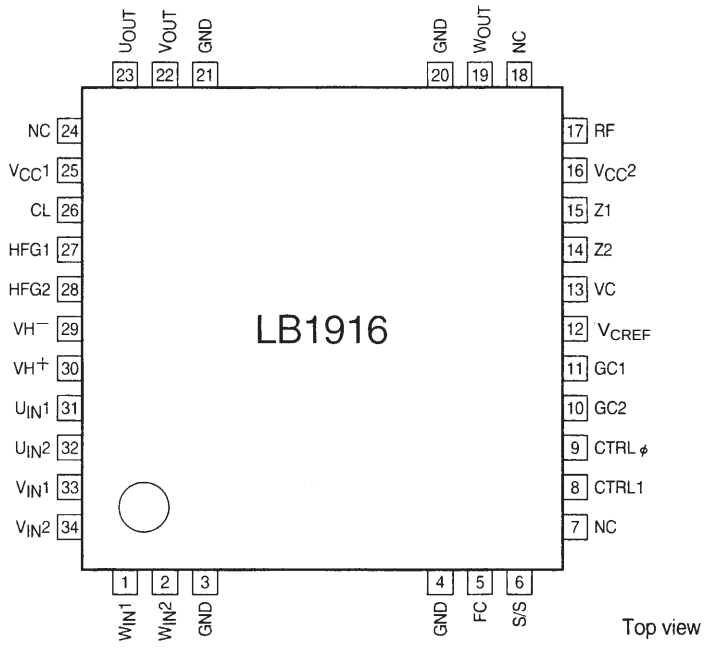
Mode Switching Truth Table

CTRL0	CTRL1	Mode
L	L	Control
L	H	Control
H	L	Acceleration
H	H	Deceleration

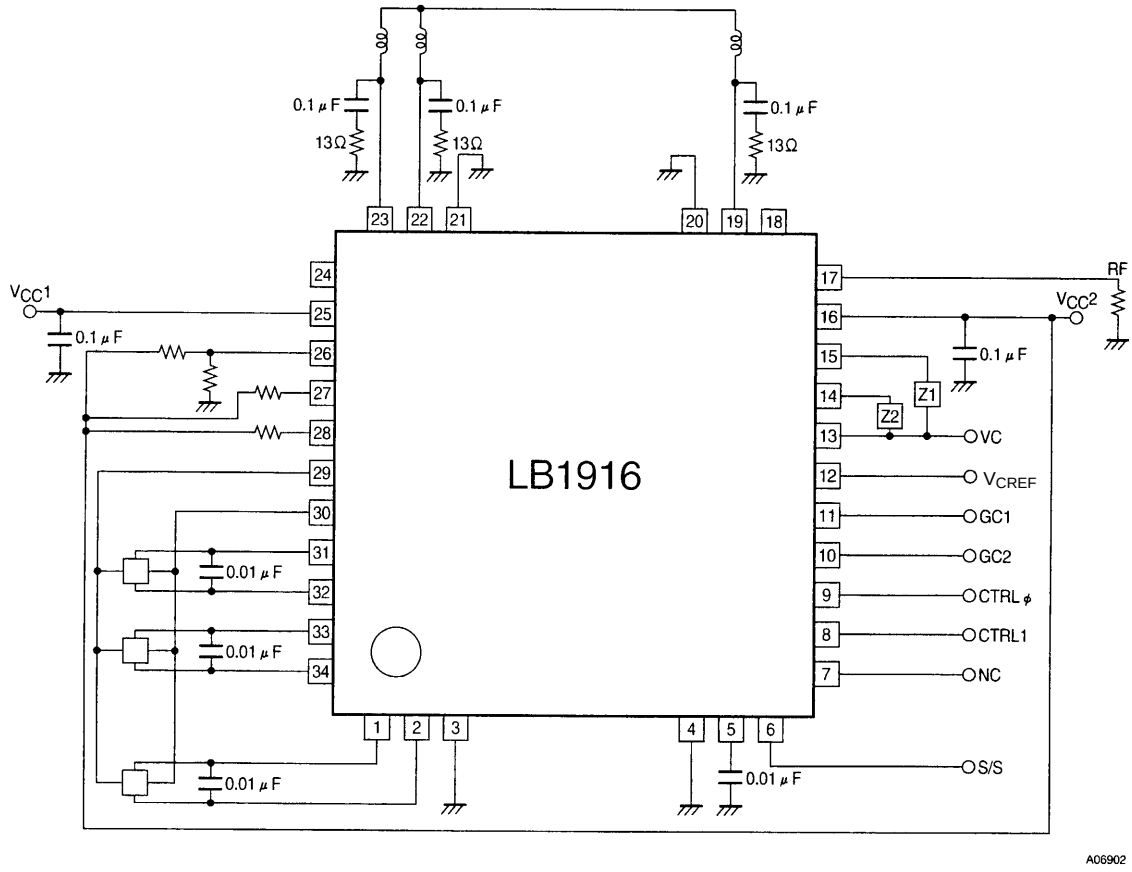
The low level is 0 to 1.0 V

The high level is 4.0 V or higher

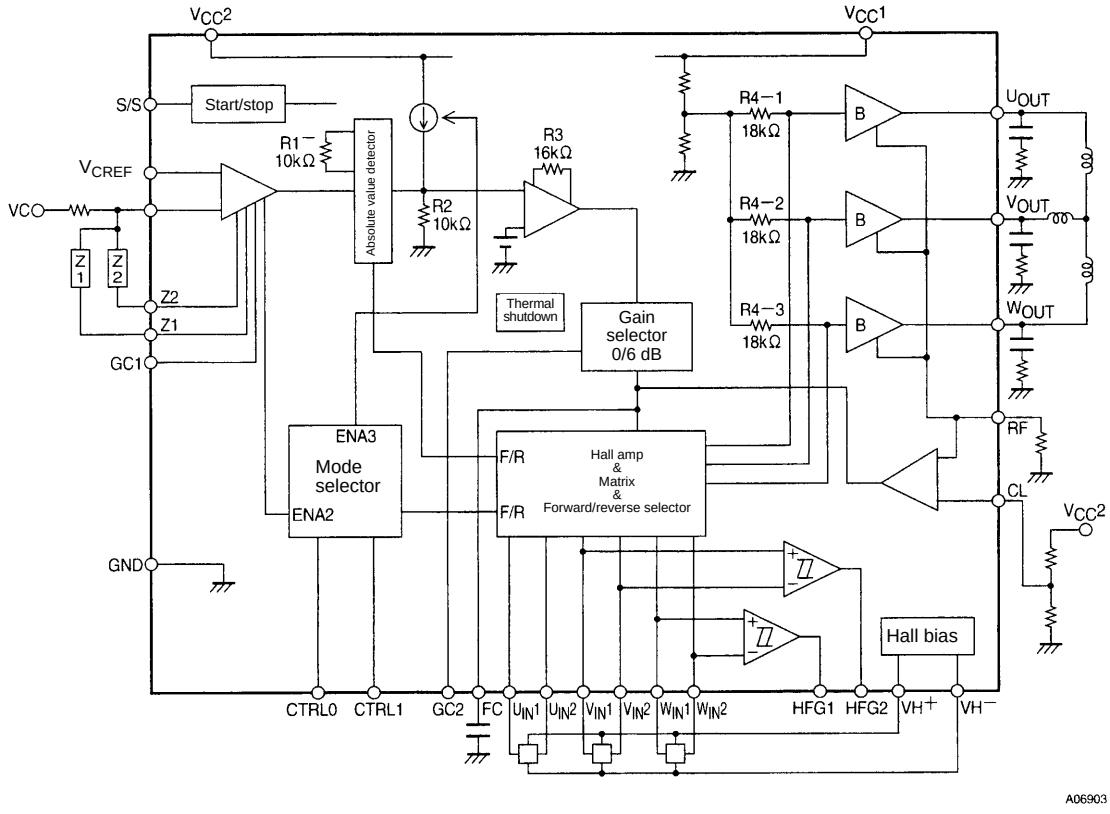
Pin Assignment



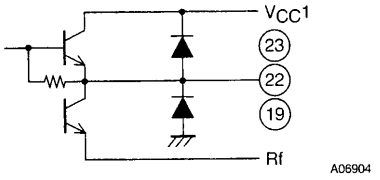
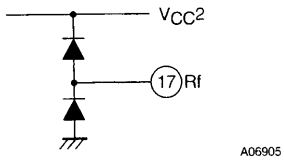
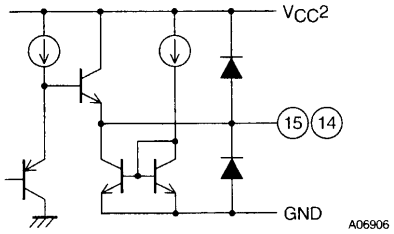
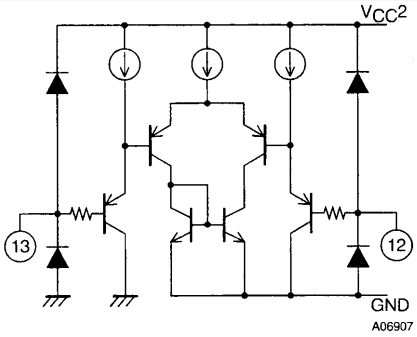
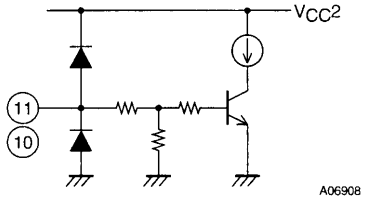
Peripheral Circuit Example



Block Diagram



Pin Functions

Pin No.	Pin	Pin voltage	Pin function	Equivalent circuit
3, 4, 20, 21	GND		• GND	
23 22 19	U_{OUT} V_{OUT} W_{OUT}		• Outputs • Connect these pins to the motor.	
17	Rf		• Ground for the output transistors • The output current can be detected as a voltage by connecting a resistor between the Rf pin and ground. This can then be used to implement overcurrent protection.	
18, 24, 7	NC		• No connection	
16	$V_{CC}2$	4.3 to 6.5 V	• Power supply for circuits other than the output block • The power supply provided by this pin must be well stabilized so that noise does not occur.	
15 14	Z1 Z2		• Connections for the resistors that set the front-end amplifier gain • Z1 and Z2 are common, and have a resistance of between a few tens of kΩ and a few hundreds of kΩ. • The gain is about 6 dB.	
13 12	V_C V_{CREF}	$\frac{V_{CC}2}{2}$ ±1.0	• V_C is the speed control pin. When $V_C > V_{CREF}$: Forward rotation When $V_C < V_{CREF}$: Reverse rotation The output voltage is controlled by the V_C voltage. • V_{CREF} determines the motor control stop voltage. Normally, this will be $V_{CC}2/2$.	
11 10	GC1 GC2	0 to $V_{CC}2$	• I/O gain switching input • GC1 switches Z1 and Z2 for the front end amplifier. When GC1 is low, Z1 is selected, and when GC1 is high, Z2 is selected. GC2 switches the amplifier in the second stage.	

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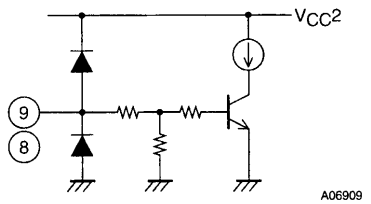
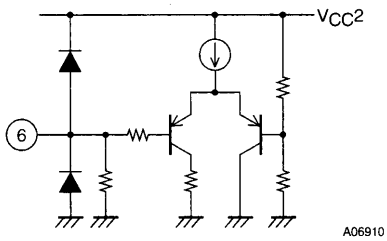
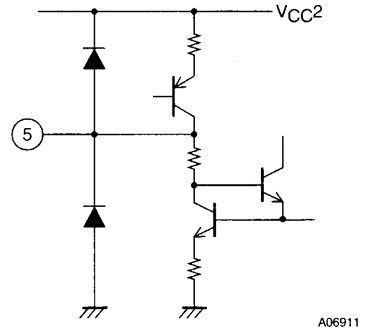
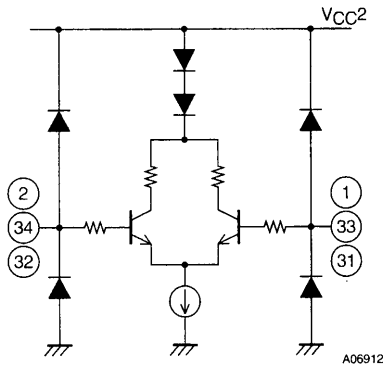
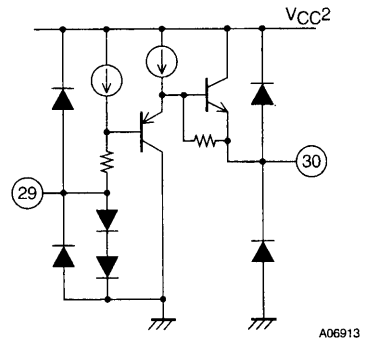
Pin No.	Pin	Pin voltage	Pin function	Equivalent circuit
9 8	CTRLϕ CTRL1	0 to $V_{CC}2$	• Operating mode switching input • These pins select control, acceleration, or deceleration according to the mode switching truth table.	
6	S/S	0 to $V_{CC}2$	• Apply a high level to the S/S pin for start, and a low level for stop. • The threshold is $V_{CC}2/2$.	
5	FC		• Oscillation can be prevented by connecting a capacitor between the FC pin and ground to lower the I/O gain frequency characteristics.	
2 1 34 33 32 31	W_{IN2} W_{IN1} V_{IN1} V_{IN2} U_{IN2} U_{IN1}	1.3 to 2.2 V	• W phase Hall element inputs Logic high is when $W_{IN}1 > W_{IN}2$. • V phase Hall element inputs Logic high is when $V_{IN}1 > V_{IN}2$. • U phase Hall element inputs Logic high is when $U_{IN}1 > U_{IN}2$.	
30 29	VH^+ VH^-	2.4 V 1.4 V	• Hall element power supply There is a potential difference of 1.0 V between VH^+ and VH^-.	

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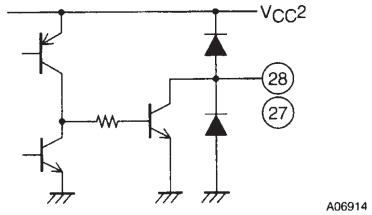
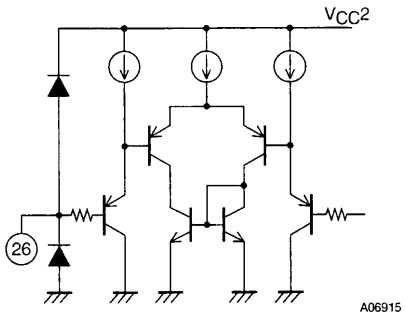
Pin No.	Pin	Pin voltage	Pin function	Equivalent circuit
28 27	HFG2 HFG1	0 to $V_{CC}2$	• Hall FG pins • The Hall waveform is modified and used as FG pulses. • The phase relationship between HFG1 and HFG2 is used as a forward/reverse signal.	
26	CL	0 to $V_{CC}2$	• The current limiter operates when the Rf pin voltage reaches the voltage on the CL pin. The CL potential is determined externally.	
25	$V_{CC}1$	5 to 12.5 V	• Power supply for the output block • The power supply provided to this pin must be well stabilized so that noise does not occur.	