

MAINTENANCE MANUAL SYNTHESIZER LOADER BOARD PL19D902207G1

TABLE OF CONTENTS

	Page
DESCRIPTION	1
CIRCUIT ANALYSIS	1
OUTLINE DIAGRAM	6
SCHEMATIC DIAGRAM	7
PARTS LIST	8

DESCRIPTION

Synthesizer Loader Board is a microprocessor controlled, synchronous, serial data loader. Three lines are used to send serial data to a synthesizer or synthesizer board assembly. These signals are CLOCK, DATA and LATCH. They are sent on power up or on manual reset. One input line, LOCK, is used to monitor lock status of the synthesizer and trigger a hardware reset if the condition goes "unlocked".

Refer to Figure 1 and the Schematic Diagram in the following discussion.

CIRCUIT ANALYSIS

The Synthesizer Loader provides three outputs: CLOCK, DATA and LATCH. These signals are used by synthesizers to generate the assigned operating frequencies. They are derived by microprocessor U2 on the basis of inputs from channel selector switches S1, S5, S3, mode switch S2 and crystal Y1. The microprocessor is controlled by the program contained in EPROM U3.

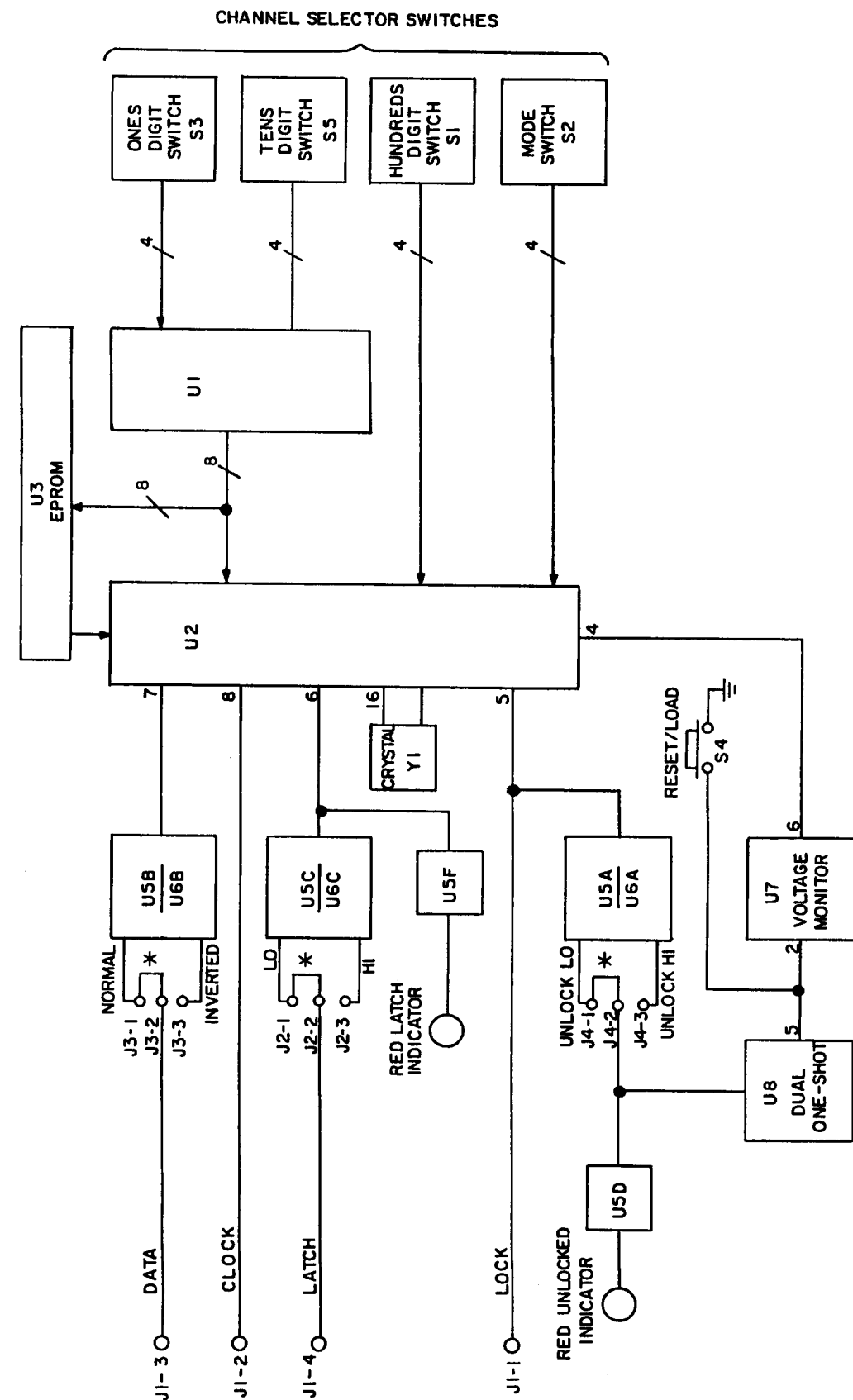
CLOCK, DATA and LATCH signals are sent on power up. After they are sent the microprocessor is turned off and its oscillator is shut down. The only way the microprocessor can be turned on again is through a hardware reset.

DATA

The data signal determines the frequencies to be generated by the synthesizers. Its content is determined by the setting of mode switch S2 and channel selector switches S1, S5 and S3. These switches are connected to microprocessor U2 by 4- and 8-bit parallel data busses.

Mode switch S2 is connected to the microprocessor by a 4-bit parallel data bus. Operating mode is determined by the base transmitter and receiver frequencies, the size of the channel steps, reference oscillator frequency and the type of synthesizer used. Any one of seven operating modes and three test modes can be selected by the setting of Mode switch S2. They are shown in the Mode Select Table. Each of the operating modes have unique loop counters (programmed bit-lengths), reference dividers, base frequency dividers, and data/latch pulse widths. Except for test modes, these values are "hard-coded" variables in the source code.

The operating channel is selected by setting the decimal channel number into the channel selector switches. Switch S1 sets the hundreds digit, switch S5 sets the tens digit, and switch S3 sets the ones digit. Hundreds digit switch S1 is connected to the microprocessor by a 4-bit parallel data bus. Both the tens and ones digit switches are connected into U1 via 4-bit parallel data busses. U1 provides this data to the microprocessor U2 on an 8-bit parallel data bus.



* FACTORY JUMPER POSITIONS

Figure 1 - Synthesizer Loader Block Diagram

Under the direction of the program in EPROM U3, microprocessor U2 scans the data from the switches and derives the DATA signal. The DATA signal, in serial form, is applied to the inputs of buffers U5B and U6B through U2-7.

The DATA signal as positive logic, taken from U5B through the jumper from J3-1 to J3-2, is applied to J1-3. It is also available as negative logic at the output of U6B. This can be routed to J1-3 by changing the jumper to connect J3-2 to J3-3.

CLOCK

The clock signal provided by the microprocessor is based on the input from crystal Y1. It is applied to J1-2 through U2-8.

LATCH

The LATCH signal provided by the microprocessor is connected from U2-6 to the input of buffers U5C and U6C and to the red latch indicator through LED driver U5F.

A low-going latch pulse, taken from the output of U5C, is applied to J1-4 through the jumper connecting J2-1 to J2-2. An inverted pulse is also available. It can be taken from the output of U6C by changing the jumper to connect J2-2 to J2-3.

MODE SELECT TABLE

Mode	IF (MHz)	Base TX (MHz)	Base RX (MHz)	CH Step (kHz)	Ref Osc (MHz)	Synth
0	70	851.0000	736.0000	25	12.8	MC145159
1	70	851.0125	736.0125	25	12.8	MC145159
2-TST	70	851.0000	736.0000	12.5	12.8	MC145159
3	70	935.0000	826.0000	12.5	17.6125	MC145159
4-TST	70	935.0000	826.0000	12.5	17.6125	MC145159
5						
6	70	935.0000	826.0000	12.5	12.8	MB1501A
7						
8						
9						
A	45	851.0000	761.0000	25	12.8	MC145159
B	45	851.0125	761.0125	25	12.8	MC145159
C	45	851.0125	761.0125	25	10.0	MC145159
D						
F-TST	Self test mode for manufacturing inspection.					

NOTE: The base frequencies are the lowest that the synthesizer will generate for the chosen mode, TX being the lowest transmit frequency and RX being the lowest injection frequency for the given IF. All 70 MHz IF modes are for future applications. Mode B is the standard mode for stations except where the border frequency plan is required in which case Mode A is used.

HARDWARE RESET

After sending the synthesizer information, the processor will turn itself off, shutting down its oscillator. The only way for the processor to turn on is through a hardware reset. This function is provided by voltage monitor U7. In addition to monitoring the operating voltage (Vcc), U7 also receives inputs from Reset/Load switch S4 and dual one-shot multivibrator U8. The one-shot multivibrator is triggered by an UNLOCK signal from the synthesizer.

A hardware reset will occur if voltage monitor U7 detects a voltage spike or a drop in the operating voltage (Vcc). This will cause a reset pulse to go from U7-6 to U2-9 on the microprocessor, and the synthesizer information will be sent again.

A hardware reset will occur if Reset/Load switch S4 is pressed. This forces a drop in Vcc, and U7 will send a reset pulse to the microprocessor as described above.

A hardware reset will occur if the synthesizer becomes "unlocked". In this event, a signal from the synthesizer, coming in on J1-1, is applied to U8 through buffer U5A or U6A. This signal can be interpreted as either positive or negative logic. It will be low if the jumper connects J4-1 to J4-2; it will be high if the jumper connects J4-2 and J4-3. The signal is applied to the red unlocked indicator through LED driver U5D, and U8-8 on the multivibrator. When the one-shot multivibrator is triggered, it sends a pulse out on U8-5 to U7-2 on the voltage monitor U7. The voltage monitor will send a reset pulse to the microprocessor as described above, provided Vcc is present.

NOTE

Figure 1 shows the position of the jumpers when the board is manufactured. The jumpers will be in these positions if the board is ordered separately. When assembled in GEMARC V 800 MHz Repeater Stations the LATCH jumper is changed to connect J2-2 to J2-3 and the UNLOCK jumper is changed to connect J4-2 to J4-3.

TEST MODES

When mode switch S2 is set to one of the test modes, the ones, tens and hundreds channel selector switches (S3, S5 and S1) are used to set up other functions. These are detailed below.

Ones And Hundreds Switch Select

During the test modes, the ONES switch will select the duration of the LATCH pulse in 400 uSec increments starting from 200 uSec (200-3800 uSec), and the HUNDREDS switch will select the rate of switching from band-end to band-end according to the following chart:

POSITION ACTIVITY

0	band-end to band-end 100 mS between loads
1	band-end to band-end 200 mS between loads
2	band-end to band-end 300 mS between loads
3	band-end to band-end 400 mS between loads
4	band-end to band-end 500 mS between loads
5	one-shot mode (restart with push-button) - programs low-end channel only!
6	step through all channels, 100 mS between each
7	step through all channels, 300 mS between each
8	reserved
9	reserved

Tens Switch Select

During MODE 2 (TEST MODE), the TENS switch will determine which of the operational mode systems is to be tested according to the following:

POSITION OPERATIONAL MODE UNDER TEST

0	Tests operations MODE 0 & MODE 1 type systems shown above.
1	Tests operational MODE A & MODE B type systems shown above.
2	Tests operational MODE C type systems shown above.

MODE 4 (TEST MODE) tests MODE 3 type systems only.

CHANNEL NUMBER CALCULATION

The channel number associated with an assigned frequency can be calculated.

Let:

Fo = The operating frequency.

F1 = The base frequency (either transmit or receive) specified for a given mode of operation on the Mode Select Table in MHz.

N = The channel number.

S = The channel step specified for a given mode of operation on the Mode Select Table in MHz.

To calculate channel number: $N = \frac{F_o - F_1}{S}$

For example: transmit frequency Fo = 853.5125
MHz
Mode is B

From Mode Select Table:

base transmit frequency F1 = 851.0125
channel step S = 25 kHz (0.025 MHz)

$$N = \frac{853.5125 - 851.0125}{0.025}$$

$$= \frac{2.5}{0.025}$$

$$= 100$$

If the channel is known, the frequency can be calculated using:

$$F_o = (N \times S) + F_1.$$

For example: channel number N = 100
Mode is B

From Mode Select Table:

base transmit frequency F1 = 851.0125
channel step S = 25 kHz (0.025 MHz)

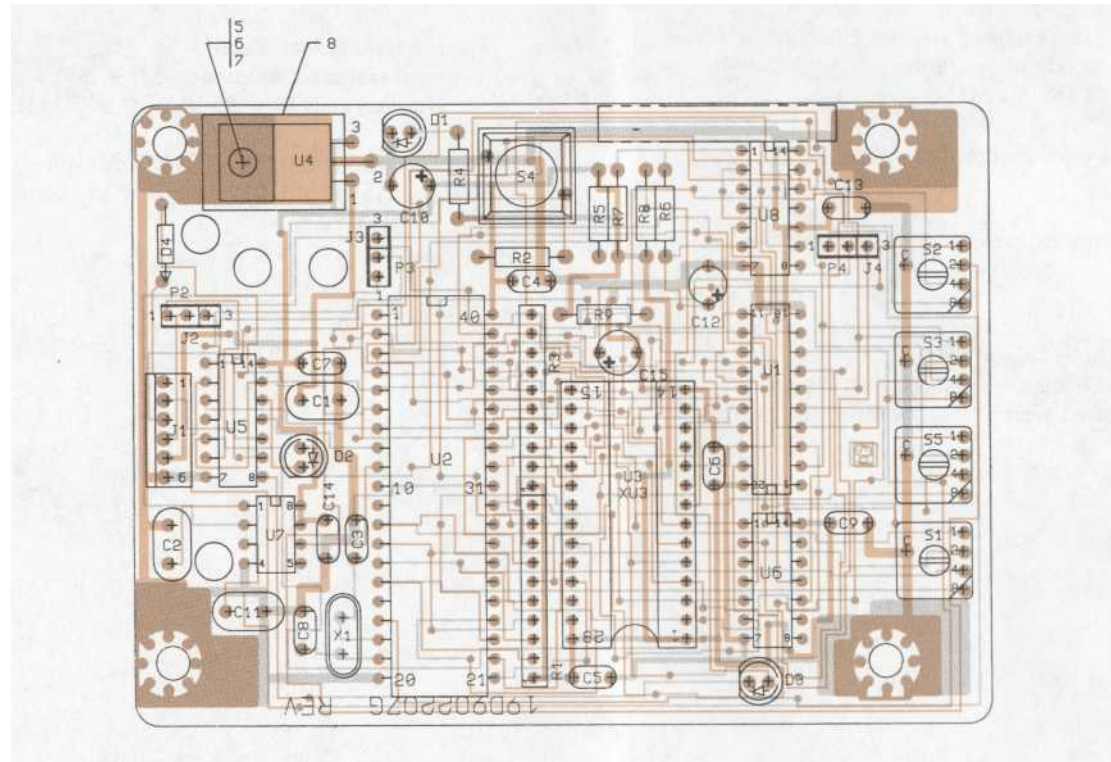
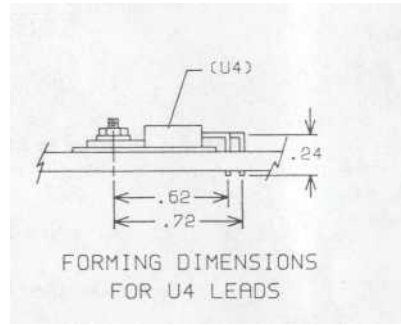
$$F_o = (100 \times 0.025) + 851.0125$$

$$= 2.5 + 851.0125$$

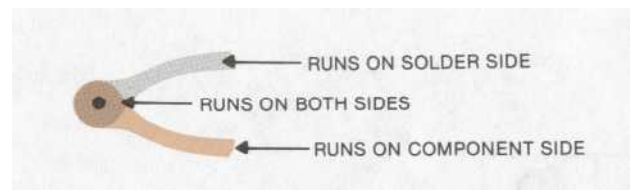
$$= 853.5125$$



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(19D902207, Sh. 1, Rev. 1)
(19D902206, Component Side, Rev. 2)
(19D902206, Solder Side, Rev. 2)



SYNTHESIZER LOADER BOARD
19D902207G1

PARTS LIST
SYNTHESIZER LOADER BOARD
19D90220701
ISSUE 2

SYMBOL	GE PART NO.	DESCRIPTION
----- CAPACITORS -----		
C1 and C2	T644ACP410K	Polyester: 0.1 uF ±10%, 50 VDCW.
C3	19A700235P15	Ceramic: 15 pF ±5%, 50 VDCW.
C4 thru C7	T644ACP310K	Polyester: .010 uF ±10%, 50 VDCW.
C8	19A700235P15	Ceramic: 15 pF ±5%, 50 VDCW.
C9	T644ACP310K	Polyester: .010 uF ±10%, 50 VDCW.
C10	19A701534P7	Tantalum: 10 uF ±20%, 16 VDCW.
C11	T644ACP410K	Polyester: 0.1 uF ±10%, 50 VDCW.
C12	19A701534P4	Tantalum: 1 uF ±20%, 35 VDCW.
C13 and C14	T644ACP310K	Polyester: .010 uF ±10%, 50 VDCW.
C15	19A701534P5	Tantalum: 2.2 uF, ±20%, 35 VDCW.
----- DIODES -----		
D1	19A134354P3	Optoelectronic: Green: sim to NP 5082-4955.
D2 and D3	19A134354P1	Optoelectronic: Red: sim to NP 5082-4655.
D4	19A700047P3	Silicon: 100 mV: sim to 1M6263.
----- JACKS -----		
J1	19A704852P32	Printed wire, two part: 6 contacts, sim to Molex 22-29-2061.
J2 thru J4	19A704852P2	Connector: 3 Pin Male Header.
----- PLUGS -----		
P2 thru P4	19A702104P2	Connector: Shorting Jumper, Gold Plated. (Housing Color: White).
----- RESISTORS -----		
R1	19A701630P2	Resistor, network: 9 resistors rated 10K ohms ±2%, 50 VDCW; sim to Bourns 4310R-101-103.
R2	N212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R3	19A701630P2	Resistor, network: 9 resistors rated 10K ohms ±2%, 50 VDCW; sim to Bourns 4310R-101-103.
R4 and R5	N212CRP133C	Deposited carbon: 330 ohms ±5%, 1/4 w.
R6	N212CRP412C	Deposited carbon: 0.12M ohms ±5%, 1/4 w.
R7	N212CRP330C	Deposited carbon: 30K ohms ±5%, 1/4 w.
R8	N212CRP133C	Deposited carbon: 330 ohms ±5%, 1/4 w.
R9	N212CRP362C	Deposited carbon: 62K ohms ±5%, 1/4 w.
----- SWITCHES -----		
S1	19B800981P3	Rotary: 10 position, contacts rated 10ma @ 5VDC; sim to Copal Electronics S-2030.
S2	19B800981P2	Rotary: 15 position, contacts rated 10 mA @ 10VDC; sim to Copal Electronics S-1030.
S3	19B800981P3	Rotary: 10 position, contacts rated 10ma @ 5VDC; sim to Copal Electronics S-2030.
S4	19A701324P1	Push-Button: sim to IEE/Schedown 210091.
S5	19B800981P3	Rotary: 10 position, contacts rated 10ma @ 5VDC; sim to Copal Electronics S-2030.

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES

SYMBOL	GE PART NO.	DESCRIPTION
----- INTEGRATED CIRCUITS -----		
U1	19A700037P408	Digital: Tri-State Octal Driver: sim to 74LS244.
U2	19A704345P1	Microcomputer: CMOS, 8 bit: sim to TP80C31EM.
U3	19A705782G1	Digital: 8K x 8-Bit EPROM: sim to 27C64. (Programmed).
U4	19A134717P1	Linear: 5 Volt Regulator: sim to MC7805CT.
U5	19A116180P56	Digital: Hex Buffer/Driver with OC outputs: sim to 7407.
U6	19A116180P75	Digital: Hex Open Collector Inverter: sim to 7406.
U7	19A705652P2	Linear: 4.6 Volt Monitor: sim to TL7705A.
U8	19A116968P3	Linear: Dual Timer: sim to Signetics SA556N.
----- SOCKETS -----		
XU3	19A700156P3	Socket, IC: 28 Pins, Tin Plated: sim to AMP 640362P3.
----- CRYSTALS -----		
Y1	19A702511G5	Quartz, 11.520000 MHz.
----- MISCELLANEOUS -----		
	H80P9005B6	Machine screw: pan head, steel.
	7141225P2	Nut, Hex: 4-40.
	H404P11B6	Lockwasher: internal: No. 4.
	19A705469P1	Insulator Plate, TO-220.

PRODUCTION CHANGES
Changes in the equipment to improve performance or to simplify circuits are identified by a "Revision Letter", which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for the descriptions of parts affected by these revisions.

REV. A - SYNTHESIZER LOADER BOARD 19D90220701
To improve operation, added D4 (19A700047P3) between U2 pin 5 and J1 pin 1. This change isolates the lock input from +10 Vdc as on 900 MHz stations.