LC05112CMT

ON Semiconductor®

http://onsemi.com

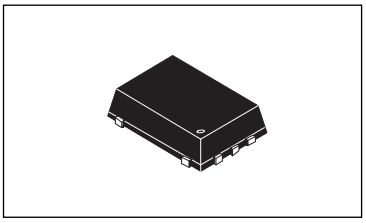
CMOS LSI

1-Cell Lithium-Ion Battery Protection IC with integrated Power MOS FET

Overview

The LC05112CMT is a protection IC for 1-cell lithium-ion secondary batteries with integrated power MOS FET. Also it integrates highly accurate detection circuits and detection delay circuits to prevent batteries from over-charging, over-discharging, over-current discharging and over-current charging.

A battery protection system can be made by only LC05112CMT and few external parts..



WDFN6 2.6x4.0, 0.65P, Dual Flag

Feature

- Charge-and-discharge power MOSFET are integrated at Ta = 25°C, V_{CC} = 4.5V
  ON resistance (total of charge and discharge) 11.2mΩ (typ)
- Highly accurate detection voltage/current at Ta = 25°C, V_{CC} = 3.7V

Over-charge detection	±25mV
Over-discharge detection	±50mV
Charge over-current detection	±0.7A
Discharge over-current detection	±0.7A

- Delay time for detection and release (fixed internally)
- Discharge/Charge over-current detection is compensated for temperature dependency of power FET.
- 0V battery charging : “Unavailable”
- Over charge detection voltage : 4.0V to 4.5V (5mV steps)
- Over charge release hysteresis : 0V to 0.3V (100mV steps)
- Over discharge detection voltage : 2.2V to 2.8V (50mV steps)
- Over discharge release hysteresis : 0V to 0.075V (25mV steps)
- Discharge over current detection : 2.0A to 8.0A (0.5A steps)
- Charge over current detection : –8.0A to -2.0A (0.5A steps)
- Over-discharge detection delay time : 20ms or 128ms

Typical Applications

- Smart phone
- Tablet
- Wearable device

ORDERING INFORMATION

See detailed ordering and shipping information on page 15 of this data sheet.

Specifications

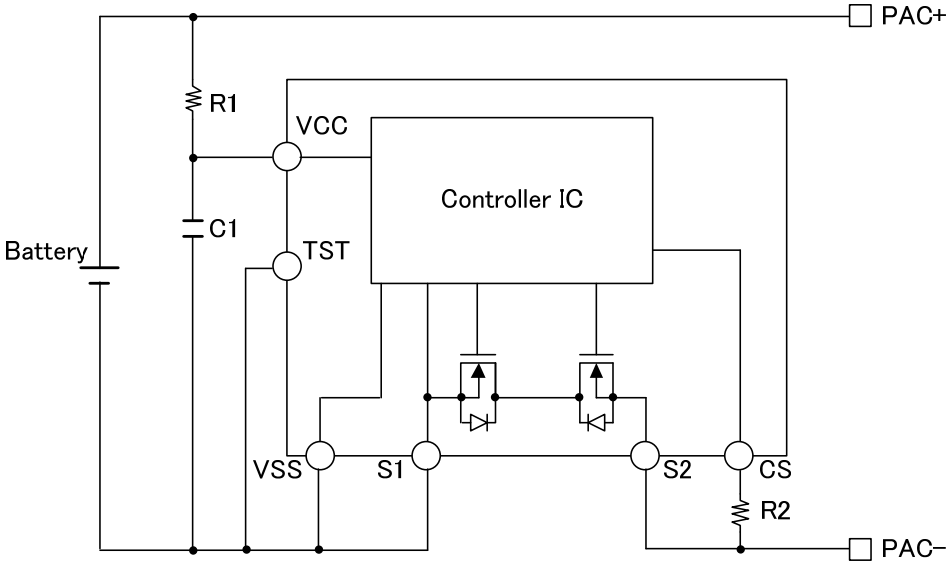
Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	-0.3-12.0	V	Between PAC+ and V_{CC} : R1=680Ω
S1 - S2 voltage	VS1-S2	24.0	V	
CS terminal Input voltage	CS	V_{CC}–24.0	V	
Charge or discharge current	BAT-, PAC-	10.0	A	
TST Input voltage	TST	-0.3-7	V	
Storage temperature	Tstg	–55 to +125	°C	
Current between S1 and S2(DC)	ID	10.0	A	V_{CC} = 3.7V
Current between S1 and S2 (continuous pulse)	IDP	35	A	Pulse Width<10μs, duty cycle<1%
Operating ambient temperature	Topr	–40 to +85	°C	
Allowable power dissipation	Pd	350	mW	Glass epoxy four-layer board. Board size 27.4mm x 3.1mm x 0.8mm
Junction temperature	Tj	125	°C	

Caution 1) Absolute maximum ratings represent the values which cannot be exceeded even for a moment.
Caution 2) If you should intend to use this IC continuously under high temperature, high current, high voltage, or drastic temperature change, even if it is used within the range of absolute maximum ratings or operating conditions, there is a possibility of decrease reliability. Please contact us for a confirmation.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Example of Application Circuit



Components	Recommended value	MAX	unit	Description
R1	680	1k	Ω	
R2	1k	2k	Ω	
C1	2.2μ	4.7u	F	

* We don't guarantee the characteristics of the circuit shown above.

* TST pin would be better to be connected to VSS pin, though it is connected to VSS with internal resistor (100kΩ typ).

Electrical Characteristics at Ta = 25°C, unless otherwise specified.

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Conditions
Detection voltage						
Over-charge detection voltage	Vov	Vov_set -25	Vov_set	Vov_set +25	mV	R1=680ohm
Over-charge release voltage	Vovr	Vovr_set -40	Vovr_set	Vovr_set +40	mV	R1=680ohm
Over-discharge detection voltage	Vuv	Vuv_set -50	Vuv_set	Vuv_set +50	mV	R1=680ohm
Over-discharge release voltage	Vuvr	Vuvr_set -100	Vuvr_set	Vuvr_set +100	mV	R1=680ohm, CS=0V
Discharge over-current detection current	Ioc	Ioc_set -0.7	Ioc_set	Ioc_set +0.7	A	R2=1kΩ, VCC=3.7V,Pulse input
Discharge over-current release current	Iocr	Ioc_set-0.7	Ioc_set	Ioc_set+0.7	A	R2=1kΩ, VCC=3.7V,Pulse input
Discharge over-current detection current (Short circuit)	Ioc2	14.7	21.0	27.3	A	R2=1kΩ, VCC=3.7V,Pulse input
Charge over-current detection current	Ioch	Ioch_set -0.7	Ioch_set	Ioch_set +0.7	A	R2=1kΩ, VCC=3.7V,Pulse input
Charge over-current release current	Iochr	Ioch_set-0.7	Ioch_set	Ioch_set+0.7	A	R2=1kΩ, VCC=3.7V,Pulse input
Input voltage						
0 V battery charge inhibition battery voltage	Vinh	0.4	0.9	1.4	V	
Current consumption						
Operating current	Icc		3.0	6.0	μA	At normal state,VCC=3.7V
Shutt down current	Ishutt			0.1	μA	At Shutt down state,VCC=2.0V
Resistance						
ON resistance 1 of integrated power MOS FET	Ron1	10.4	13.0	18.2	mΩ	VCC=3.1V I=±2.0A
ON resistance 2 of integrated power MOS FET	Ron2	9.6	12.0	15.6	mΩ	VCC=3.7V I=±2.0A
ON resistance 3 of integrated power MOS FET	Ron3	9.2	11.6	15.0	mΩ	VCC=4.0V I=±2.0A
ON resistance 4 of integrated power MOS FET	Ron4	8.8	11.2	14.0	mΩ	VCC=4.5V I=±2.0A
Internal resistance (VCC-CS)	Rcsu		300		kΩ	VCC=2.0V, CS=0V
Internal resistance (VSS-CS)	Rcsd		15		kΩ	VCC=3.7V, CS=1.0V
Detection and Release delay time						
Over-charge detection delay time	Tov	0.8	1.0	1.2	sec	VCC=3.7V
Over-charge release delay time	Tovr	12.8	16.0	19.2	ms	VCC=3.7V
Over-discharge detection delay time	Tuv	102 16	128 20	154 24	ms	VCC=3.7V
Over-discharge release delay time	Tuvr	0.9	1.1	1.3	ms	VCC=3.7V
Discharge over-current detection delay time 1	Toc1	9.6	12.0	14.4	ms	VCC=3.7V
Discharge over-current release delay time 1	Tocr1	3.2	4.0	4.8	ms	VCC=3.7V
Discharge over-current detection delay time 2 (Short circuit)	Toc2	80	200	320	us	VCC=3.7V
Charge Over-current detection delay time	Toch	12.8	16.0	19.2	ms	VCC=3.7V
Charge Over-current release delay time	Tochr	3.2	4.0	4.8	ms	VCC=3.7V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Electrical Characteristics2 at Ta = -30 to +70°C , unless otherwise specified.

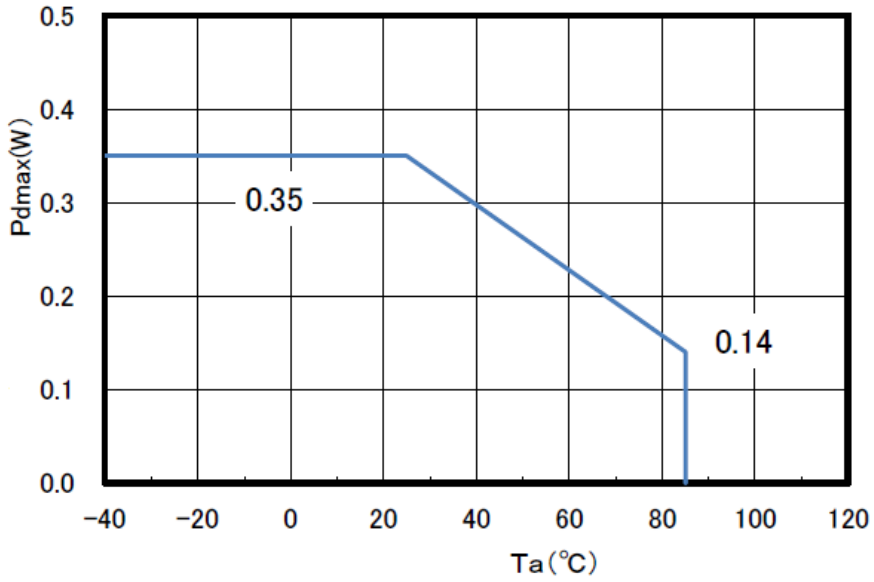
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Conditions
Detection voltage						
Over-charge detection voltage	Vov	Vov_set -30	Vov_set	Vov_set +30	mV	R1=680ohm
Over-charge release voltage	Vovr	Vovr_set -70	Vovr_set	Vovr_set +70	mV	R1=680ohm
Over-discharge detection voltage	Vuv	Vuv_set -80	Vuv_set	Vuv_set +80	mV	R1=680ohm
Over-discharge release voltage	Vuvr	Vuvr_set -120	Vuvr_set	Vuvr_set +120	mV	R1=680ohm,CS=0V
Discharge over-current detection current	Ioc	Ioc_set -1.2	Ioc_set	Ioc_set +1.2	A	R2=1kΩ, VCC=2.5-4.3V, Pulse input
Discharge over-current release current1	Iocr	Ioc_set-1.2	Ioc_set	Ioc_set+1.2	A	R2=1kΩ, VCC=2.5-4.3V, Pulse input
Discharge over-current detection current2 (Short circuit)	Ioc2	10.5	21.0	31.5	A	R2=1kΩ, VCC=2.5-4.3V, Pulse input
Charge over-current detection current	Ioch	Ioch_set -1.2	Ioch_set	Ioch_set +1.2	A	R2=1kΩ, VCC=2.5-4.3V, Pulse input
Charge over-current release current	Iochr	Ioch_set-1.2	Ioch_set	Ioch_set+1.2	A	R2=1kΩ, VCC=2.5-4.3V, Pulse input
Resistance						
Internal resistance (VCC-CS)	Rcsu		300		kΩ	VCC=2.0V, CS=0V
Internal resistance (S1-CS)	Rcsd		15		kΩ	VCC=3.7V, CS=1.0V
Detection and Release delay time						
Over-charge detection delay time	Tov	0.6	1.0	1.5	sec	VCC=3.7V
Over-charge release delay time	Tovr	9.6	16.0	24.0	ms	VCC=3.7V
Over-discharge detection delay time	Tuv	77	128	192	ms	VCC=3.7V
		12	20	30		
Over-discharge release delay time	Tuvr	0.6	1.1	1.5	ms	VCC=3.7V
Discharge over-current detection delay time 1	Toc1	7.2	12.0	18.0	ms	VCC=3.7V
Discharge over-current release delay time 1	Tocr1	2.4	4.0	6.0	ms	VCC=3.7V
Discharge over-current detection delay time 2 (Short circuit)	Toc2	50	200	350	us	VCC=3.7V
Charge Over-current detection delay time	Toch	9.6	16.0	24	ms	VCC=3.7V
Charge Over-current release delay time	Tochr	2.4	4.0	6.0	ms	VCC=3.7V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

SELECTION GUIDE

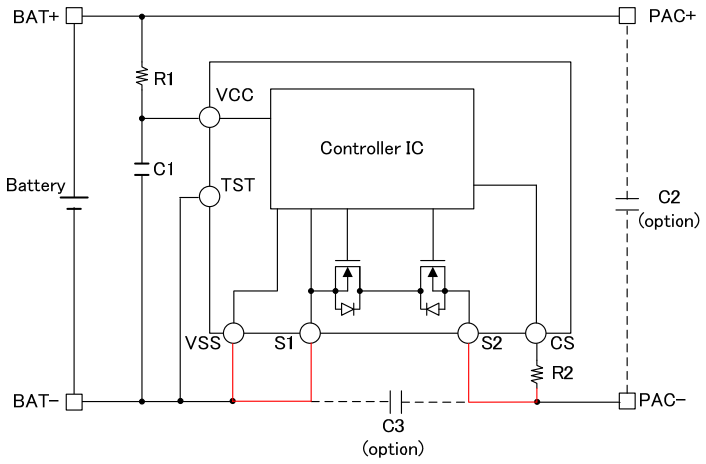
Device	Vov(V)	Vovr(V)	Vuv(V)	Vuvr(V)	Ioc(A)	Ioch(A)	Ioc2(A)	Tuv(ms)	0Vcharge
LC05112C01MTTTG	4.285	4.085	2.200	2.200	6.3	4.0	21	128	unavailable

Pdmax-Ta graph



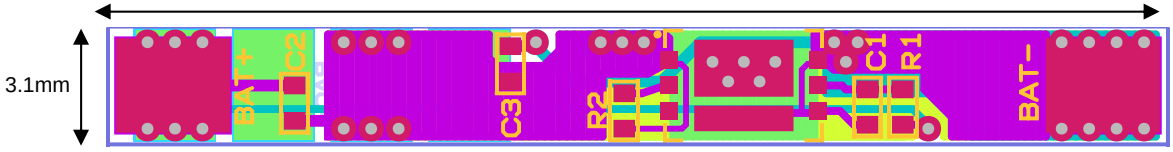
Recommended board layout

Board schematic

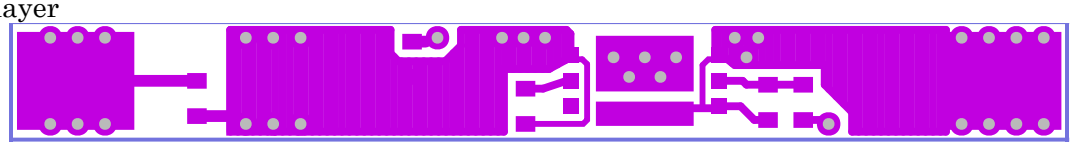


Board size L=27.4mm W=3.1 mm H=0.8mm glass-epoxy 4layers

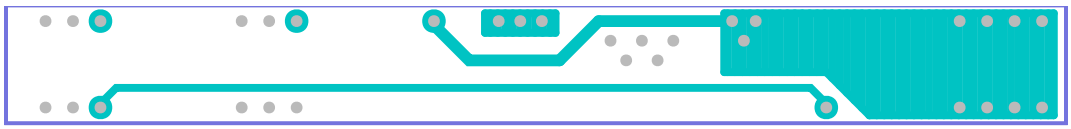
All layer



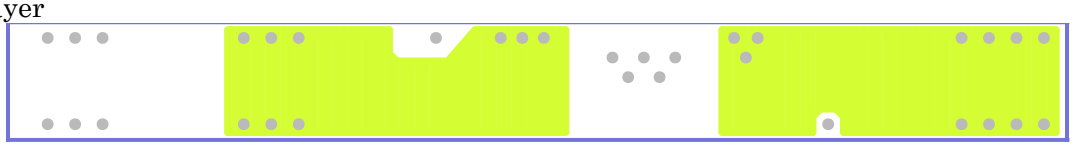
Top layer



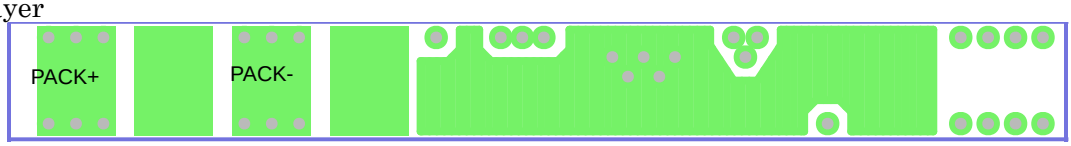
2nd layer



3rd layer



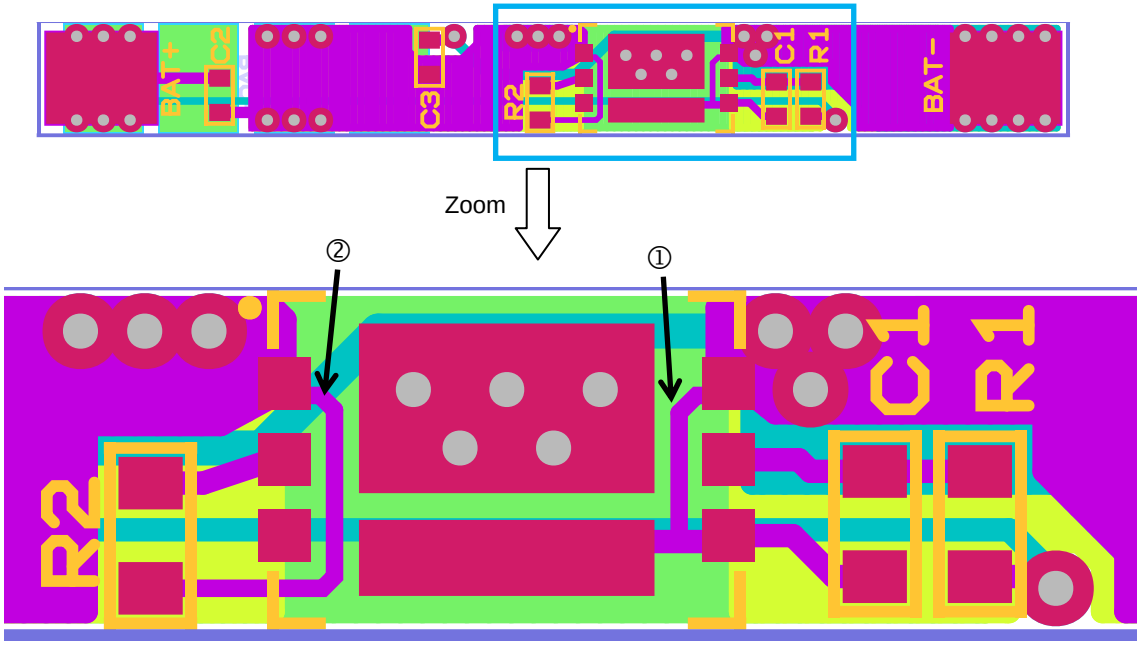
4th layer



Note

① Please connect the VSS line to a pin of S1 directly.
② Please connect the resistance of R2 to a pin of S2 directly.

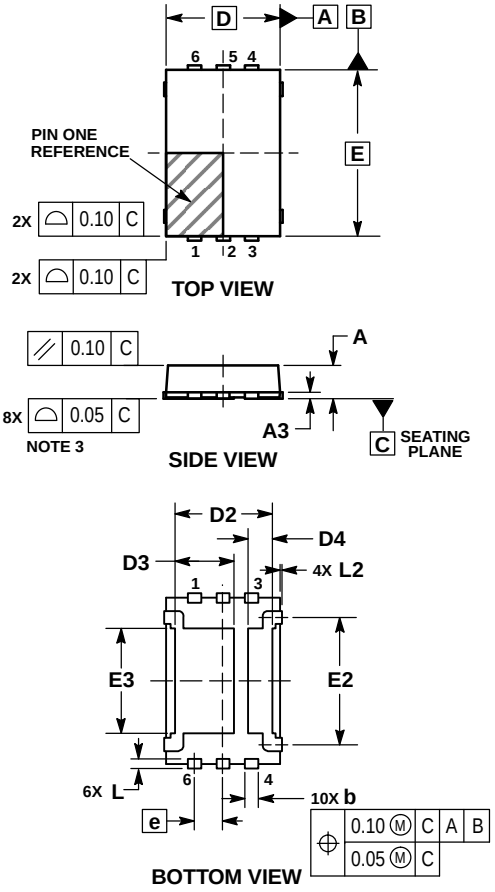
It can perform the detection of the overcurrent exactly by performing these.
It can get rid of influence of the wiring impedance caused by a severe electric current flowing through S1 and S2.
Red line of schematic is very important line.



Package Demensions

unit : mm

WDFN6 2.6x4.0, 0.65P, Dual Flag
CASE 511BZ
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. PROFILE TOLERANCE APPLIES TO THE EXPOSED PADS AS WELL AS THE LEADS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.80
A3	0.10	0.25
b	0.25	0.40
D	2.60 BSC	
D2	2.075	2.375
D3	1.20	1.50
D4	0.40	0.70
E	4.00 BSC	
E2	2.95	3.05
E3	2.25	2.55
e	0.65 BSC	
L	0.12	0.32
L2	---	0.10

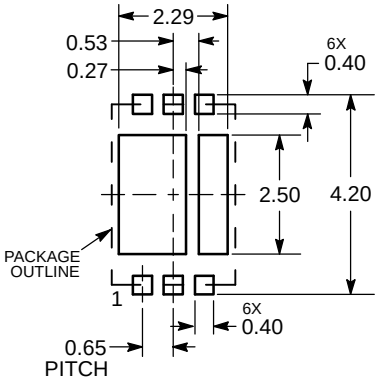
GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.

RECOMMENDED SOLDERING FOOTPRINT*



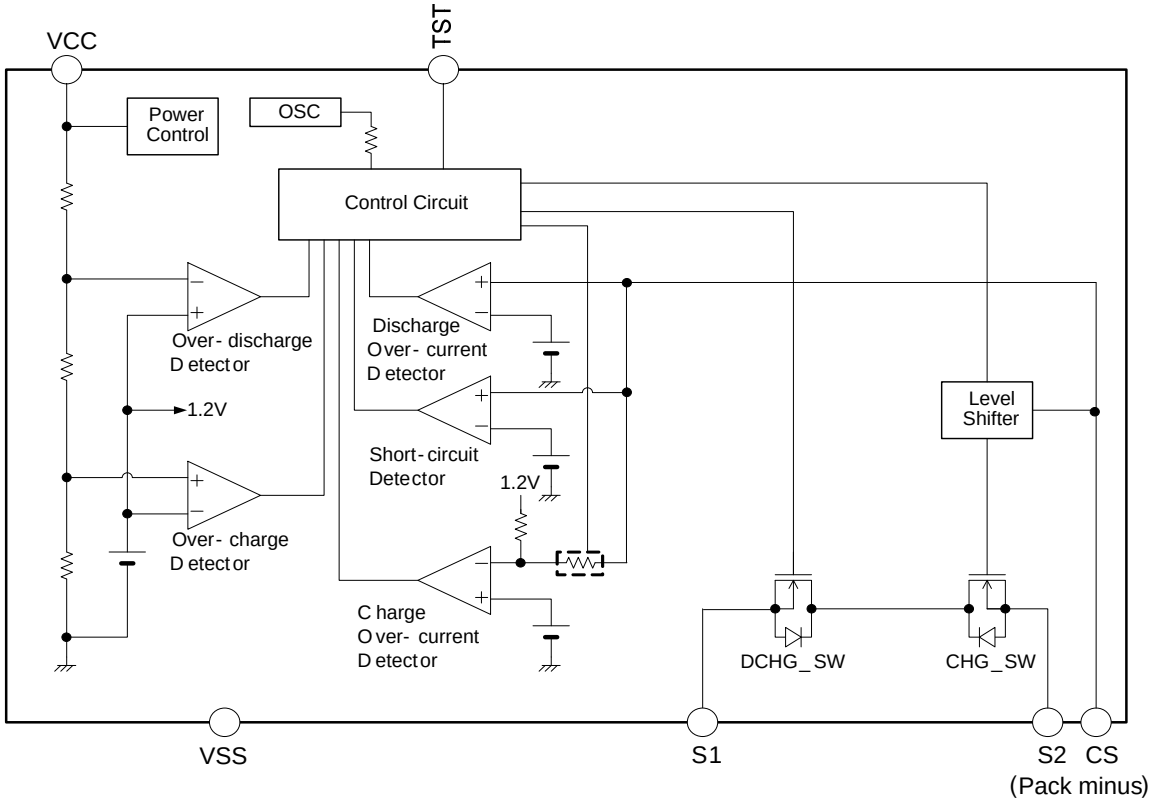
DIMENSION: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Pin Functions

Pin No.	Symbol	Pin Function	Description
1	S2	Charger minus voltage input pin	
2	CS	Charger minus voltage input pin	
3	TST	Package trimming Termainal	Connected to VSS by internal 100kΩ resistor
4	VSS	Negative power input	
5	VCC	VCC terminal	
6	S1	Negative power input	
7	Drain	**Drain of FET**	Exposed pad
8	Sub	**IC Sub (VSS)**	Exposed pad

Block Diagram



Description of operation

(1) Normal mode

- LC05112CMT controls charging and discharging by detecting cell voltage (VCC) and controls S2-S1 current. In case that cell voltage is between over-discharge detection voltage (Vuv) and over-charge detection voltage (Vov), and S2-S1 current is between charge over-current detection current (Ioch) and discharge over-current detection current (Ioc), internal power MOS FETs as CHG_SW, DCHG_SW are all turned ON.
  This is the normal mode, and it is possible to be charged and discharged.

(2) Over-charging mode

- Internal power MOS FET as CHG_SW will be turned off if cell voltage will get equal to or higher than over-charge detection voltage (Vov) over the delay time of over-charging (Tov).
  This is the over-charging detection mode.

- The recovery from over-charging will be made after the following three conditions are all satisfied.
  a. Charger is removed from IC.
  b. CS pin voltage will get equal to or higher than discharge over-current detection current (Ioc) due to load connected
  c. Cell voltage will get lower than over-charge release voltage (Vovr) over the delay time of over-charging release (Tovr) due to discharging through load.

  Consequently, internal power MOS FET as CHG_SW will be turned on and normal mode will be resumed.

- In over-charging mode, discharging over-current detection is made only when CS pin will get higher than discharging over-current detection current 2(Ioc2), because discharge current flows through parasitic diode of CHG_SW FET.
  If CS pin voltage will get higher than discharging over-current detection current 2 (Ioc2) over the delay time of discharging over-current 2 (Toc2), discharging will be shut off, because internal power FETs as DCHG_SW is turned off.(short-circuit detection mode)
  After detecting short-circuit, CS pin will be pulled down to Vss by internal resistor Rcsd.

  The recovery from short circuit detection in over-charging mode will be made after the following two conditions are satisfied.
  a. Load is removed from IC.
  b. CS pin voltage will get equal to or lower than discharging over-current detection current 2 (Ioc2) due to CS pin pulled down through Rcsd.

  Consequently, internal power MOS FET as DCHG_SW will be turned on, and over-charging detection mode will be resumed.

(3) Over-discharging mode

- If cell voltage will get lower than over-discharge detection voltage (Vuv) over the delay time of over-discharging (Tuv), discharging will be shut off, because internal power FETs as DCHG_SW is turned off.
  This is the over-discharging mode.
  After detecting over-discharging, CS pin will be pulled up to Vcc by internal resistor Rcsu and the bias of internal circuits will be shut off. (Stand-by mode)
  In stand-by mode, operating current is suppressed under 0.95uA (max).

- The recovery from stand-by mode will be made by internal circuits biased after the following two conditions are satisfied.
  a. Charger is connected.

- By continuing to be charged, if cell voltage will get higher than over-discharge detection voltage (Vuvr) over the delay time of over-discharging (Tuvr), internal power MOS FETs as DCHG_SW is turned on and normal mode will be resumed.

- In over-discharge detection mode, charging over-current detection does not operate.
  By continuing to be charged, charging over-current detection starts to operate after cell voltage goes up more than over-discharge release voltage (Vuvr).

(4) Discharging over-current detection mode 1

- Internal power MOS FET as DCHG_SW will be turned off and discharging current will be shut off if CS pin voltage will get equal to or higher than discharging over-current detection current (Ioc) over the delay time of discharging over-current (Toc1).
  This is the discharging over-current detection mode 1.
  In discharging over-current detection mode 1, CS pin will be pulled down to Vss with internal resistor Rcsd.

- The recovery from discharging over-current detection mode will be made after the following two conditions are satisfied.
  a. Load is removed from IC.
  b. CS pin voltage will get equal to or lower than discharging over-current release current (Iocr) over the delay time of discharging over-current release (Tocr1) due to CS pin pulled down through Rcsd.

  Consequently, internal power MOS FET as DCHG_SW will be turned on, and normal mode will be resumed.

(5) Discharging over-current detection mode 2 (short circuit detection)

- Internal power MOS FET as DCHG_SW will be turned off and discharging current will be shut off if CS pin voltage will get equal to or higher than discharging over-current detection current2 (Ioc2) over the delay time of discharging over-current 2 (Toc2).
  This is the short circuit detection mode.

- In short circuit detection mode, CS pin will be pulled down to Vss by internal resistor Rcsd.
  The recovery from short circuit detection mode will be made after the following two conditions are satisfied.
  a. Load is removed from IC.
  b. CS pin voltage will get equal to or lower than discharging over-current release current (Iocr) over the delay time of discharging over-current release (Tocr1) due to CS pin pulled down through Rcsd.

  Consequently, internal power MOS FET as DCHG_SW will be turned on, and normal mode will be resumed.

(6) Charging over-current detection mode

- Internal power MOS FET as CHG_SW will be turned off and charging current will be shut off if CS pin voltage will get equal to or lower than charging over-current detection current (Ioch) over the delay time of charging over-current (Toch).
  This is the charging over-current detection mode.

- The recovery from charging over-current detection mode will be made after the following two conditions is satisfied.
  a. Charger is removed from IC and CS pin will get higher by load connected.
  b. CS pin voltage will get equal to or higher than charging over-current release current (Iochr) over the delay time of charging over-current release (Tocrh).

  Consequently, internal power MOS FET as CHG_SW will be turned on, and normal mode will be resumed.

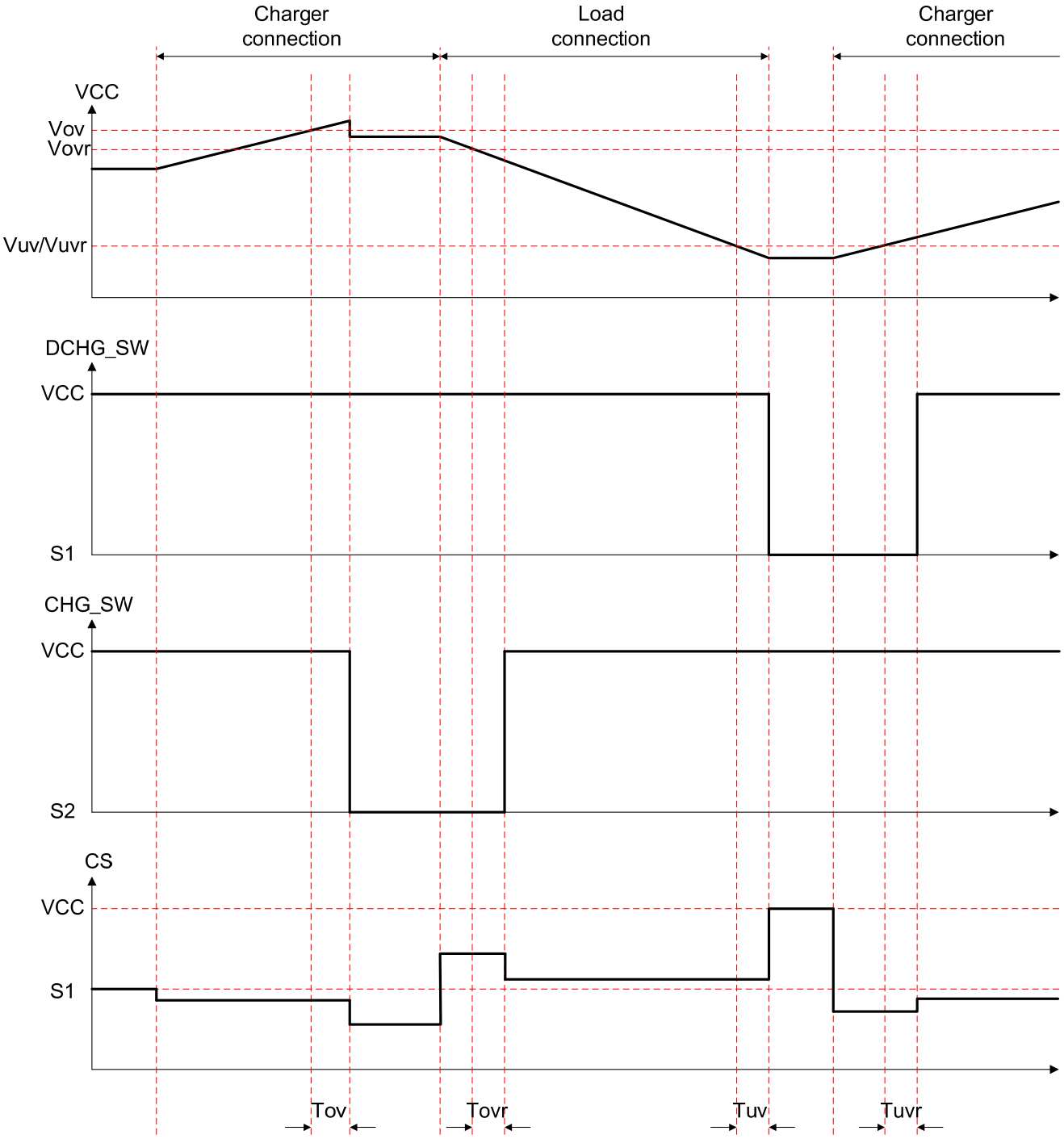
  *Internal current flows out through CS and S2 terminals.
  After charger is removed, it flows through parasitic diode of CHG_SW FET.
  Therefore, CS pin voltage will go up more than charging over-current release current (Iochr).
  So CS pin voltage is not an indispensable condition for recovery from charging over-current detection.

(7) 0V battery charge inhibition function

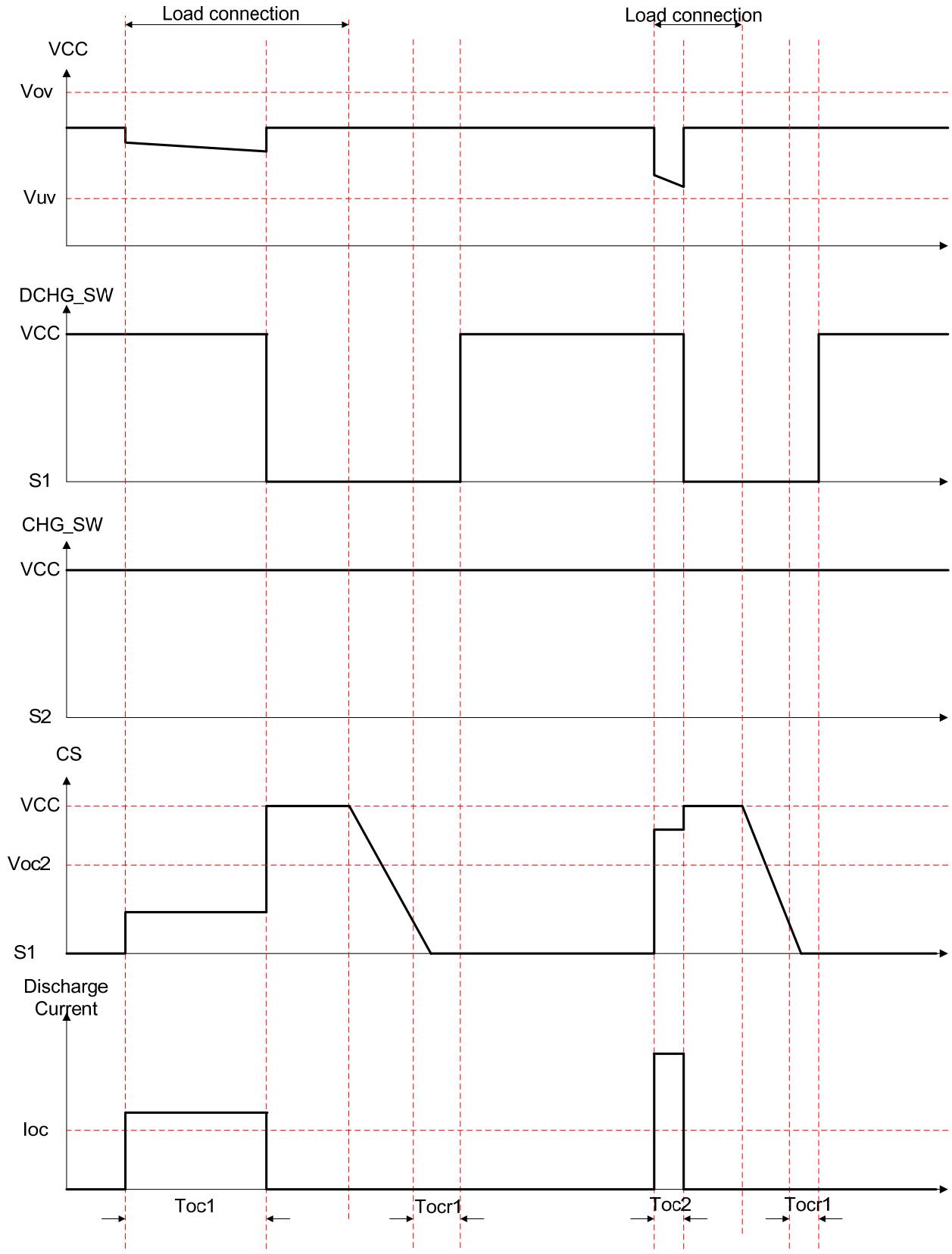
When the battery (0 V battery) of internal short-circuit is connected, it is the function to forbid charge.
When battery voltage is below typ.0.9 V, the gate of FET for charge control is fixed to the PAC-terminal voltage, and charge is forbidden.
It can charge, when battery voltage is more than 0 V battery charge prohibition battery voltage (Vinh).

Timing Chart

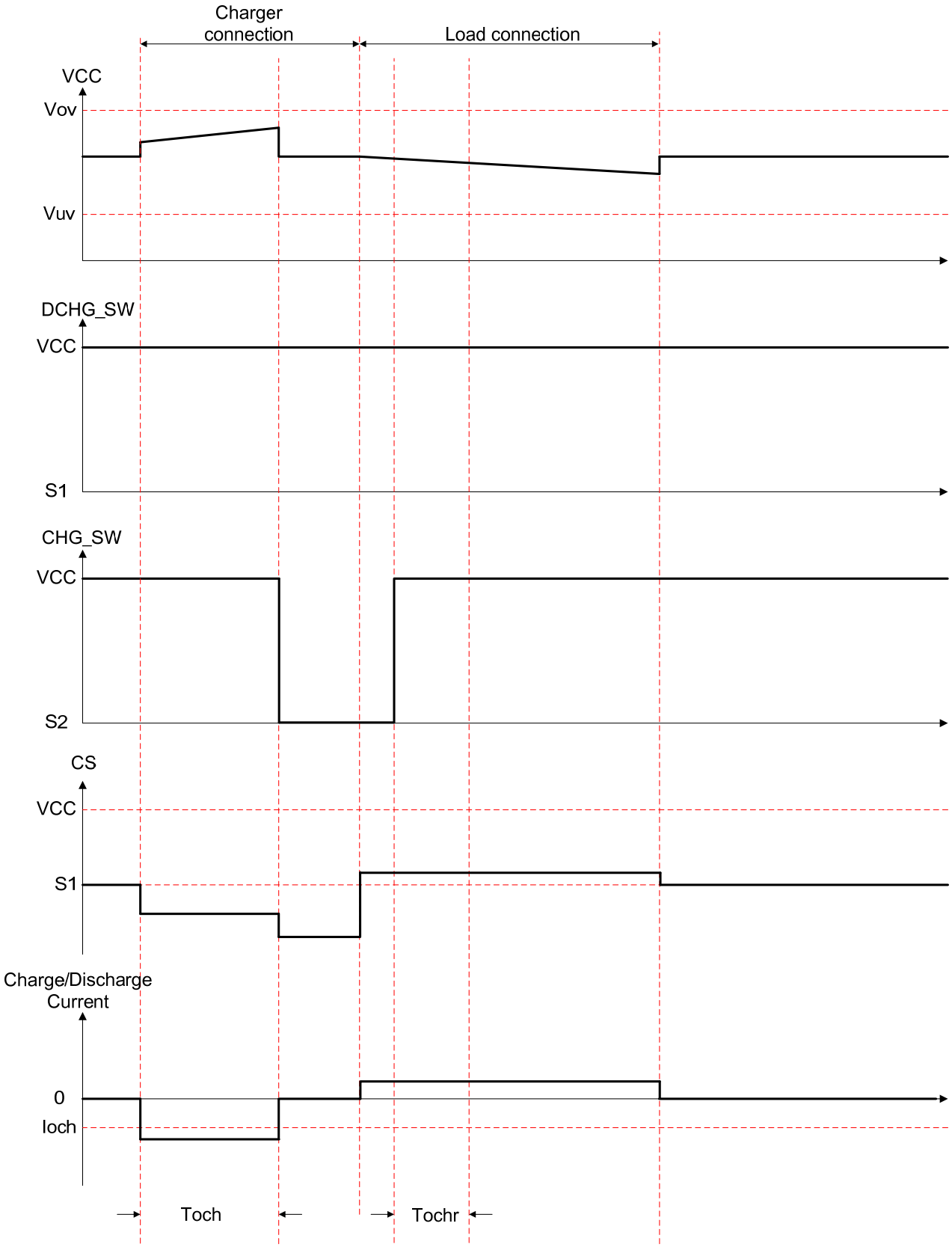
Over-charge detection/release, Over-discharge detection/release (connect charger)



Discharge over-current detection1, Discharge over-current detection2 (Short circuit)



Charge over-current detection



ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC05112C01MTTTG	WDFN6 (2.6×4.0) (Pb-Free / Halogen Free)	4000 / Tape & Reel