LC2452S

16V, 2.5A, 500KHz COT Synchronous Step-Down DC/DC Converter

DESCRIPTION

The LC2452S is a fully integrated synchronous rectified step-down converter that provides wide 4.2V to 16V input voltage range and 2.5A continuous load current capability. The LC2452S can achieve high efficiency and reduce power loss at light load. In shutdown mode, the Max supply current is about 3μA.

The LC2452S protection function includes cycle-by-cycle current limit, UVLO and thermal shutdown. Besides, internal soft-start prevents inrush current at fast power-on. This device uses Constant On-Time (COT) control mode which provides fast load transient response. Internal loop compensation function reduces the external compensator components and simplifies the design process.

The LC2452S requires a minimum number of readily available standard external components and is available in a SOT23-6 tiny package.

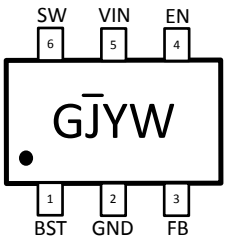
FEATURES

- Wide input voltage range: 4.2V to 16V
- 2.5A output current
- 0.8V reference voltage
- Low $R_{DS(ON)}$ integrated power MOSFET (120/80mΩ)
- 3μA(Max) shutdown current
- Integrated internal compensation
- High efficiency at light load
- Internal 1ms soft-start
- Cycle-by-cycle current limit
- Over-temperature protection with auto recovery
- Under voltage lockout(UVLO)
- Hiccup short circuit protection
- Available in a SOT23-6 tiny package
- RoHS compliant

APPLICATIONS

- Distributed power system
- Flat Panel television and monitors
- STB (Set-top-box)
- Networking, XDSL modem

PIN OUT & MARKING



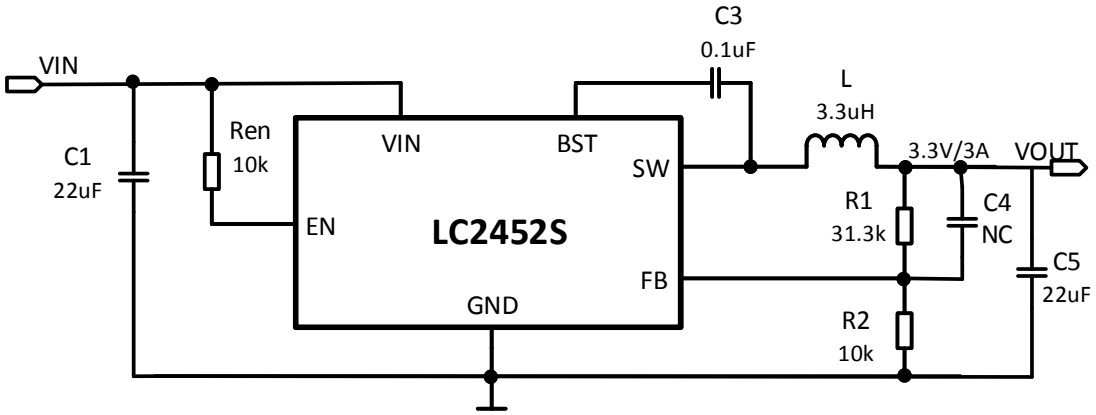
SOT23-6

GJ̄: Product Code
YW: Date code (Year & Week)

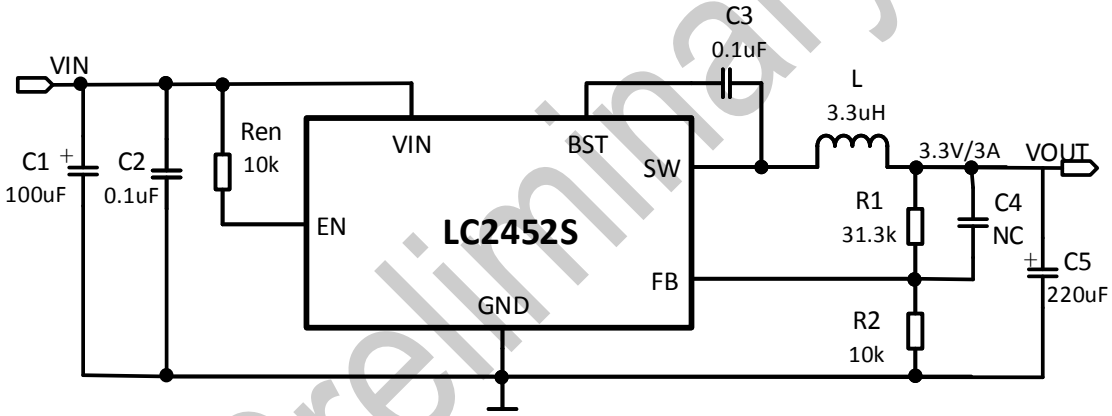
ORDERING INFORMATION

Part No.	LC2452SCB6TR
Package	SOT23-6
Tape&Reel	3000/reel

TYPICAL APPLICATION



C_{IN} &C_{OUT} use Ceramic Capacitors Application Circuit



C_{IN} &C_{OUT} use Electrolytic Capacitors Application Circuit

Table1. Recommended Component Values

V_{IN}=12V, the recommended BOM list is shows as below.

V_{OUT}	C1	C2	L	R1	R2	C5
5V	10uF/MLCC	-	4.7uH-10uH	52.5K	10K	22uF/MLCC
3.3V			3.3uH-4.7uH	31.3K	10K	
1.8V			1.0uH-2.2uH	12.5K	10K	
1.5V			1.0uH-2.2uH	8.8K	10K	
1.2V			1.0uH-2.2uH	5K	10K	
0.9V			1.0uH-2.2uH	1.25K	10K	
5V	100uF/25V/ECL	0.1uF/MLCC	4.7uH-10uH	52.5K	10K	220uF/6.3V/ECL
3.3V			3.3uH-4.7uH	31.3K	10K	
1.8V			1.0uH-2.2uH	12.5K	10K	
1.5V			1.0uH-2.2uH	8.8K	10K	
1.2V			1.0uH-2.2uH	5K	10K	
0.9V			1.0uH-2.2uH	1.25K	10K	

ABSOLUTE MAXIMUM RATING

Parameter	Value
Supply voltage V_{IN}	-0.3V to 18V
Switch node voltage V_{SW}	-0.3V to (V_{IN}+0.5V)
Boost voltage V_{BST}	V_{SW}-0.3V to V_{SW}+5V
Enable voltage V_{EN}	-0.3V to 18V
All other pins	-0.3V to 6V
Operating temperature range	-40°C to 85°C
Storage temperature range	-65°C to 150°C
Lead temperature (Soldering, 10s)	260°C

Note: *Exceed these limits to damage to the device. Exposure to absolute maximum rating conditions may affect device reliability.*

ELECTRICAL CHARACTERISTICS

(V_{IN} =12V, T_A=25°C, unless otherwise stated)

Parameter	Conditions	Min	Typ	Max	Unit
Input voltage range		4.2		16	V
UVLO threshold	V_{IN} rising		3.8		V
UVLO hysteresis	V_{IN} falling		300		mV
Supply current in operation	V_{EN} = 5V, V_{FB} = 1V		150		uA
Supply current in shutdown	V_{EN} = 0V		1		uA
Regulated feedback voltage	V_{IN} = 12V, V_{EN} = 5V	0.784	0.8	0.816	V
High-side switch on resistance	V_{BST-SW} = 5V		120		mΩ
Low-side switch on resistance	V_{IN} = 5V		80		mΩ
High-side switch leakage current	V_{EN} = 0V, V_{SW} = 0V		0.1	1	uA
Peak current limit			5		A
Valley current limit			4		A
Oscillation frequency	V_{OUT} = 1.2V, I_{OUT} = 1A		500		KHz
Maximum duty cycle			80		%
Minimum duty cycle			5		%
Minimum on time			100		ns
Minimum off time			250		ns
EN input voltage “H”		1.5			V
EN input voltage “L”				0.4	V
Soft-start period			0.7		ms
Input OVP	I_{OUT} = 0.1A, V_{IN} rising		19.5		V
Input OVP hysteresis	I_{OUT} = 0.1A, V_{IN} rising		2		V
Thermal shutdown			160		°C
Thermal hysteresis			30		°C

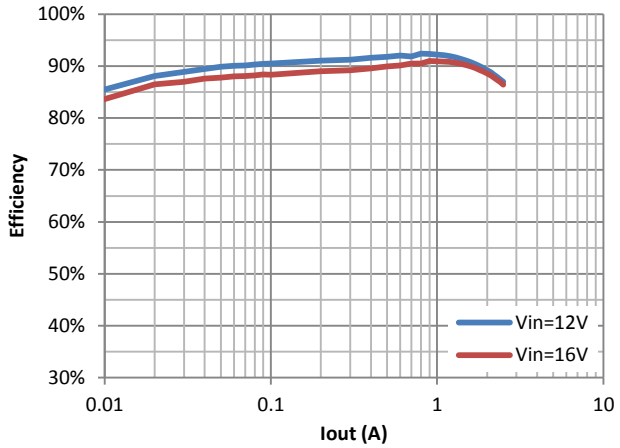
PIN DESCRIPTION

Pin#	Name	Description
1	BST	High side power transistor gate drive boost input.
2	GND	Ground.
3	FB	Feedback input with reference voltage set to 0.8V.
4	EN	Enable input. Set this pin to high level to enable the part, low level to disable.
5	VIN	Power input. Bypass with a 22uF ceramic capacitor to GND.
6	SW	Power switching node to connect inductor.

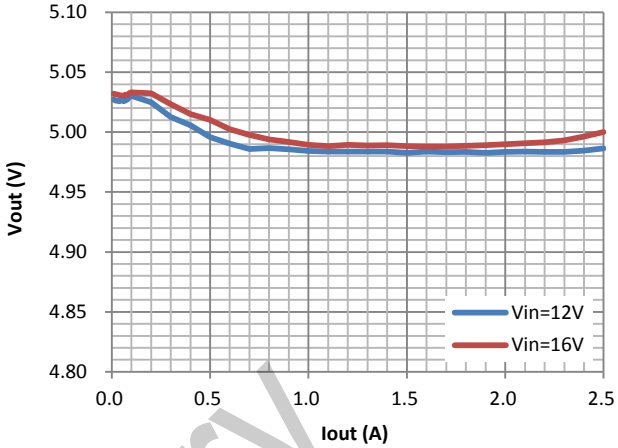
ELECTRICAL PERFORMANCE

Tested under T_A=25°C, unless otherwise specified

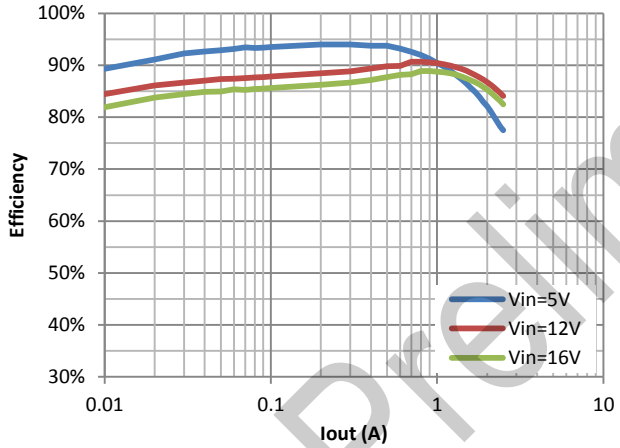
Efficiency vs. Iout
(Vout=5.0V)



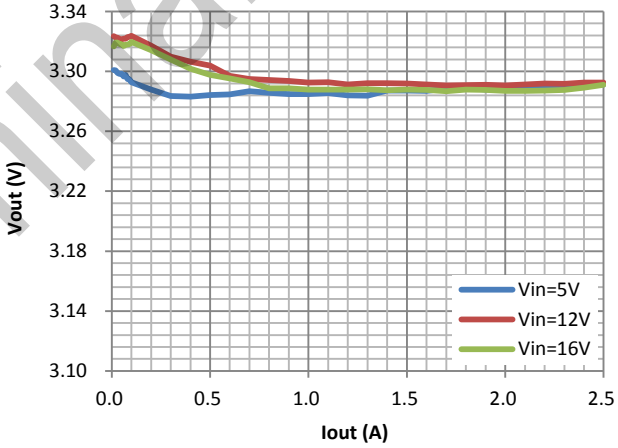
Load Regulation
(Vout=5.0V)



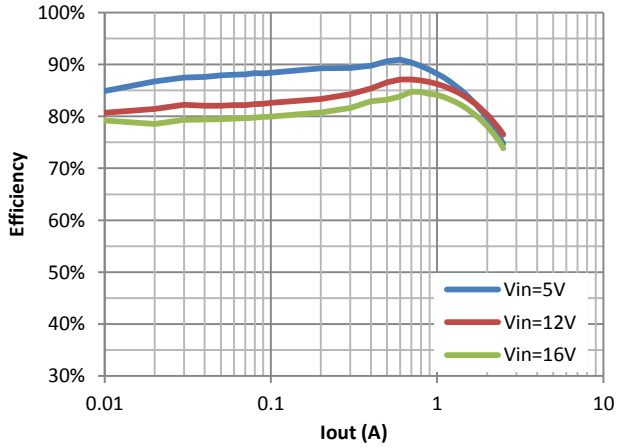
Efficiency vs. Iout
(Vout=3.3V)



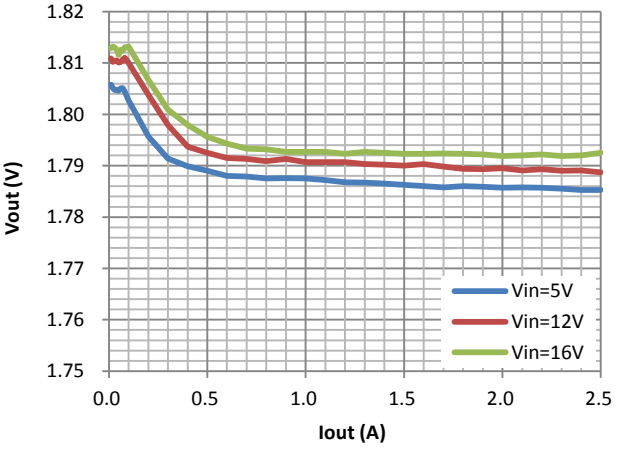
Load Regulation
(Vout=3.3V)



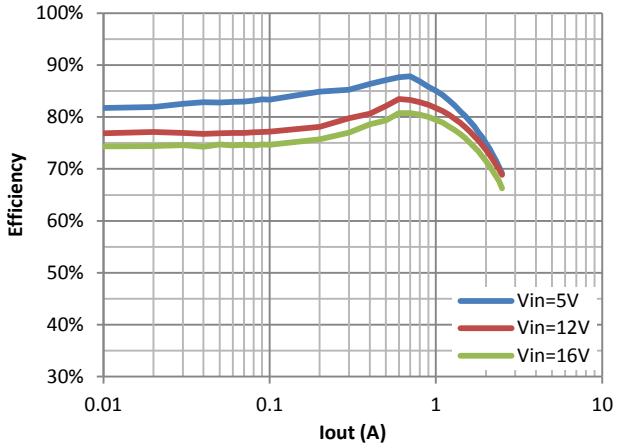
Efficiency vs. Iout
(Vout=1.8V)



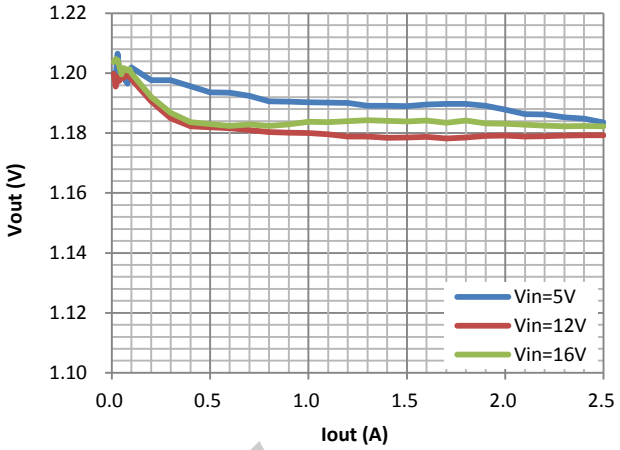
Load Regulation
(Vout=1.8V)



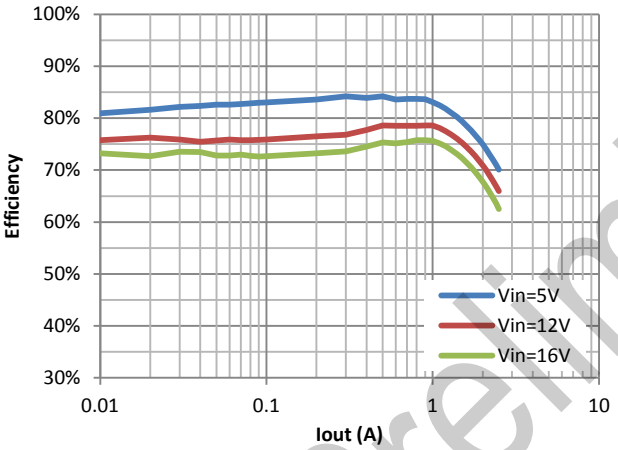
Efficiency vs. Iout
(Vout=1.2V)



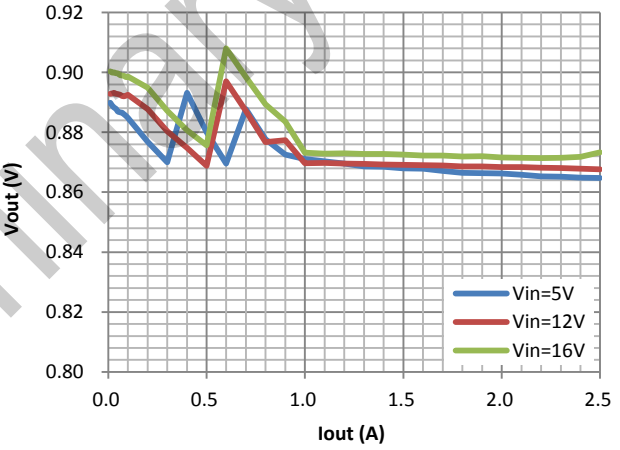
Load Regulation
(Vout=1.2V)



Efficiency vs. Iout
(Vout=0.9V)

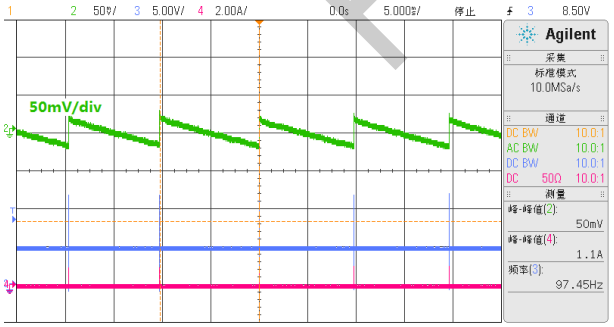


Load Regulation
(Vout=0.9V)



Steady State Waveform

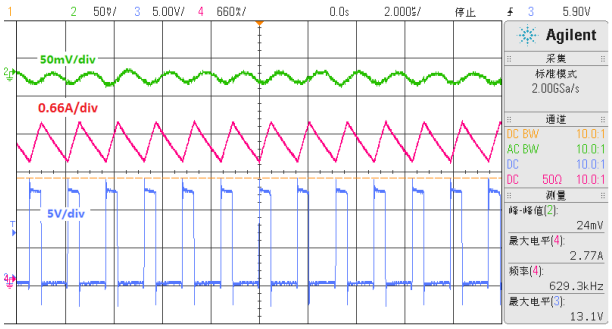
(Vin=12V, Vout=3.3V, Cin=Cout=20uF, L=3.3uH, Iout=0A)



Ch2: Vout, Ch3: V_{SW}, Ch4: I_{SW}

Steady State Waveform

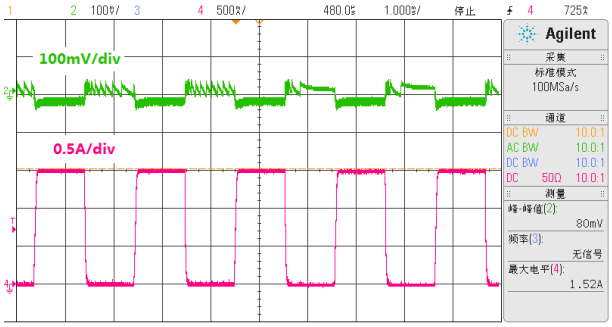
(Vin=12V, Vout=3.3V, Cin=Cout=20uF, L=3.3uH, Iout=2.5A)



Ch2: Vout, Ch3: V_{SW}, Ch4: I_{SW}

Load Transient

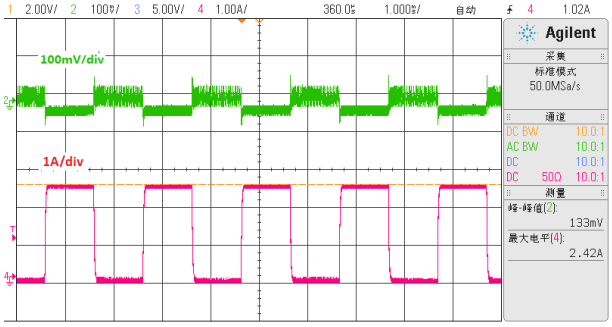
(Vin=12V, Vout=3.3V, Iout=0.01~1.5A)



Ch2: Vout, Ch4: I_L

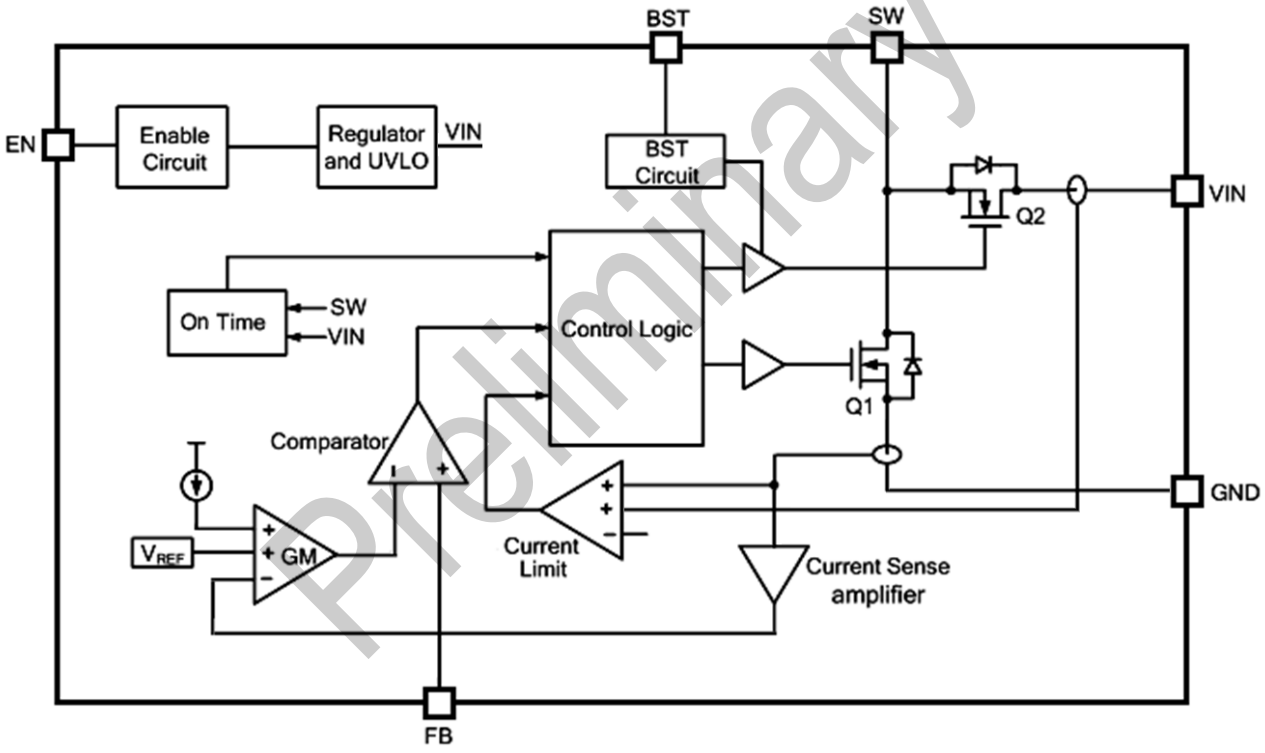
Load Transient

(Vin=12V, Vout=3.3V, Iout=0.01~2.5A)



Ch2: Vout, Ch4: I_L

BLOCK DIAGRAM



FUNCTIONAL DECRIPTIONS

Loop operation

The LC2452S is a wide input range, high-efficiency, DC-to-DC step-down switching regulator, capable of delivering up to 2.5A of output current, integrated with a 120/80mΩ synchronous MOSFET pair, eliminating the need for external diode. It uses Constant On-Time control mode scheme. An error amplifier integrates error between the FB signal and the internal reference voltage. The output of the integrator is then compared to the sum of a current-sense signal and the slope compensation ramp. This operation generates a PWM signal that modulates the duty cycle of the power MOSFETs to achieve regulation for output voltage.

Internal soft-start

The soft-start is important for many applications because it eliminates power-up initialization problems. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transient events to the input power bus.

Over-current-protection and hiccup

The LC2452S has a cycle-by-cycle over-current limit for when the inductor current peak value exceeds the set current-limit threshold. First, when the output voltage drops until FB falls below the Under-Voltage (UV) threshold (typically 200mV) to trigger a UV event, the LC2452S enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground. This greatly reduces the average short-circuit current to alleviate thermal issues and to protect the regulator. The LC2452S exits hiccup mode once the overcurrent condition is removed.

Startup and shutdown

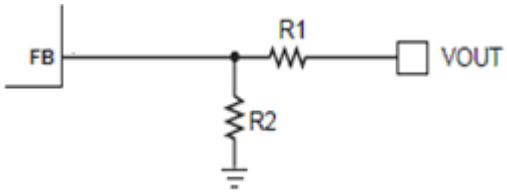
If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

APPLICATIONS INFORMATION

Setting output voltages

The external resistor divider is used to set the output voltage. The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor. R2 is then given by:

$$R_2 = \frac{R_1}{V_{out}/V_{FB} - 1}$$



Selecting the inductor

Use a 1μH-to-6.8μH inductor with a DC current rating of at least 25% higher than the maximum load current for most applications. For most designs, derive the inductance value from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{osc}}$$

Where ΔIL is the inductor ripple current. Choose an inductor current approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light-load conditions (below 100mA), use a larger inductor to improve efficiency.

Selecting the output capacitor

The output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. Use low ESR capacitors to limit the output voltage ripple. Estimate the output voltage ripple with:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \times \left[R_{ESR} + \frac{1}{8 \times f_S \times C_2}\right]$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, estimate the output voltage ripple with:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L \times C_2} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The LC2452S can be optimized for a wide range of capacitance and ESR values.

PCB LAYOUT RECOMMENDATION

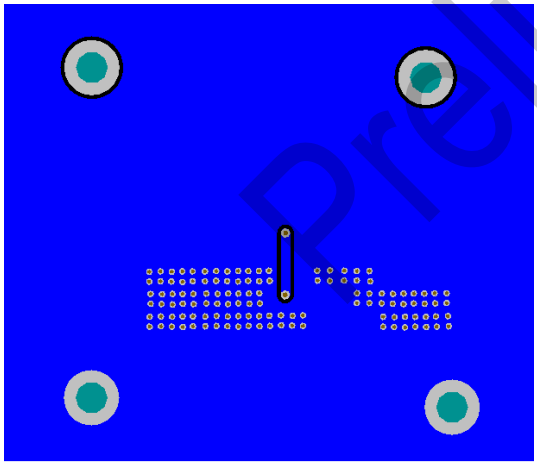
The device's performance and stability are dramatically affected by PCB layout. It is recommended to follow these general guidelines shown as below:

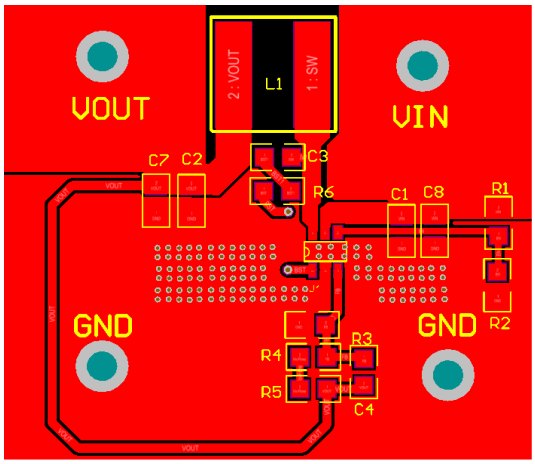
1. Place the input capacitors and output capacitors as close to the device as possible. The traces which connect to these capacitors should be as short and wide as possible to minimize parasitic inductance and resistance.

2. Place feedback resistors close to the FB pin.

3. Keep the sensitive signal (FB) away from the switching signal (SW).

4. Multi-layer PCB design is recommended.

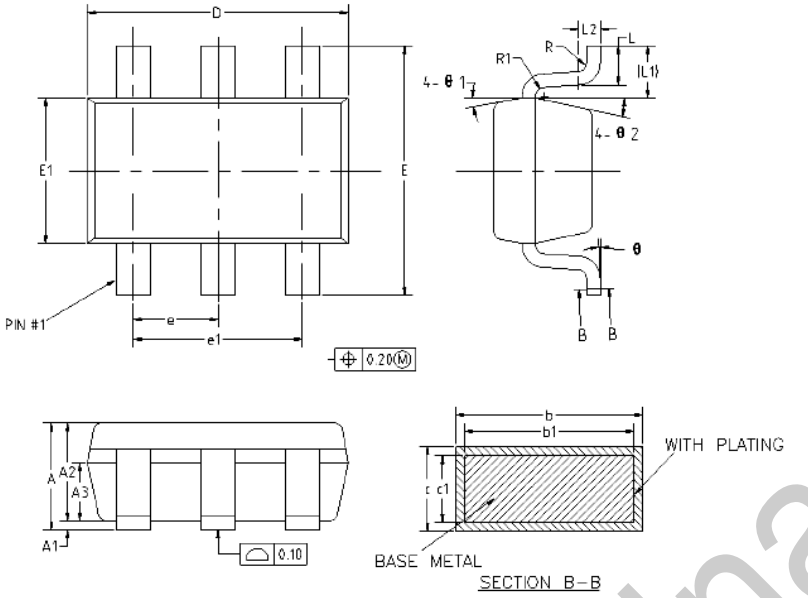




PACKAGE OUTLINE

Package	SOT23-6	Devices per reel	2500pcs

Package specification：



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.25
A1	0	–	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.36	–	0.45
b1	0.35	0.38	0.41
c	0.14	–	0.20
c1	0.14	0.15	0.16
D	2.826	2.926	3.026
E	2.60	2.80	3.00
E1	1.526	1.626	1.726
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
L	0.30	0.44	0.60
L1		0.59REF	
L2		0.25BSC	
R	0.05	–	0.20
R1	0.05	–	0.20
θ	0°	–	8°
θ 1	8°	10°	12°
θ 2	10°	12°	14°

Unit：mm