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产 品 规 格 书
Product Specification

产品名 Product **TFT-LCD OPEN CELL**

机种名 Model **LC320TU2A**

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RECORDS OF REVISION

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1. APPLICATION

This technical literature applies to the color 31.5" Wide XGA TFT-LCD LC320TU2A.

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* This module is not designed to use in dusty environment and to prevent image retention caused by long-term display of fixed pattern. So please consider items mentioned above before use and design equipment.
* In case of using the device for applications such as control and safety equipment for transportation (aircraft, trains, automobiles, etc.), rescue and security equipment and various safety related equipment which require higher reliability and safety, take into consideration that appropriate measures such as fail-safe functions and redundant system design should be taken.
* Do not use the device for equipment that requires an extreme level of reliability, such as aerospace applications, telecommunication equipment (trunk lines), nuclear power control equipment and medical or other equipment for life support.
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2. OVERVIEW

This module is color active matrix LCD Open-cell incorporating amorphous silicon TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel, driver ICs, etc. Graphics and texts can be displayed on a 1366×RGB×768 dots panel with about 16,777,216 colors(R/G/B 8bit in each color) by using LVDS(Low Voltage Differential Signaling) to interface, +12V of DC supply voltage.

In order to improve the response time of LCD, this module applies the Over Shoot driving (O/S driving) technology for the control circuit. In the O/S driving technology, signals are being applied to the Liquid Crystal according to a pre-fixed process as an image signal of the present frame when a difference is found between image signal of the previous frame and that of the current frame after comparing them.

By using the captioned process, the image signals of this LCD module are being set so that image response can be completed within one frame, as a result, image blur can be improved and clear image performance can be realized.

3. MECHANICAL TECHNICAL LITERATURES

Parameter	Technical literatures	Unit
Display size	80.039 (Diagonal)	cm
	31.5 (Diagonal)	inch
Active area	697.6845(H) x 392.256(V)	mm
Pixel Format	1366(H) x 768(V) (1pixel = R+G+B)	pixel
Pixel pitch	0.51075(H) x 0.51075 (V)	mm
Pixel configuration	R, G, B vertical stripe	
Display mode	Normally black	
Outline Dimensions (*1), (*2)	715.7(H) x455.5(V) x 4.0(D) (Open cell (with PWB))	mm
	715.7(H)×411.2(V)×1.74 (D) (Multi-cell (Without PWB))	mm
Mass	1.18±0.1	kg
Surface treatment(*2)	Anti glare Low haze (15 or less) Hard coating: 3H(CF Side)/ None(TFT Side)	

(*1) Outline dimensions are shown in Fig.3-1.Fig3-2.

(*2) This specification is without the protection film.

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4. PIXEL ARRAY AND MEMBER LOCATION

Pixel array and member located as below.
There are 4 Source Drivers (1026 input terminals S-Dr) on this panel.

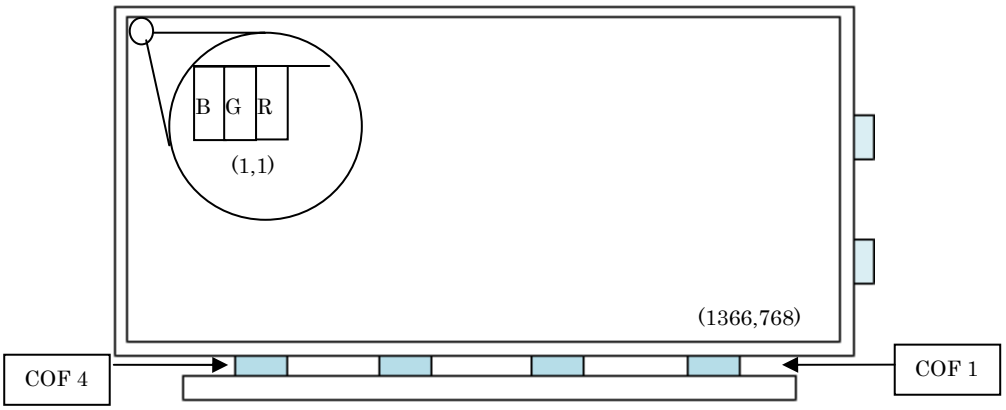

Fig.4-1 Pixel array and member location

Please use this Open Cell like following figure.

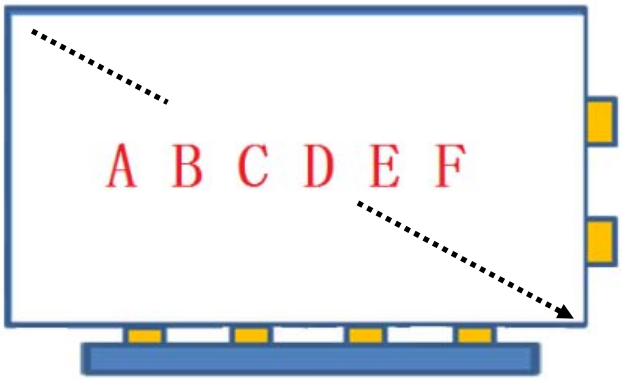

Fig.4-2 Scan direction

5. INPUT TERMINALS

5.1 TFT PANEL DRIVING

CN1 (Interface signals and +12V DC power supply) shown on the next table.
Using connector:FI-X30SSLA-HF-R2500(Japan Aviation Electronics Ind.,Ltd) or equivalent device.
Matching connector: FI-X30C2L(Japan Aviation Electronics Ind., Ltd) or equivalent device.
Matching LVDS transmitter: THC63LVDM83R (THine) or equivalent device.

Pin No.	Symbol		Remark
1	VCC	+12V Power Supply	
2	VCC	+12V Power Supply	
3	VCC	+12V Power Supply	
4	VCC	+12V Power Supply	
5	GND	Ground	
6	GND	Ground	
7	GND	Ground	
8	WP	EEPROM Write Protection (for P-Vcom) (0V~0.7V_Disable,2.7V~3.3V/Open _Enable)	
9	SELLVDS	Select LVDS data format[Note1]	Default: pull down (L:GND) [Note2]
10	Reserved	Not Available	
11	GND	Ground	
12	RIN0-	Negative(-) LVDS differential data input	LVDS
13	RIN0+	Positive(+) LVDS differential data input	LVDS

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14	GND	Ground	
15	RIN1-	Negative(-) LVDS differential data input	LVDS
16	RIN1+	Positive(+) LVDS differential data input	LVDS
17	GND	Ground	
18	RIN2-	Negative(-) LVDS differential data input	LVDS
19	RIN2+	Positive(+) LVDS differential data input	LVDS
20	GND	Ground	
21	CLKIN-	Clock Signal(-)	LVDS
22	CLKIN+	Clock Signal(+)	LVDS
23	GND	Ground	
24	RIN3-	Negative(-) LVDS differential data input	LVDS
25	RIN3+	Positive(+) LVDS differential data input	LVDS
26	GND	Ground	
27	NC	Not connection, this pin should be open.	[Note 3]
28	SCL	Serial clock input (for P-Vcom)	
29	SDA	Serial data input (for P-Vcom)	
30	GND	Ground	

[Note 1] SELLVDS

Transmitter		SELLVDS	
Pin No	Data	VESA	JEITA
		= L(GND) or Open	=H(3.3V)
51	TA0	R0(LSB)	R2
52	TA1	R1	R3
54	TA2	R2	R4
55	TA3	R3	R5
56	TA4	R4	R6
3	TA5	R5	R7(MSB)
4	TA6	G0(LSB)	G2
6	TB0	G1	G3
7	TB1	G2	G4
11	TB2	G3	G5
12	TB3	G4	G6
14	TB4	G5	G7(MSB)
15	TB5	B0(LSB)	B2
19	TB6	B1	B3
20	TC0	B2	B4
22	TC1	B3	B5
23	TC2	B4	B6
24	TC3	B5	B7(MSB)
27	TC4	NA	NA
28	TC5	NA	NA
30	TC6	DE(*)	DE(*)
50	TD0	R6	R0(LSB)
2	TD1	R7(MSB)	R1
8	TD2	G6	G0(LSB)
10	TD3	G7(MSB)	G1
16	TD4	B6	B0(LSB)
18	TD5	B7(MSB)	B1
25	TD6	NA	NA

NA: Not Available

(*)The display position is prescribed by the rise of DE (Display Enable) signal, please do not fix DE signal during operation at "High."

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[Note 2] The equivalent circuit figure of the terminal

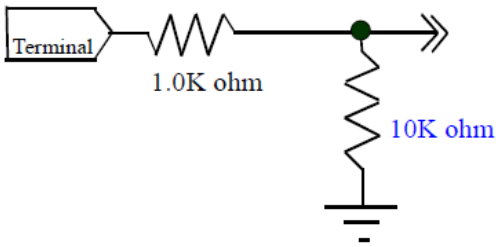

Fig.5-1 The equivalent circuit figure of the terminal

[Note 3] Built-in Self Test (BIST)

*1) PIN27=NC: Disable BIST function.
Available LVDS Signal input : Display LVDS input Pattern.
No LVDS Signal or unavailable LVDS Signal input : Display Black Pattern.

*2) PIN27=High (3.0V~3.6V) : Enable BIST function.
Available LVDS Signal input : Display LVDS input Pattern.
No LVDS Signal or unavailable LVDS Signal input : Display BIST Pattern.

5.2 INTERFACE BLOCK DIAGRAM

Corresponding Transmitter: THC63LVDM83R (THine) or equivalent device.

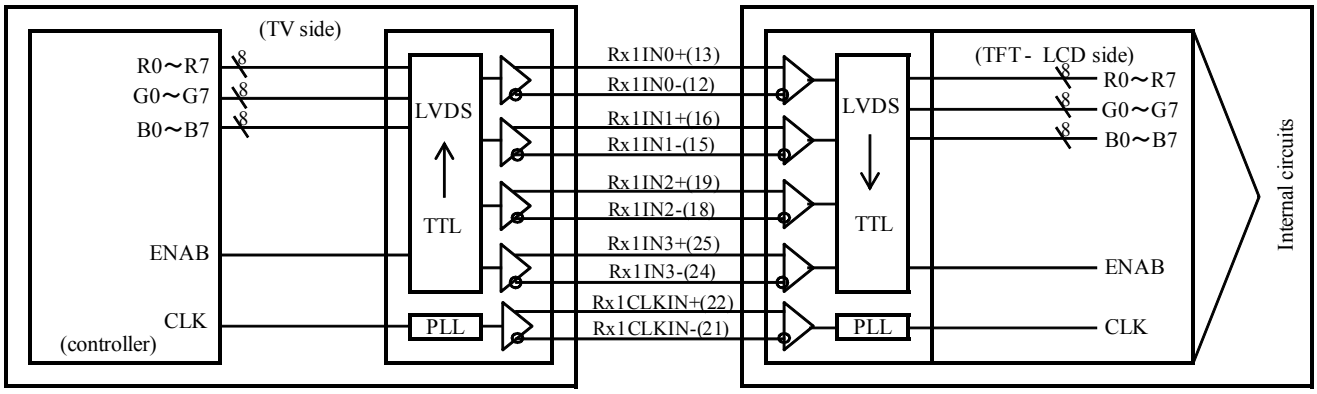

Fig.5-2 Interface block diagram

5.3 BLOCK DIAGRAM (OPEN-CELL)

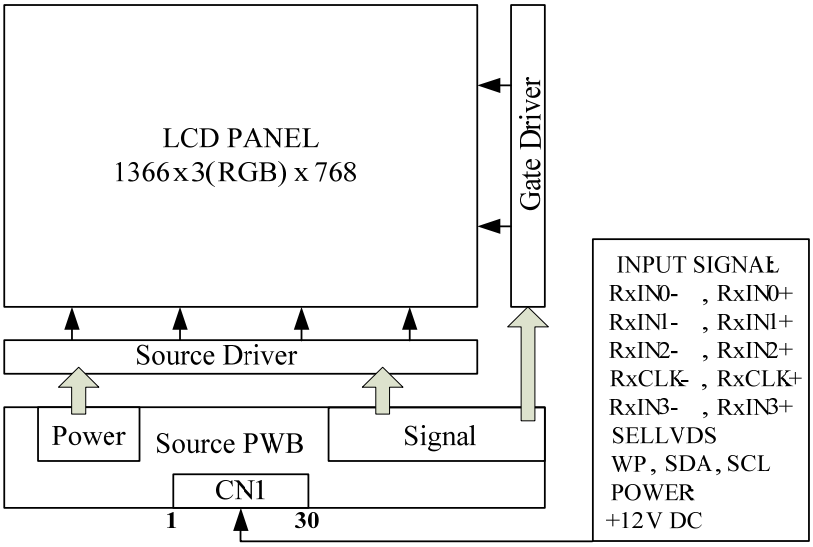

Fig.5-3 block diagram (Open-cell)

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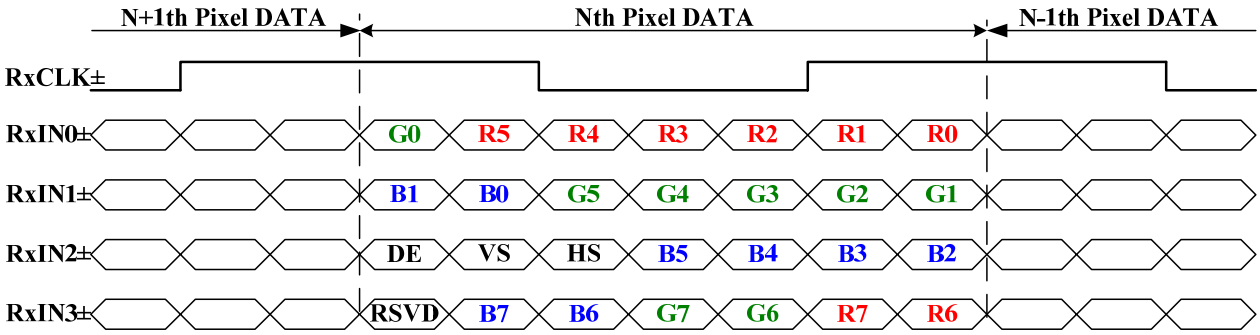
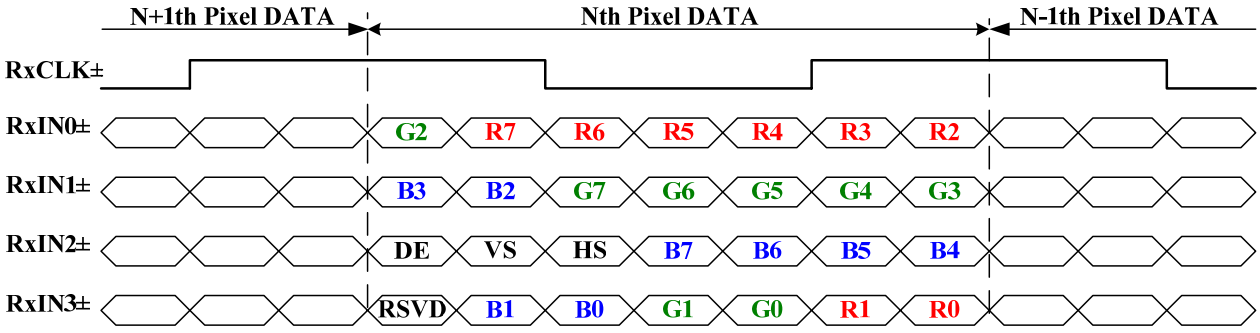
VESA Format: SELLVDS = L(GND) or OPEN(FLOATING)



JEIDA Format: SELLVDS = HIGH(3.3V)



R0~R7:Pixel R DATA(R7:MSB , R0:LSB)
G0~G7:Pixel G DATA(G7:MSB , G0:LSB)
B0~B7:Pixel B DATA(B7:MSB , B0:LSB)
DE:DATA enable Signal

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6. ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATING

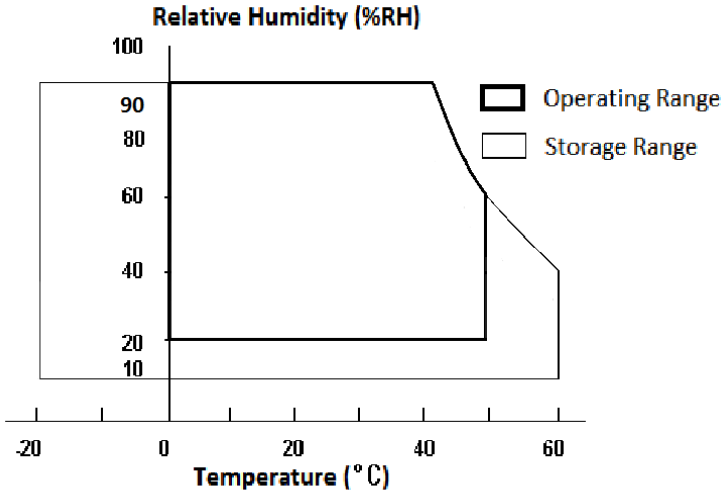
Parameter	Symbol	Condition	Ratings	Unit	Remark
Input voltage	V_I	Ta=25℃	-0.3～3.6	V	[Note 1]
+12V supply voltage	V_{CC}	Ta=25℃	0～+14	V	
Storage temperature	T_{stg}	-	-20～+60	℃	
Operation temperature	T_{opa}	-	0～+50	℃	[Note 2]

[Note 1] SELLVDS

[Note 2] Max Humidity: 90%RH. (Ta≦40℃)

Wet-bulb temperature should be 39℃Max. (Ta>40℃).

No condensation.



6.2 CONTROL CIRCUIT DRIVING

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
+12V supply voltage	Supply voltage	V_{CC}	+10.8	+12.0	+13.2	V	[Note 1]
	Current dissipation	I_{CC}	-	350	600	mA	[Note 2]
		I_{RUSH}	-	-	6	A	[Note 5]
Permissible input ripple voltage		V_{RP}	-	-	300	mVp-p	Vcc=+12.0V
Differential input threshold voltage	High	V_{TH}	100	-	-	mV	[Note 4]
	Low	V_{TL}	-	-	-100	mV	
Input Low voltage		V_{IL}	0		0.7	V	[Note 3]
Input High voltage		V_{IH}	2.7	-	3.3	V	
Input leak current (Low)		I_{IL}	-	-	400	μA	V_I=0V [Note 3]
Input leak current (High)		I_{IH}	-	-	100	μA	V_I =3.3V [Note 3]
Terminal resistor		RT	-	100	-	Ω	Differential input
Input Differential voltage		|VID|	200	400	600	mV	[Note 4]
Differential input common mode voltage		VCM	1.0	1.2	1.4	V	[Note 4]

V_{CM}: Common mode voltage of LVDS driver.

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[Note 1]

Input voltage sequences

50us ≦ t1 ≦ 20ms

0 < t2-1<50ms

0 < t2-2<50ms

0 < t3-1≦1s

0 < t3-2≦1s

1s ≦ t4

500ms ≦ t5-1

500ms ≦ t5-2

0 < t6-1

0 < t6-2

Dip conditions for supply voltage

a) 9.1V ≦ V_{CC} < 10.8V

td ≦ 10ms

b) V_{CC} < 9.1V

Dip conditions for supply voltage is based on input voltage sequence.

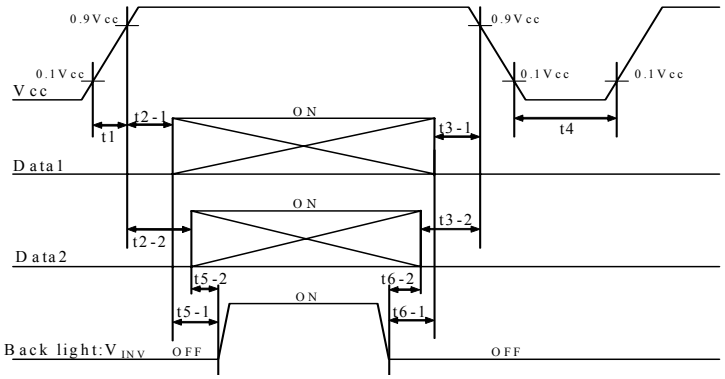

Fig. 6-1 Input voltage sequences

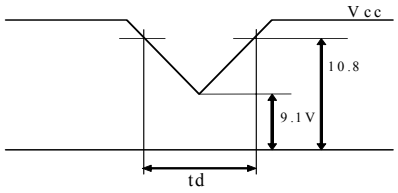

Fig. 6-2 Dip conditions for supply voltage

* Data1: CLKIN±,RIN0±,RIN1±, RIN2±, RIN3±
* Data2: SELLVDS
* About the relation between data input and back light lighting, please base on the above-mentioned input sequence.

When back light is switched on before panel operation or after a panel operation stop, it may not display normally. But this phenomenon is not based on change of an incoming signal, and does not give damage to a liquid crystal display.

[Note 2] Typical current situation: 256 gray-bar pattern (VCC = +12.0V).

The explanation of RGB gray scale is seen in section 8.

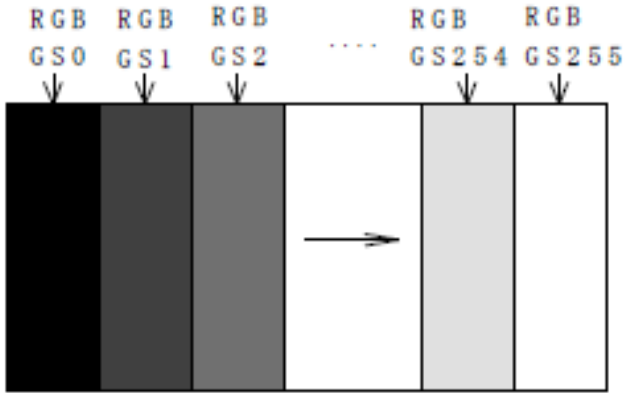

Fig. 6-3 Typical current situation

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[Note 3] SELLVDS

[Note 4] CLKIN+/CLKIN-, RIN0+/RIN0-, RIN1+/RIN1-, RIN2+/RIN2-, RIN3+/RIN3-

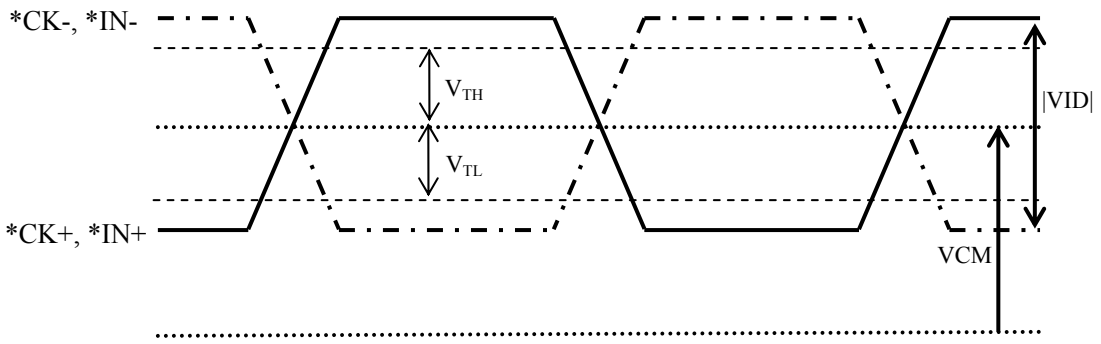
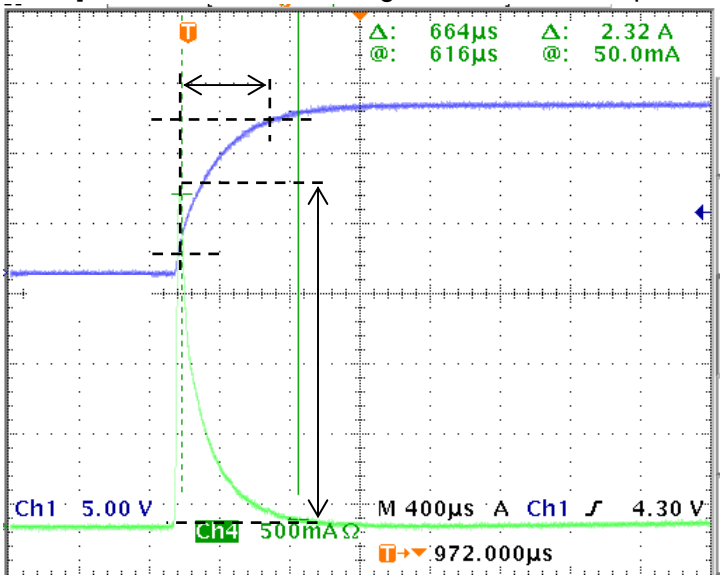


Fig. 6-4 LVDS input characteristics

[Note 5] The Rush current corrugation at the time of power on.



Ton: Vcc(+12V) Rising Time
From 10%Vcc to 90%Vcc
I: Current of Vcc(+12V)
I_{RUSH}: The max current
After Vcc rise.

[HOW TO]
Measure the Vcc(12V) when you turn the power on. At the same time, measure the current of Vcc(12V). The single mode of the oscilloscope is useful in this case.

Fig. 6-5 The waveform of rush current

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7. TIMING CHARACTERISTICS OF INPUT SIGNALS

7.1 TIMING CHARACTERISTICS

Parameter		Symbol	Min	Typ.		Max.	Unit
				NTSC	PAL		
Clock	Frequency	Fclk=1/Tc	72	82	82	85	MHz
	Spread Spectrum Modulation range	Fclk_mod	Fclk-3%	-	-	Fclk+3%	MHz
	Spread Spectrum Modulation frequency	FSSM	30	-	-	100	KHz
Data enable signal	Horizontal period	TH	1540	1696	1696	1940	clock
			17.15	20.68	20.68	21.42	μs
	Horizontal period (High)	THd	1366	1366	1366	1366	clock
	Horizontal Blanking period	TH-THd	174	330	330	574	clock
	Vertical period	TV	778	806	967	972	line
			47.7	60	50	62.35	Hz
	Vertical period (High)	TVd	768	768	768	768	line
	Vertical Blanking period	TV-TVd	10	38	199	204	line

*Timing diagrams of input signal are shown in Fig. 7-1.
* SSCG (Spread spectrum clock generator) is defined as Fig. 7-2.

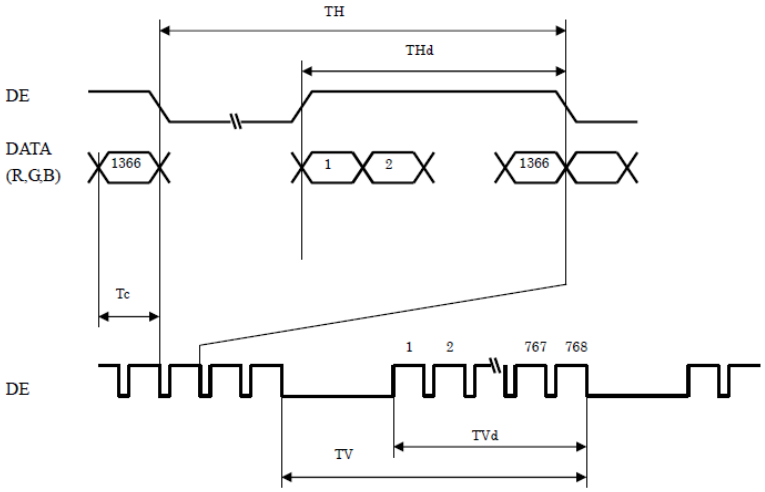

Fig.7-1 Timing characteristics of input signals

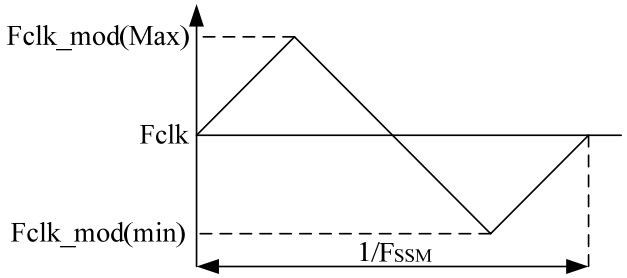

Fig.7-2 Spread spectrum clock generator

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7.2 LVDS SIGNAL CHARACTERISTICS

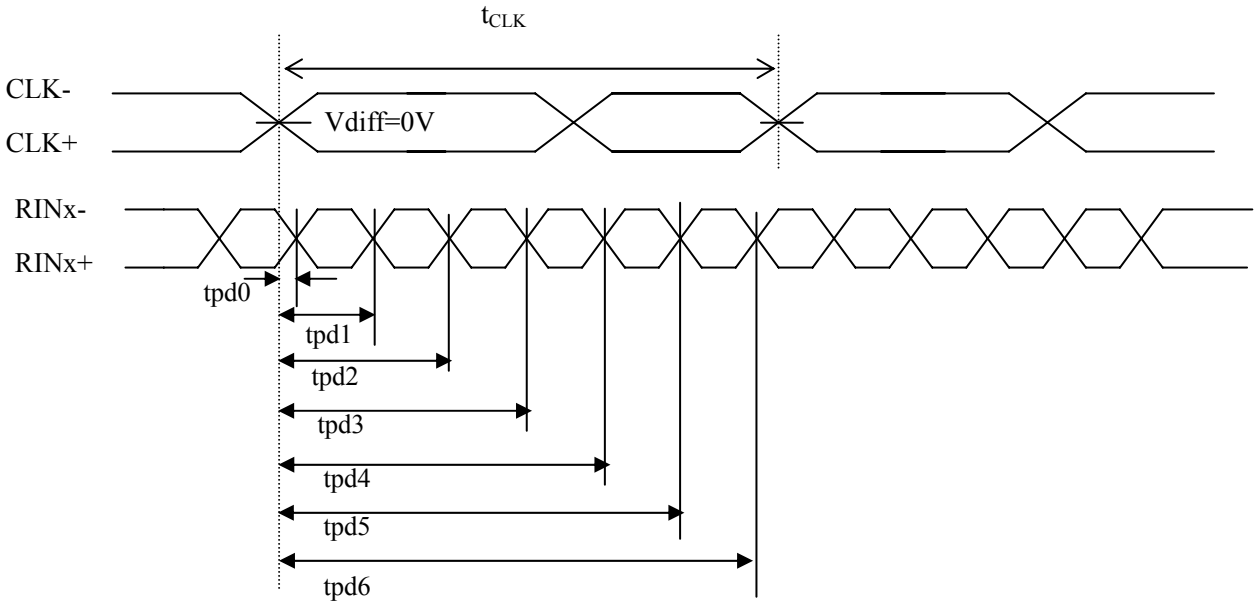

Fig.7-3 LVDS signal characteristics

The item		Symbol	min.	typ.	Max.	unit
Data position	Delay time, CLK rising edge to serial bit position 0	tpd0	-0.40	0	0.40	ns
	Delay time, CLK rising edge to serial bit position 1	tpd1	typ-0.40	1* t_{CLK} /7	typ+0.40	
	Delay time, CLK rising edge to serial bit position 2	tpd2	typ-0.40	2* t_{CLK} /7	typ+0.40	
	Delay time, CLK rising edge to serial bit position 3	tpd3	typ-0.40	3* t_{CLK} /7	typ+0.40	
	Delay time, CLK rising edge to serial bit position 4	tpd4	typ-0.40	4* t_{CLK} /7	typ+0.40	
	Delay time, CLK rising edge to serial bit position 5	tpd5	typ-0.40	5* t_{CLK} /7	typ+0.40	
	Delay time, CLK rising edge to serial bit position 6	tpd6	typ-0.40	6* t_{CLK} /7	typ+0.40	

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8. INPUT SIGNAL, BASIC DISPLAY COLORS AND GRAY SCALE OF EACH COLOR

	Colors & Gray scale	Gray Scale	Data signal																									
			R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	B3	B4	B5	B6	B7
Basic Color	Black	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	–	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	–	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	–	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	–	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓					↓								↓								↓			
	⇩	↓					↓								↓								↓			
	Brighter	GS253	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇩	GS254	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓					↓								↓								↓			
	⇩	↓					↓								↓								↓			
	Brighter	GS253	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	⇩	GS254	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Green	GS255	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale of Blue	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	⇧	↓					↓								↓								↓			
	⇩	↓					↓								↓								↓			
	Brighter	GS253	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1
	⇩	GS254	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	Blue	GS255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Fig.8-1 Input Signal

0: Low level voltage,

1: High level voltage.

Each basic color can be displayed in 256 gray scales from 8 bit data signals. According to the combination of total 24 bit data signals, the 16,777,216 colors display can be achieved on the screen.

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9. OPTICAL CHARACTERISTICS

Ta=25°C

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range	Horizontal	θ21 θ22	CR≥10	-	88	-	Deg.	[Note1,4]
	Vertical	θ11 θ12		-	88	-	Deg.	
Contrast ratio		CR	θ=0 deg.	-	5000	-	-	[Note2,4]
Response time		τ_{DRV}		-	7	-	ms	[Note3,4,5]
Chromaticity of white		x		Typ-0.03	0.280	Typ+0.03	-	[Note 4]
		y			0.290		-	
Chromaticity of red		x			0.646		-	
		y			0.346		-	
Chromaticity of green		x			0.305		-	
		y			0.624		-	
Chromaticity of blue		x			0.150		-	
		y			0.075		-	
White variation		δW	-	-	-	1.3	-	[Note 6]
Crosstalk		CT			4		%	[Note 7]

*The measurement shall be executed 60 minutes after lighting at rating.
*These values are measured with CPL LED back light unit.
*The optical characteristics are measured using the following equipment.

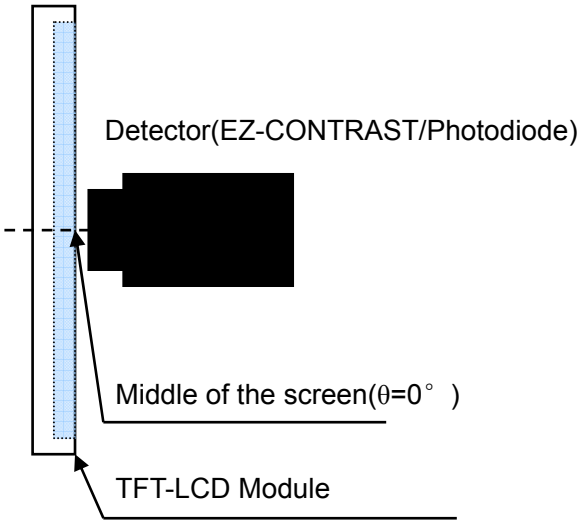

Fig.9-1 Measurement of Viewing angle range and Response time.
(Viewing angle range: EZ-CONTRAST, Response time: Photodiode)

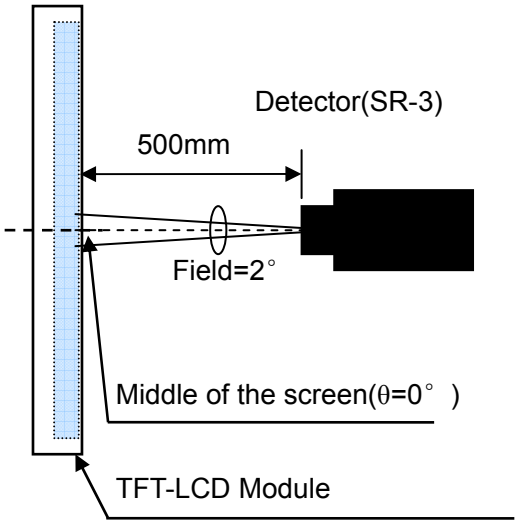

Fig.9-2 Measurement of Contrast, Luminance, Chromaticity, White variation

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[Note 1] Definitions of viewing angle range:

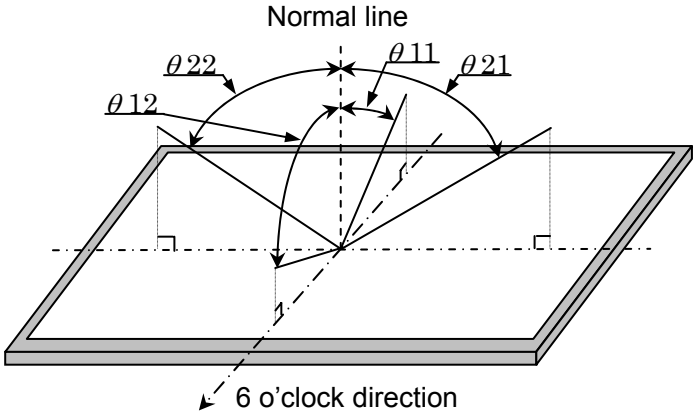

Fig.9-3 Viewing angle

[Note 2] Definition of contrast ratio:

The contrast ratio is defined as the following.

$$\text{Contrast Ratio} = \frac{\text{Luminance (Brightness) with white screen}}{\text{Luminance (Brightness) with black screen}}$$

[Note 3] Definition of response time

The response time (τ_{DRV}) is defined as the following figure and shall be measured by switching the input signal for "any level of gray (0%, 25%, 50%, 75% and 100%) and "any level of gray (0%, 25%, 50%, 75% and 100%).

	0%	25%	50%	75%	100%
0%		τ_r:0%–25%	τ_r:0%–50%	τ_r:0%–75%	τ_r:0%–100%
25%	τ_d:25%–0%		τ_r:25%–50%	τ_r:25%–75%	τ_r:25%–100%
50%	τ_d:50%–0%	τ_d:50%–25%		τ_r:50%–75%	τ_r:50%–100%
75%	τ_d:75%–0%	τ_d:75%–25%	τ_d:75%–50%		τ_r:75%–100%
100%	τ_d:100%–0%	τ_d:100%–25%	τ_d:100%–50%	τ_d:100%–75%	

τ*:x-y...response time from level of gray(x) to level of gray(y)

$\tau_{DRV} = \Sigma (\tau$*:x-y)/20

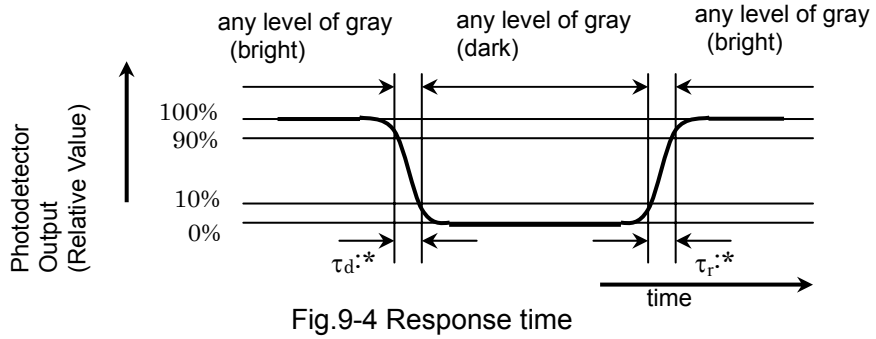

Fig.9-4 Response time

[Note 4] This shall be measured at center of the screen.

When black brightness is a max value, the specification of the contrast is satisfied.

[Note 5] This value is valid when O/S driving is used at typical input time value.

[Note 6] Definition of white variation:

White variation is defined as the following with five measurements. (A～E)

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$$\delta w = \frac{\text{Maximum luminance of five points (brightness)}}{\text{Minimum luminance of five points (brightness)}}$$

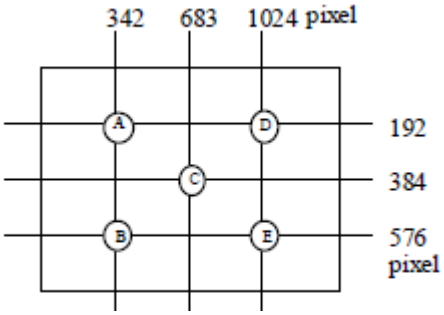

Fig.9-5 measurement locations of white variation

[Note 7] Definition of Crosstalk(CT):

$CT=|Y_B - Y_A| / Y_A \times 100(\%)$

Where:

Y_A=Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B=Luminance of measured location with gray level 0 pattern (cd/m^2)

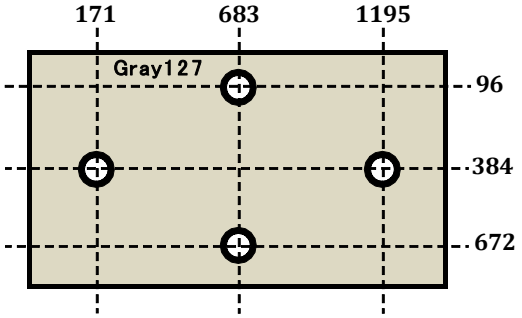

Fig.9-6 measurement locations of Y_A

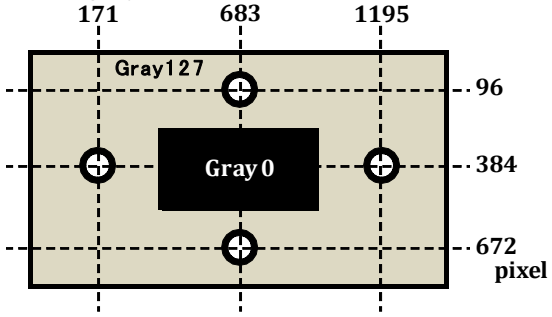

Fig.9-7 measurement locations of Y_B

10. HANDLING PRECAUTIONS OF THE OPEN-CELL

a) Be sure to turn off the power supply when inserting or disconnecting the cable.
b) Be sure to design the cabinet so that the module can be installed without any extra stress such as warp or twist.
c) Since the front polarizer is easily damaged, pay attention not to scratch it.
d) Since long contact with water may cause discoloration or spots, wipe off water drop immediately.
e) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
f) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface. Handle with care.
g) Since CMOS LSI is used in this module, take care of static electricity and take the human earth into consideration when handling.
h) The module has a printed circuit boards (PCB) on the back side, take care to keep it from any stress or pressure when handling or installing the module; otherwise some of electronic parts on the PCB may be damaged.
i) Observe all other precautionary requirements in handling components.
j) When some pressure is added onto the module from rear side constantly, it causes display non-uniformity issue, functional defect, etc. So, please avoid such design.
k) When giving a touch to the panel at power on supply, it may cause some kinds of degradation. In that case, once turn off the power supply, and turn on after several seconds again, and that is disappear.
l) When handling LCD modules and assembling them into cabinets, please be noted that long-term storage in the environment of oxidization or deoxidization gas and the use of such materials as reagent, solvent, adhesive, resin, etc. which generate these gasses, may cause corrosion and discoloration of the LCD modules.
m) This LCD module is designed to prevent dust from entering into it. However, there would be a possibility to have a bad effect on display performance in case of having dust inside of LCD module. Therefore, please ensure to design your TV set to keep dust away around LCD module.

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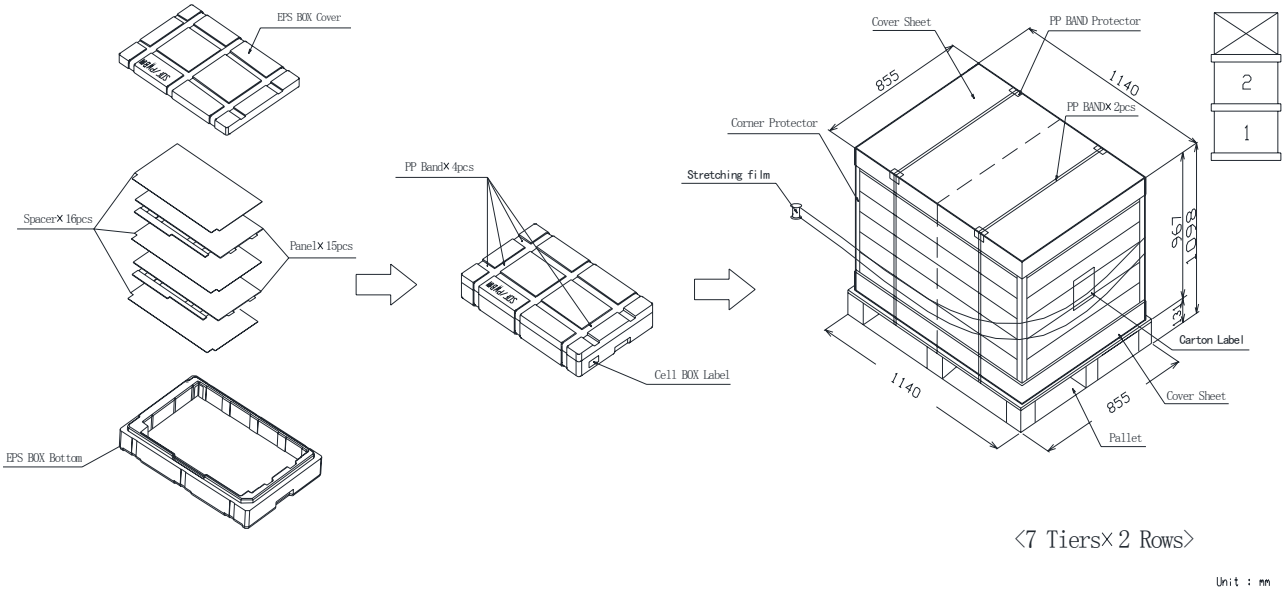
11. PACKING FORM

(a)Piling number of Pallet	: 14 cell boxes/1 pallet
(b)Packing quantity in one EPS BOX	: 15 pcs
(c)EPS BOX size	: 829(L)×557(W)×141(H) mm
(d)Pallet size	: 1140(L)×855(W)×131(H) mm
(e)Pallet size after packing(with 14 boxes)	: 1140(L)×855(W)×1098(H) mm
(f) Total mass of one pallet filled with full open-cell	: MAX 330 kg



12. RELIABILITY TEST ITEM

No.	Test item	Condition
1	High temperature storage test	Ta= 60°C 240h
2	Low temperature storage test	Ta=-20°C 240h
3	High temperature and high humidity operation test	Ta= 50°C ; 80%RH 240h (No condensation)
4	High temperature operation test	Ta= 50°C 240h
5	Low temperature operation test	Ta= 0°C 240h
6	Thermal shock test	-20℃/30mins, 60℃/30mins, 100 cycles
7	Package vibration test	Wave form：Random Vibration level：1.0 Grms Frequency：5-50 Hz Duration：X,Y,Z each direction per 10mins
8	Package drop test	Height：15cm (2 edges, 1 surface)
9	ESD	At the following conditions, it is a thing without incorrect operation and destruction. Both under Contact and Non-contact conditions, apply electric discharge ±300V to the input terminal. condition:200pF 0Ω under non-operation.

[Result evaluation criteria]
Under the display quality test condition with normal operation state, there shall be no change, which may affect practical display function.

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13. OTHERS

a) Panel label

a-1) The label of Multi-cell which is stuck on the front side of the panel.

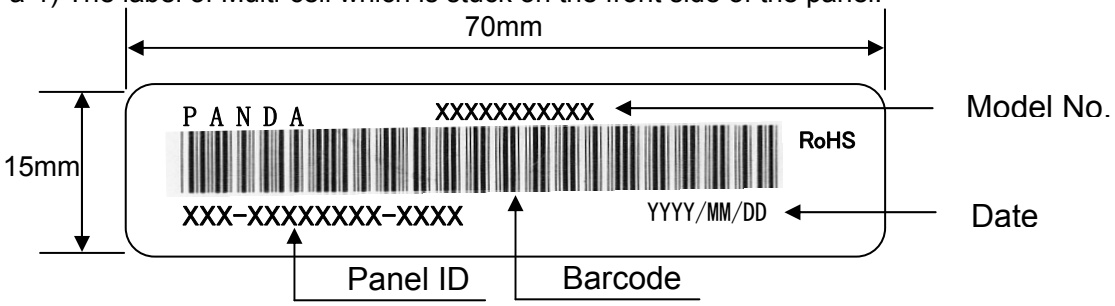


Fig.13-1 Multi-cell label

a-2) The label of Open-cell which is stuck on component side of the PWB.

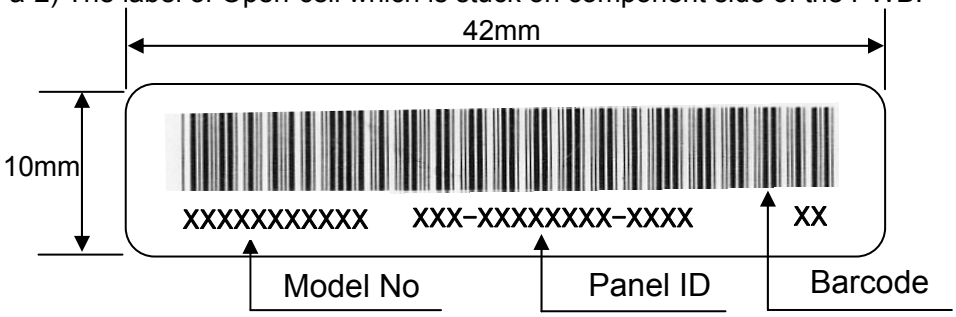
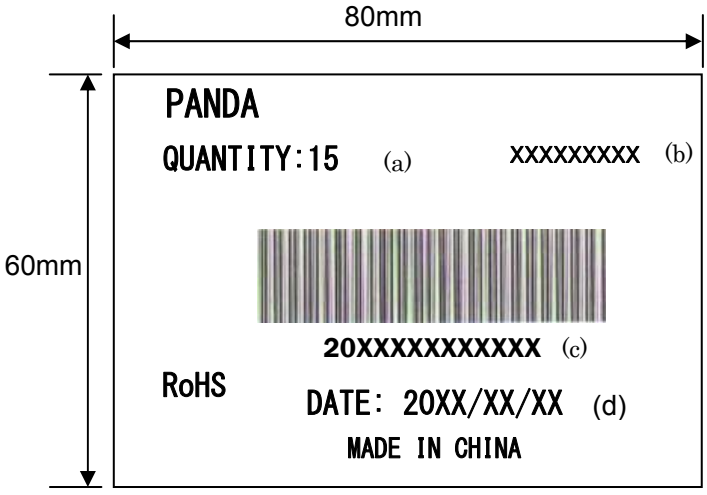


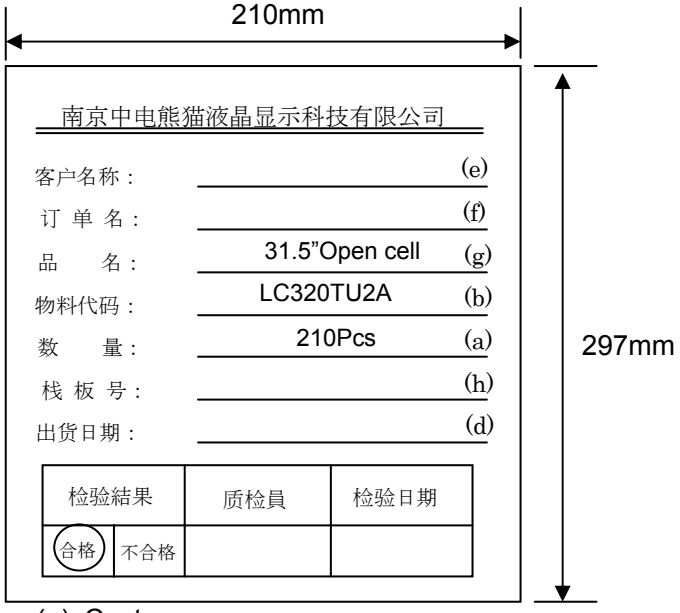
Fig.13-2 Open-cell label

b) Packing label

b-1) EPS BOX



b-2) Pallet



(a) Quantity
(b) Model No.
(c) Box ID
(d) Date

(e) Customer name
(f) Order No.
(g) Name of products
(h) Pallet No.

Fig.13-3 Packing label

c) Adjusting volume has been set optimally before shipment, so do not change any adjusted value. If adjusted value is changed, the specification may not be satisfied.

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d) Disassembling the module can cause permanent damage and should be strictly avoided.

e) Please be careful since image retention may occur when a fixed pattern is displayed for a long time.

f) The chemical compound, which causes the destruction of ozone layer, is not being used.

g) When any question or issue occurs, it shall be solved by mutual discussion.

h) Regulation to utilize an ozone depletion chemical substance.
Restricted substance : CFCs, halon, carbon, tertrachloide, and 1,1,1-trichloroethane
This product don't include the above matter.
Production process of this product and parts don't include above matter.

14. EPS BOX STORAGE CONDITION

Temperature: 0°C to 40°C
Humidity: 80%RH or less
Reference condition: 20°C to 35°C, 80%RH or less (summer)
5°C to 15°C, 80%RH or less (winter)
The total storage time (40°C, 80%RH): 240h or less
Sunlight: Be sure to shelter a product from the direct sunlight.
Atmosphere: Harmful gas, such as acid and alkali which bites electronic components and/or wires must not be detected.
Be sure to put cartons on palette or base, don't put it on floor, and store them with removing from wall. Please take care of ventilation in storehouse and around cartons, and control changing temperature is within limits of natural environment.
Storage life 1 year

15. PRECAUTIONS

a) Because the Open-Cell is too weak to destroy by static electricity, please don't touch the terminal with bare hands.
b) Front polarizer can easily be damaged. Pay attention on it.
c) Since long contact with drops of water may cause discoloration or spots, please wipe off them as soon as possible.
d) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
e) The Panel will be broken or chipped when it is dropped or bumped against a hard substance.
f) Precautions of peeling off the Protection film:
- Be sure to peel off slowly (recommended more than 7 sec.) and constant speed.
- Peeling direction shown in the Fig. 15-1.
- Be sure to ground person with adequate methods such as the anti-static wrist band.
- Be sure to connect PWB to GND while peeling off the protection film.
- Ionized air should be blown to the surface while peeling off the protection film.
- The protection film must not touch drivers and PWB.
- After the protection film has been peeled off, some adhesive may be remained on the polarizer. Please use isopropyl-alcohol to remove it.

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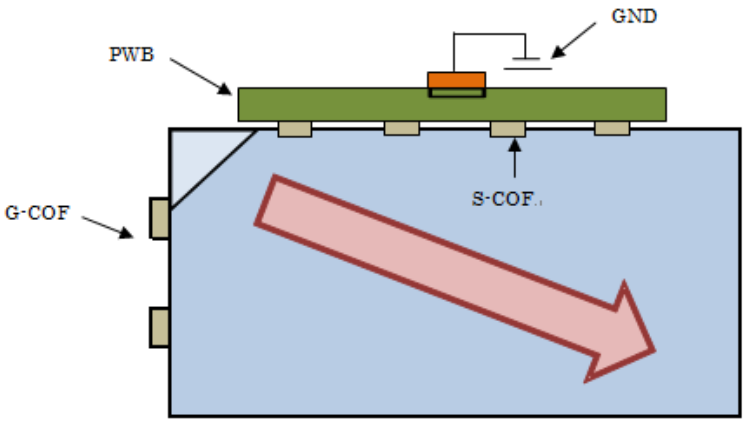

Fig.15-1 Direction of peeling off

g) Since the Open-cell consists of TFT and electronic circuits with CMOS-ICs, which are very weak to electrostatic discharge, persons who are handling an Open-Cell should be grounded though adequate methods such as an anti-static wrist band. Connector pins should not be touched directly with bare hands.
Reference: Process control standard of CPL.

	item	Management standard value and performance standard
1	Anti-static mat(shelf)	1to50[Mega ohm]
2	Anti-static mat(floor, desk)	1to100[Mega ohm]
3	Ionizer	Attenuate from ±1000V to ±100V within two seconds.
4	Anti-static wrist band	0.8 to 10 [Mega ohm]
5	Anti-static wrist band entry and ground resistance	Below 1000[ohm]
6	Temperature	22 to 26 [℃]
7	Humidity	60 to 70 [%]

h) Since the Open-cell has a PWB, please take care to keep it off any stress or pressure when handling or installing the Open-cell, otherwise some of electronic parts on it may be damaged.
i) Be sure to turn off the power supply when inserting or disconnecting the cable.
j) Be sure to design the module and cabinet so that the Open-cell van is installed without any extra stress such as warp or twist.
k) When handling and assembling Open-Cell into module, please be noted that long-term storage in the environment of oxidization or deoxidization gas and the use of materials such as reagent, solvent, adhesive, resin, etc. which generate these gasses, may cause corrosion and discoloration of the Open-Cell.
l) Applying too much force and stress to PWB and drivers may cause a malfunction electrically and mechanically.
m) The Open-cell has high frequency circuits. Sufficient suppression to EMI should be done by system manufactures.
n) Please be careful since image retention may occur when a fixed pattern is displayed for a long time.
o) The chemical compound, which causes the destruction of ozone layer, is not being used.
p) This Open-Cell module is corresponded to RoHS.
q) When any question or issue occurs, it shall be solved by mutual discussion.

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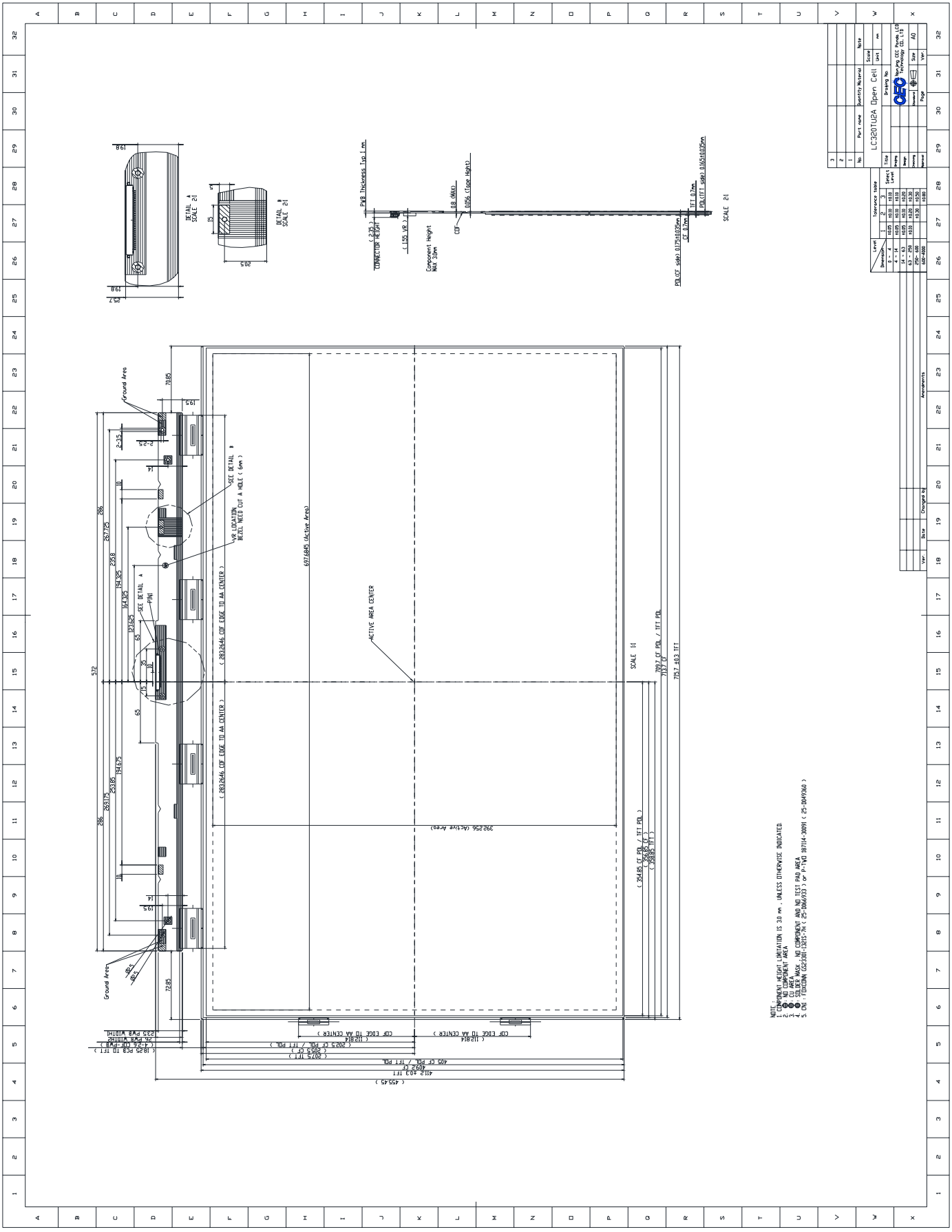

Fig.3-1. Front outline drawing

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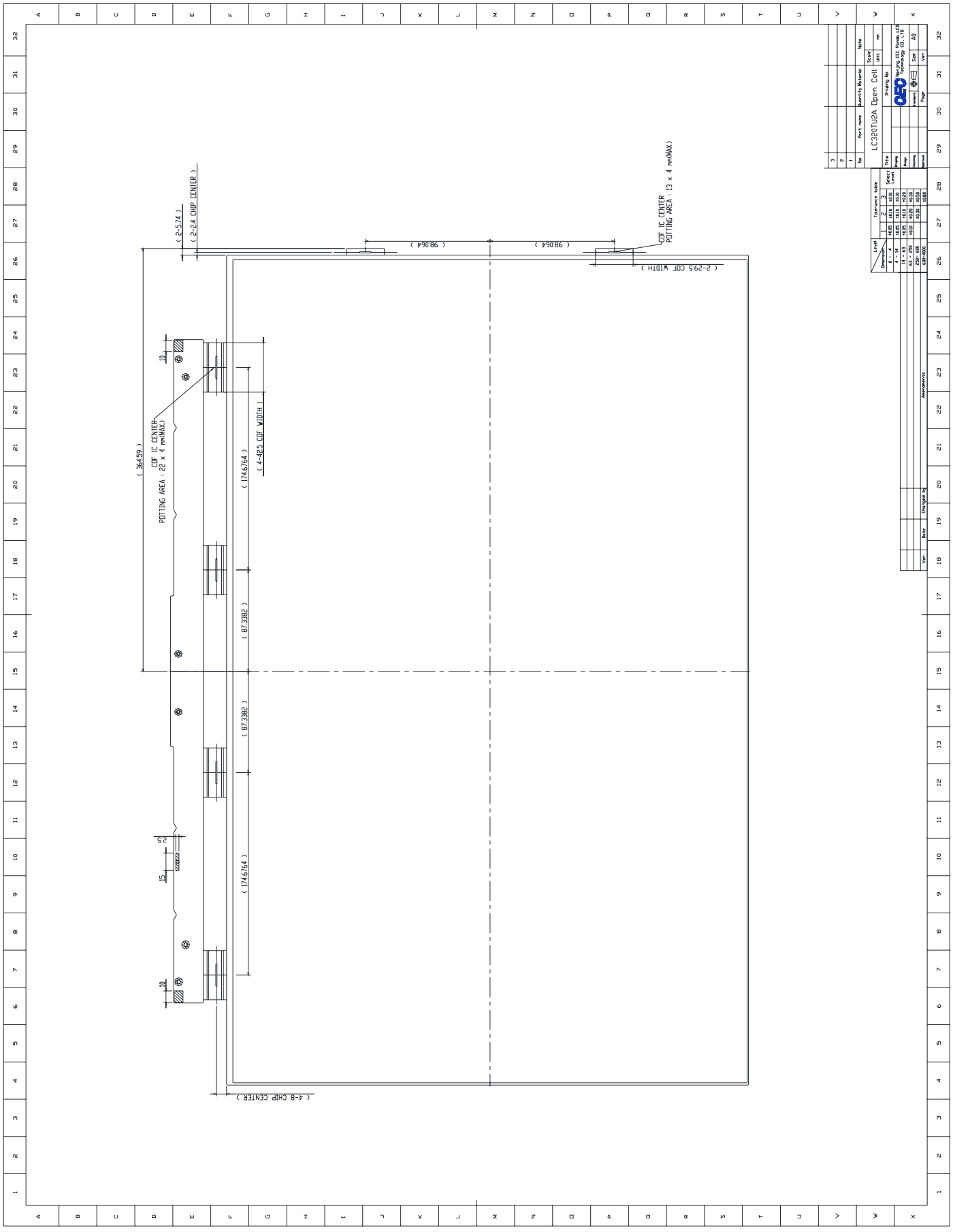

Fig.3-2. Back outline drawing

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