Ordering number : EN4795C

CMOS LSI

LC321664AJ, AM, AT-80

1 MEG (65536 words × 16 bits) DRAM
Fast Page Mode, Byte Write

Overview

The LC321664AJ, AM, AT is a CMOS dynamic RAM operating on a single 5 V power source and having a 65536-word × 16-bit configuration. Equipped with large capacity capabilities, high-speed transfer rates and low power dissipation, this series is suited for a wide variety of applications ranging from computer main memory and expansion memory to commercial equipment.
Address input utilizes a multiplexed address bus which permits it to be enclosed in compact plastic packages of SOJ 40-pin, SOP 40-pin and TSOP 44-pin. Refresh rates are within 4 ms with 256 row address (A0 to A7) selection and support $\overline{RAS}$-only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh and hidden refresh settings.
There are functions such as page mode, read-modify-write, and byte-write.

Features

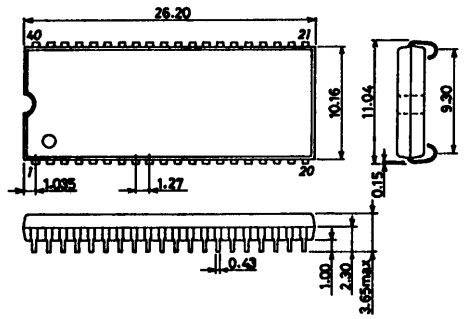
- 65536-word × 16-bit configuration
- Single 5 V ±10% power supply
- All input and output (I/O) TTL compatible
- Supports fast page mode, read-modify-write, and byte-write.
- Supports output caching control using early write and Output Enable ($\overline{OE}$) control.
- 4 ms refresh using 256 refresh cycles
- Supports $\overline{RAS}$-only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh and hidden refresh.
- Packages
  SOJ 40-pin (400 mil) plastic package: LC321664AJ
  SOP 40-pin (525 mil) plastic package: LC321664AM
  TSOP 44-pin (400 mil) plastic package: LC321664AT
- $\overline{RAS}$ access time/column address access time/$\overline{CAS}$ access time/ cycle time/power dissipation

Package Dimensions

unit: mm

3200-SOJ40

[LC321664AJ]

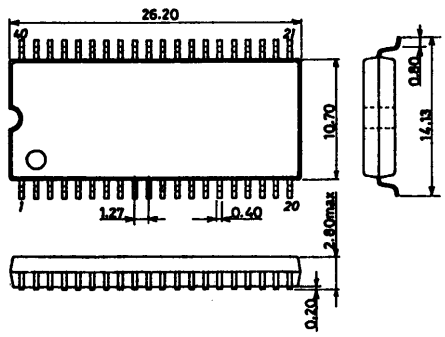


SANYO:SOJ40

unit : mm

3195-SOP40

[LC321664AM]



SANYO:SOP40

Parameter		LC321664AJ, AM, AT-80
$\overline{RAS}$ access time		80 ns
Column address access time		45 ns
$\overline{CAS}$ access time		30 ns
Cycle time		135 ns
Power dissipation (max.)	During operation	633 mW
	During standby	5.5 mW (CMOS level)/11 mW (TTL level)

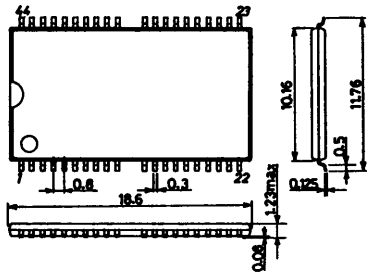
SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-0005 JAPAN

Package Dimensions

unit : mm

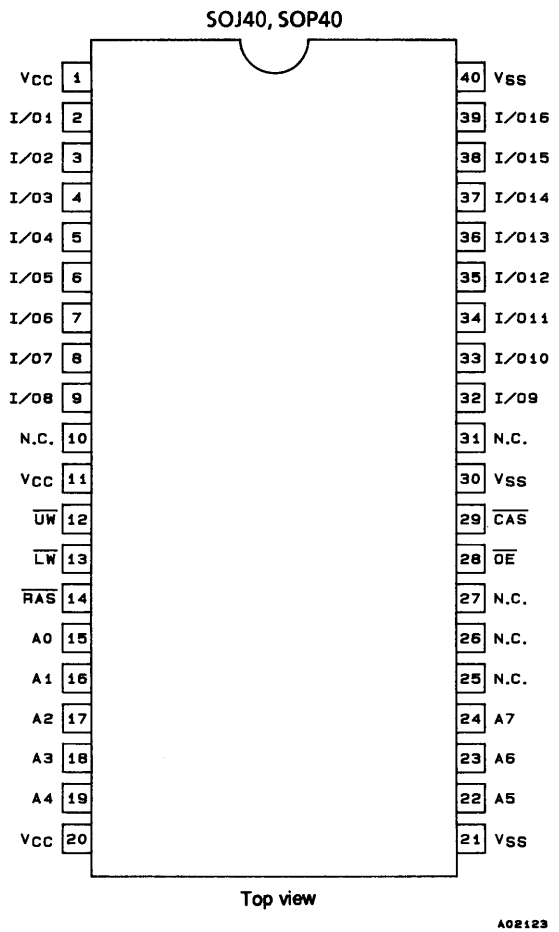
3207-TSOP44

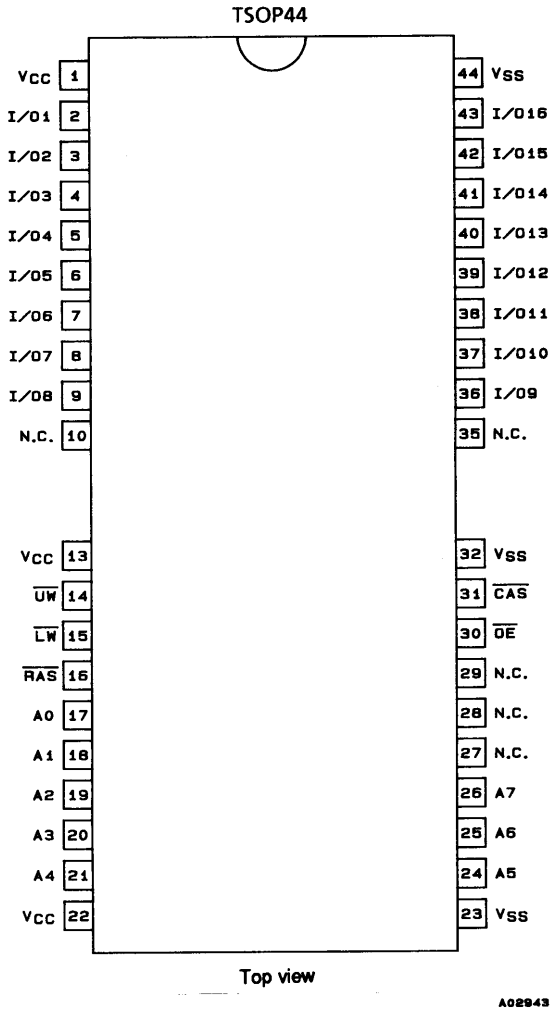
[LC321664AT]



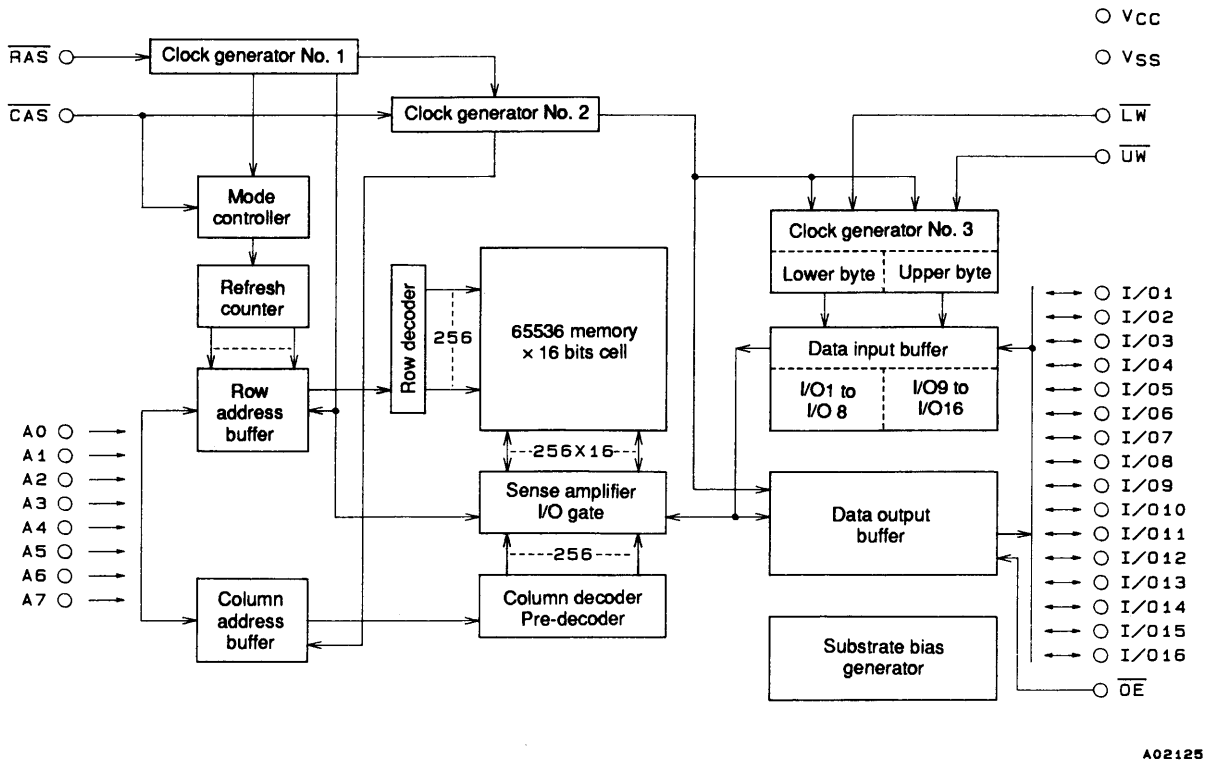
SANYO:TSOP44 (TYPE-II)

Pin Assignments





Block Diagram



Specifications

Absolute Maximum Ratings

Parameter		Symbol	Ratings	Unit	Note
Maximum supply voltage		V_{CC} max	–1.0 to +7.0	V	1
Input voltage		V_{IN}	–1.0 to +7.0	V	1
Output voltage		V_{OUT}	–1.0 to +7.0	V	1
Allowable power dissipation	LC321664AJ, AM	Pd max	800	mW	1
	LC321664AT		700		
Output short-circuit current		I_{OUT}	50	mA	1
Operating temperature range		Topr	0 to +70	°C	1
Storage temperature range		Tstg	–55 to +150	°C	1

Note: 1) Stresses greater than the above listed maximum values may result in damage to the device.

DC Recommended Operating Ranges at Ta = 0 to +70°C

Parameter	Symbol	min	typ	max	Unit	Note
Power supply voltage	V_{CC}	4.5	5.0	5.5	V	2
Input high level voltage	V_{IH}	2.4		6.5	V	2
Input low level voltage (A0 to A7, $\overline{RAS}$, $\overline{CAS}$, $\overline{UW}$, $\overline{LW}$, $\overline{OE}$)	V_{IL}	–1.0*		+0.8	V	2
Input low level voltage (I/O1 to I/O16)	V_{IL}	–0.5*		+0.8	V	2

Note: 2) All voltages are referenced to V_{SS}.
A bypass capacitor of about 0.1 µF should be connected between V_{CC} and V_{SS} of the device.
* –2.0 V when pulse width is less than 20 ns

DC Electrical Characteristics at Ta = 0 to + 70°C, V_{CC} = 5 V ± 10%

Parameter	Symbol	Conditions	min	max	Unit	Note
Operating current (Average current during operation)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$, address cycling: $t_{RC} = t_{RC}$ min		115	mA	3, 4, 5
Standby current	I_{CC2}	$\overline{RAS} = \overline{CAS} = V_{IH}$		2	mA	
$\overline{RAS}$-only refresh current	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC}$ min		115	mA	3, 5
Fast page mode current	I_{CC4}	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ address cycling: $t_{PC} = t_{PC}$ min		70	mA	3, 4, 5
Standby current	I_{CC5}	$\overline{RAS} = \overline{CAS} = V_{CC}$–0.2V		1	mA	
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	$\overline{RAS}$, $\overline{CAS}$ cycling: $t_{RC} = t_{RC}$ min		115	mA	3
Input leakage current	I_{IL}	$0V \le V_{IN} \le 6.5V$, pins other than measuring pin = 0V	–10	+10	µA	
Output leakage current	I_{OL}	D_{OUT} disable, $0V \le V_{OUT} \le 5.5V$	–10	+10	µA	
Output high level voltage	V_{OH}	I_{OUT} = –2.5mA	2.4		V	
Output low level voltage	V_{OL}	I_{OUT} = 2.1mA		0.4	V	

Note: 3) All current values are measured at minimum cycle rate. Since current flows immoderately, if cycle time is longer than shown here value becomes smaller.

4) I_{CC1} and I_{CC4} are dependent on output loads. Maximum values for I_{CC1} and I_{CC4} represent values with output open.

5) One address change can be performed while $\overline{RAS} = V_{IL}$ (I_{CC1} and I_{CC3}).
One address change can be performed during one t_{PC} cycle (I_{CC4}).

AC Electrical Characteristics at Ta = 0 to +70°C, V_{CC} = 5 V ± 10% (Note 6, 7, 8)

Parameter	Symbol	min	max	Unit	Note
Random read or write cycle time	t_{RC}	135		ns	
Read-write/read-modify-write cycle time	t_{RWC}	180		ns	
Fast page mode cycle time	t_{PC}	55		ns	
Fast page mode Read-write/read-modify-write cycle time	t_{PRWC}	100		ns	
$\overline{RAS}$ access time	t_{RAC}		80	ns	9, 14 15
$\overline{CAS}$ access time	t_{CAC}		30	ns	9, 14
Column address access time	t_{AA}		45	ns	9, 15
$\overline{CAS}$ precharge access time	t_{CPA}		50	ns	9
Output low-impedance time from $\overline{CAS}$ low	t_{CLZ}	0		ns	9
Output buffer turn-off delay time	t_{OFF}	0	20	ns	10
Rise or fall time	t_T	3	50	ns	
$\overline{RAS}$ precharge time	t_{RP}	45		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	ns	
$\overline{RAS}$ pulse width for fast page mode only	t_{RASP}	80	100000	ns	
$\overline{RAS}$ hold time	t_{RSH}	30		ns	
$\overline{CAS}$ hold time	t_{CSH}	80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	30	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	50	ns	14
$\overline{RAS}$ to column address delay time	t_{RAD}	17	35	ns	15
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		ns	
$\overline{CAS}$ precharge time	t_{CP}	10		ns	
Row address setup time	t_{ASR}	0		ns	
Row address hold time	t_{RAH}	12		ns	
Column address setup time	t_{ASC}	0		ns	
Column address hold time	t_{CAH}	20		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	60		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	45		ns	
Read command setup time	t_{RCS}	0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		ns	11
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		ns	11
Write command hold time	t_{WCH}	15		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	60		ns	
Write command pulse width	t_{WP}	15		ns	

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Parameter	Symbol	min	max	Unit	Note
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		ns	
Data input setup time	t_{DS}	0		ns	12
Data input hold time	t_{DH}	20		ns	12
Data input hold time referenced to $\overline{RAS}$	t_{DHR}	60		ns	
Refresh period	t_{REF}		4	ms	
Write command setup time	t_{WCS}	0		ns	13
$\overline{CAS}$ to $\overline{UW}$, $\overline{LW}$ delay time	t_{CWD}	50		ns	13
$\overline{RAS}$ to $\overline{UW}$, $\overline{LW}$ delay time	t_{RWD}	100		ns	13
Column address to $\overline{UW}$, $\overline{LW}$ delay time	t_{AWD}	65		ns	13
$\overline{CAS}$ precharge to $\overline{UW}$, $\overline{LW}$ delay time (fast page mode cycle only)	t_{CPWD}	70		ns	13
$\overline{CAS}$ setup time for $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_{CSR}	10		ns	
$\overline{CAS}$ hold time for $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_{CHR}	15		ns	
$\overline{RAS}$ precharge time to $\overline{CAS}$ active time	t_{RPC}	10		ns	
$\overline{CAS}$ precharge time for $\overline{CAS}$-before-$\overline{RAS}$ counter test	t_{CPT}	40		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	15		ns	
$\overline{OE}$ access time	t_{OEA}		25	ns	9
$\overline{OE}$ delay time	t_{OED}	15		ns	
$\overline{OE}$ to output buffer turn-off delay time	t_{OEZ}	0	15	ns	10
$\overline{OE}$ command hold time	t_{OEH}	20		ns	
Data input to $\overline{CAS}$ delay time	t_{DZC}	0		ns	16
Data input to $\overline{OE}$ delay time	t_{DZO}	0		ns	16
Masked write setup time	t_{MCS}	0		ns	
Masked write hold time referenced to $\overline{RAS}$	t_{MRH}	0		ns	
Masked write hold time referenced to $\overline{CAS}$	t_{MCH}	0		ns	

Input/Output Capacitance at Ta = 25°C, f = 1 MHz, V_{CC} = 5 V ± 10%

Parameter	Symbol	min	max	Unit
Input capacitance (A_0 to A_7, $\overline{RAS}$, $\overline{CAS}$, $\overline{UW}$, $\overline{LW}$, $\overline{OE}$)	C_{IN}		7	pF
I/O capacitance (I/O_1 to I/O_{16})	$C_{I/O}$		7	pF

Notes: 6) After the power is turned on, 200 μs are required after the arrival of V_{CC} stabilized current before memory is initialized and begins operation. In addition, before memory operation initializes, approximately 8 cycles worth of $\overline{RAS}$ dummy cycles are required. When the on-chip refresh counter is applied, approximately 8-cycles worth of $\overline{CAS}$-before-$\overline{RAS}$ dummy cycles are required instead of the $\overline{RAS}$ dummy cycles.

7) Measured at t_T = 5 ns.

8) When measuring input signal timing, V_{IH} (min) and V_{IL} (max) are used for reference points. In addition, rise and fall time are defined between V_{IH} and V_{IL}.

9) Measured using an equivalent of 50 pF and one standard TTL load.

10) t_{OFF} (max) and t_{OEZ} (max) are defined as the time until output voltage can no longer be measured when output switches to a high impedance condition.

11) Operation is guaranteed if either t_{RRH} or t_{RCH} are satisfied.

12) These parameters are measured from the falling edge of $\overline{CAS}$ for an early-write cycle, and from the falling edge of $\overline{UW}$ and $\overline{LW}$ for a read-write/read-modify-write cycle.

13) t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters for memory in that they specify the operating mode. If $t_{WCS} \geq t_{WCS}$ (min), the cycle switches to an early-write cycle and output pins switch to high impedance throughout the cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPWD} \geq t_{CPWD}$ (min), the cycle switches to a read-write/read-modify-write cycle and data outputs equal information in the selected cells. If neither of the above conditions are satisfied, output pins are in an undefined state.

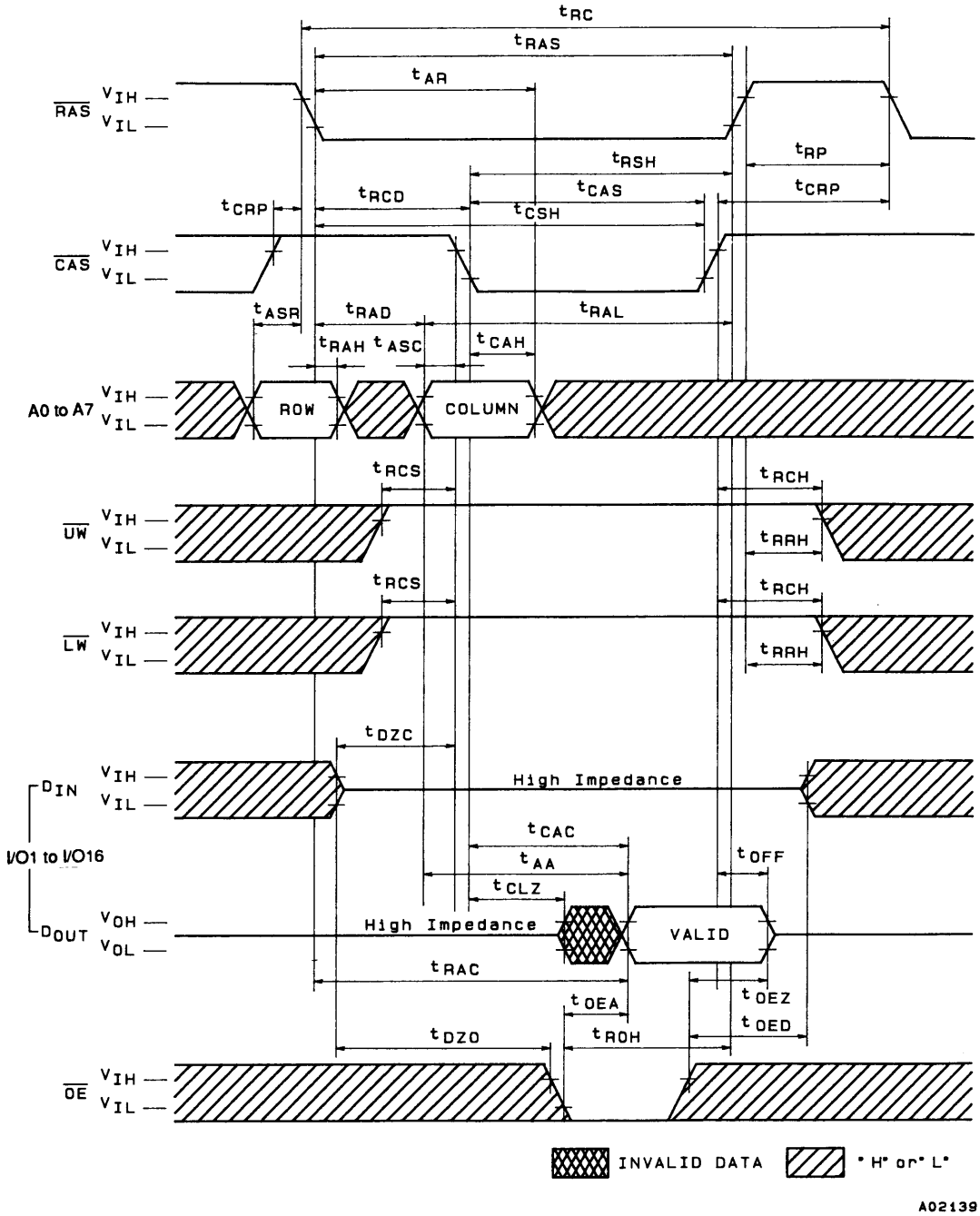
14) t_{RCD} (max) does not indicate a restrictive operating parameter but instead represents the point at which the access time t_{RAC} (max) is guaranteed. If $t_{RCD} \geq t_{RCD}$ (max), access time is determined according to t_{CAC}.

15) t_{RAD} (max) does not indicate a restrictive operating parameter but instead represents the point at which the access time t_{RAC} (max) is guaranteed. If $t_{RAD} \geq t_{RAD}$ (max), access time is determined according to t_{AA}.

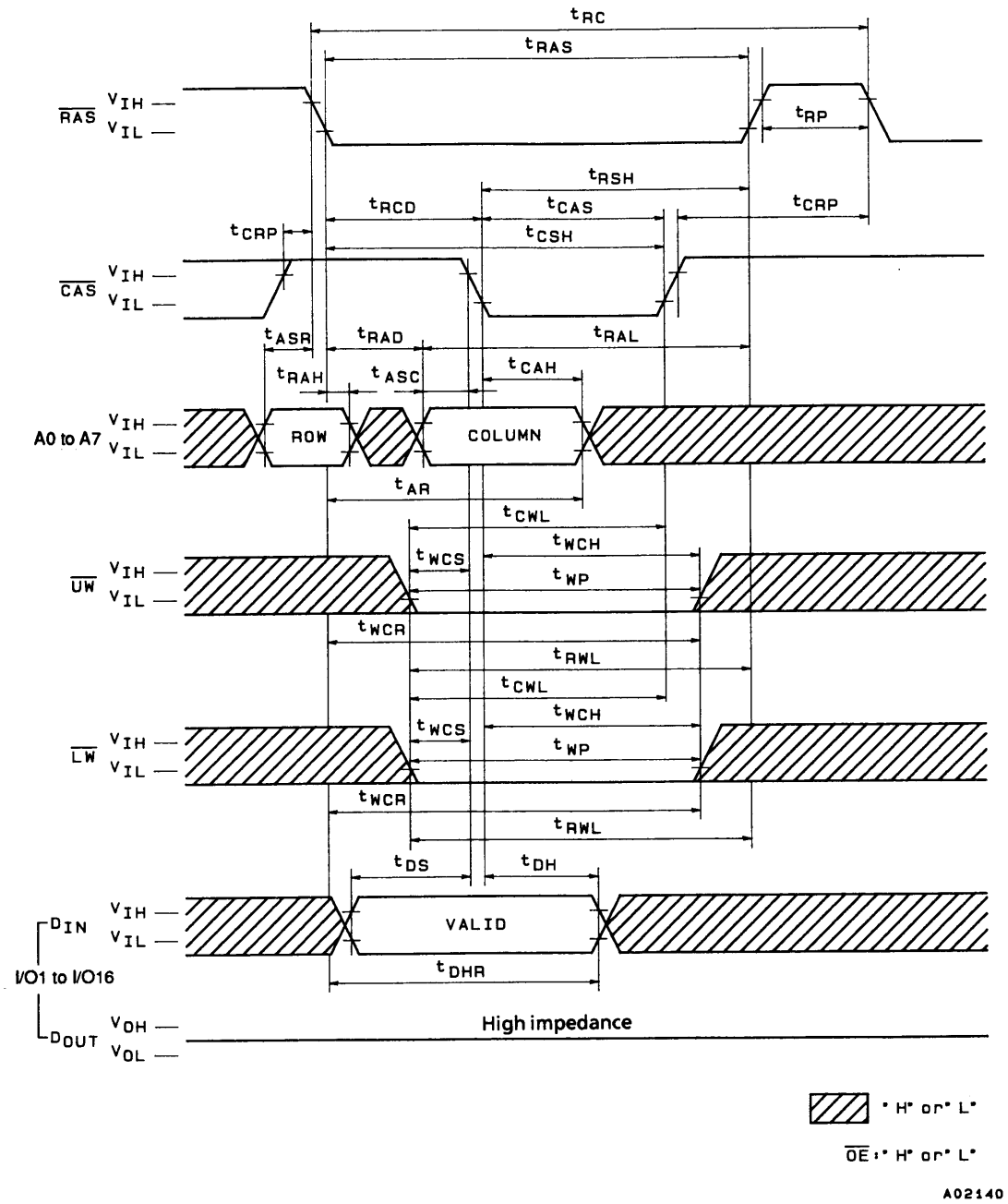
16) Operation is guaranteed if either t_{DZC} or t_{DZO} are satisfied.

Timing Chart

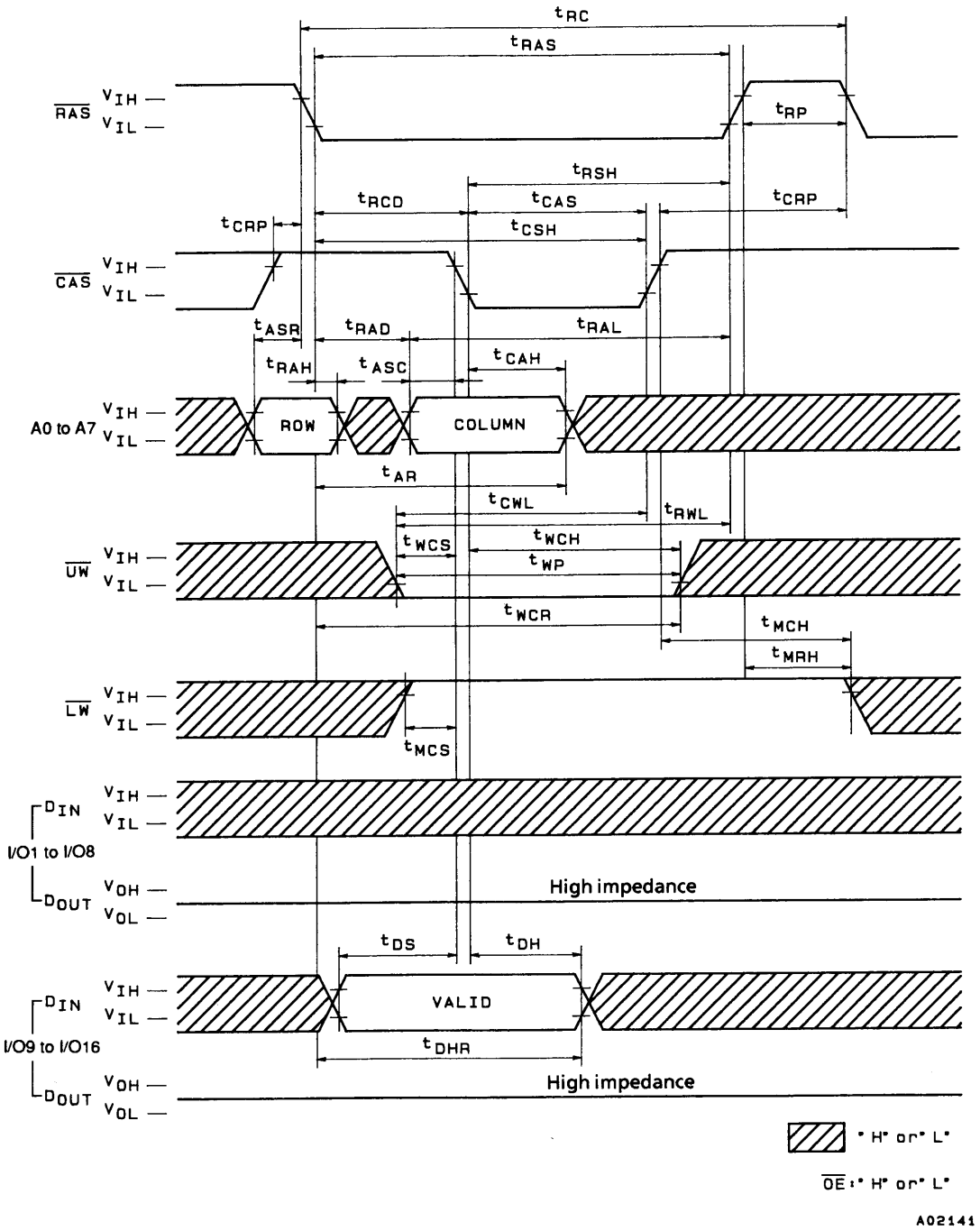
Read Cycle



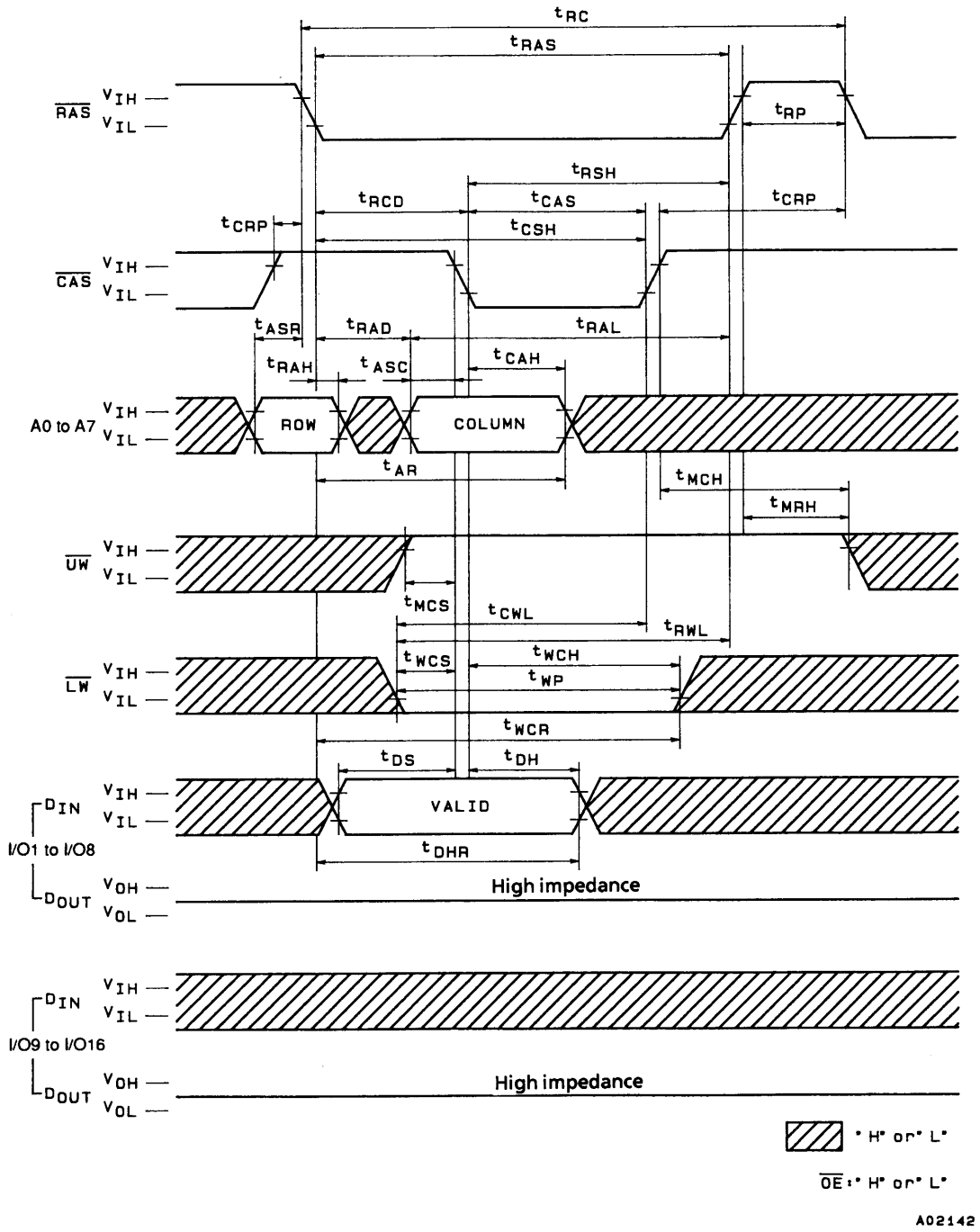
Early Write Cycle



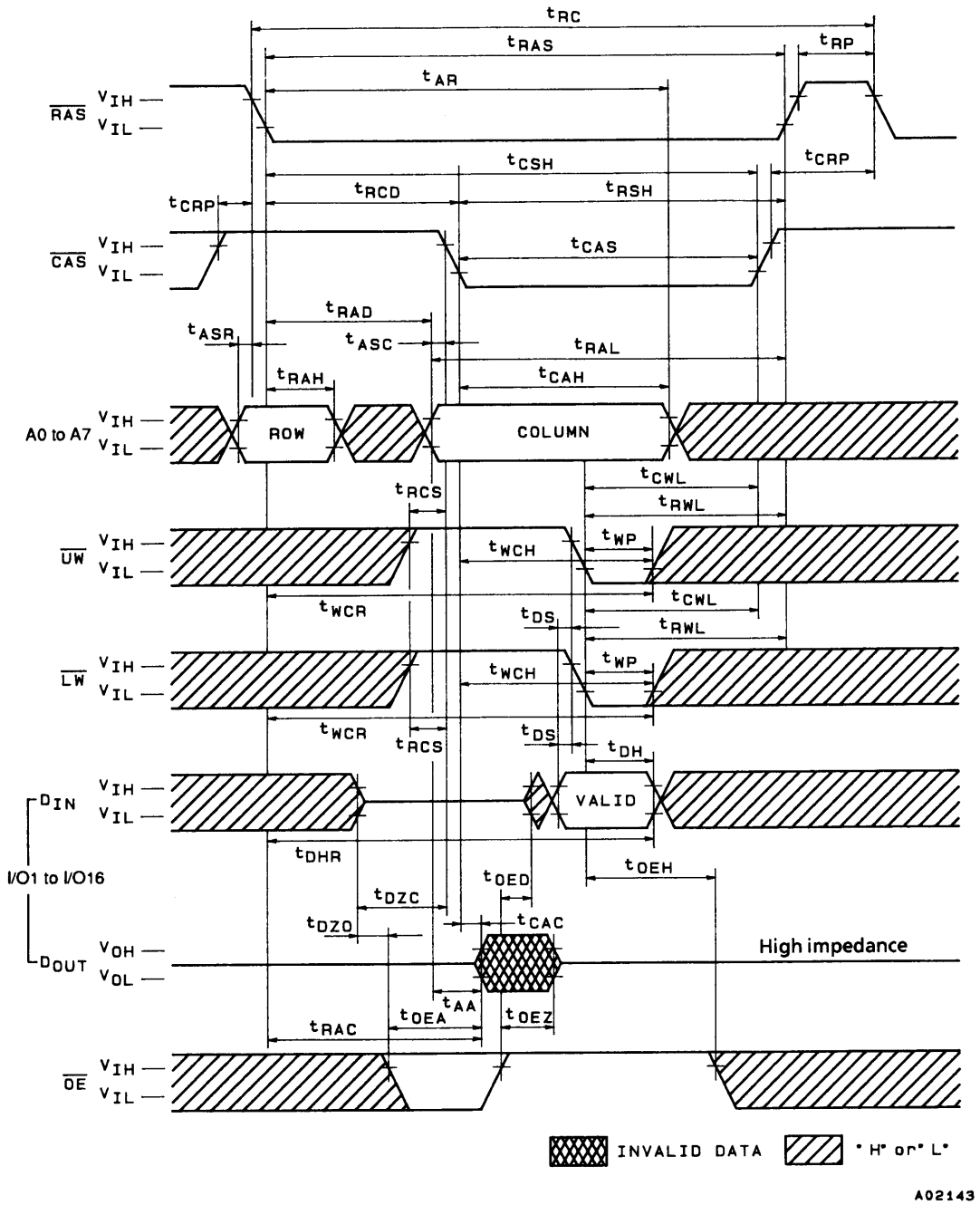
Upper Byte Early Write Cycle



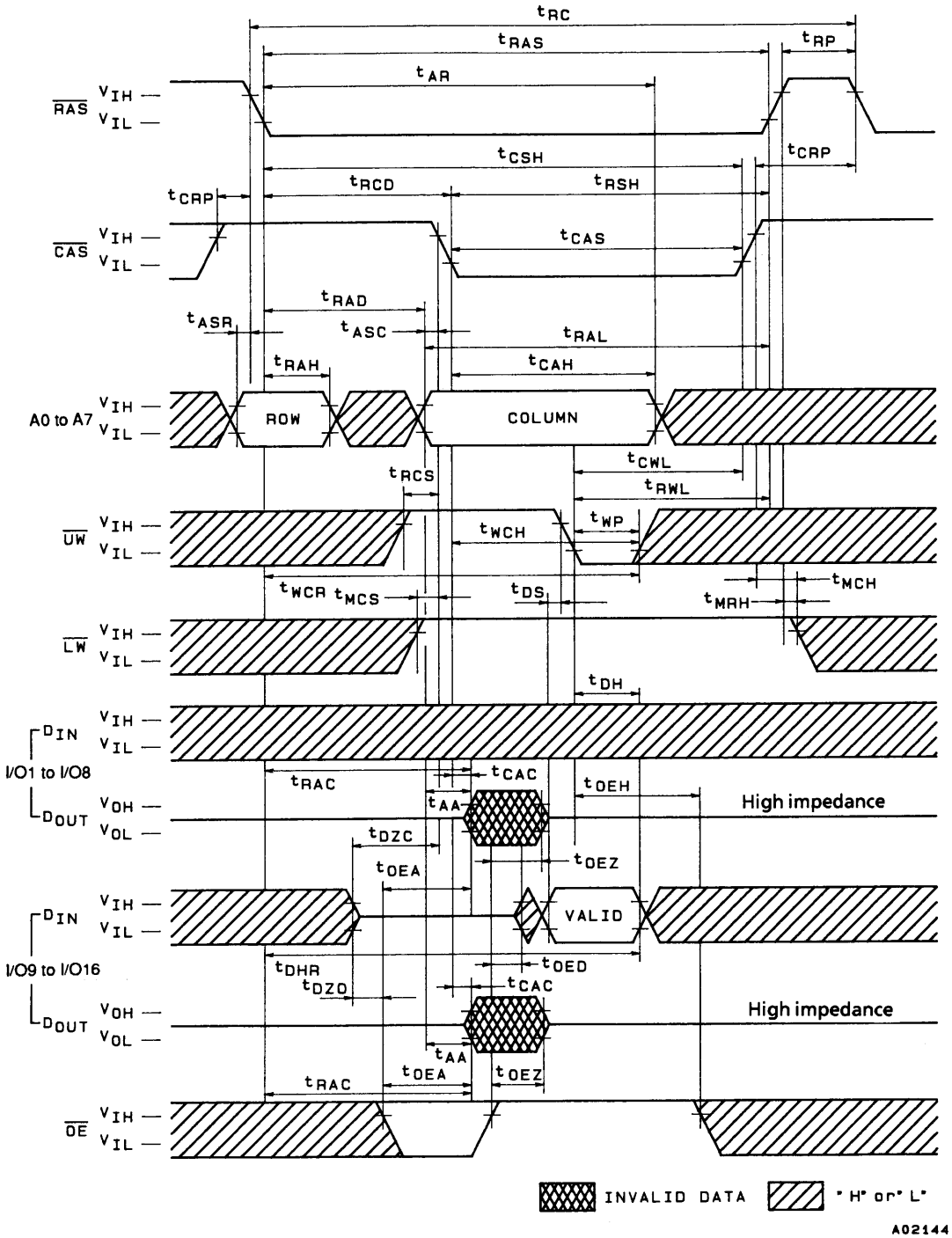
Lower Byte Early Write Cycle



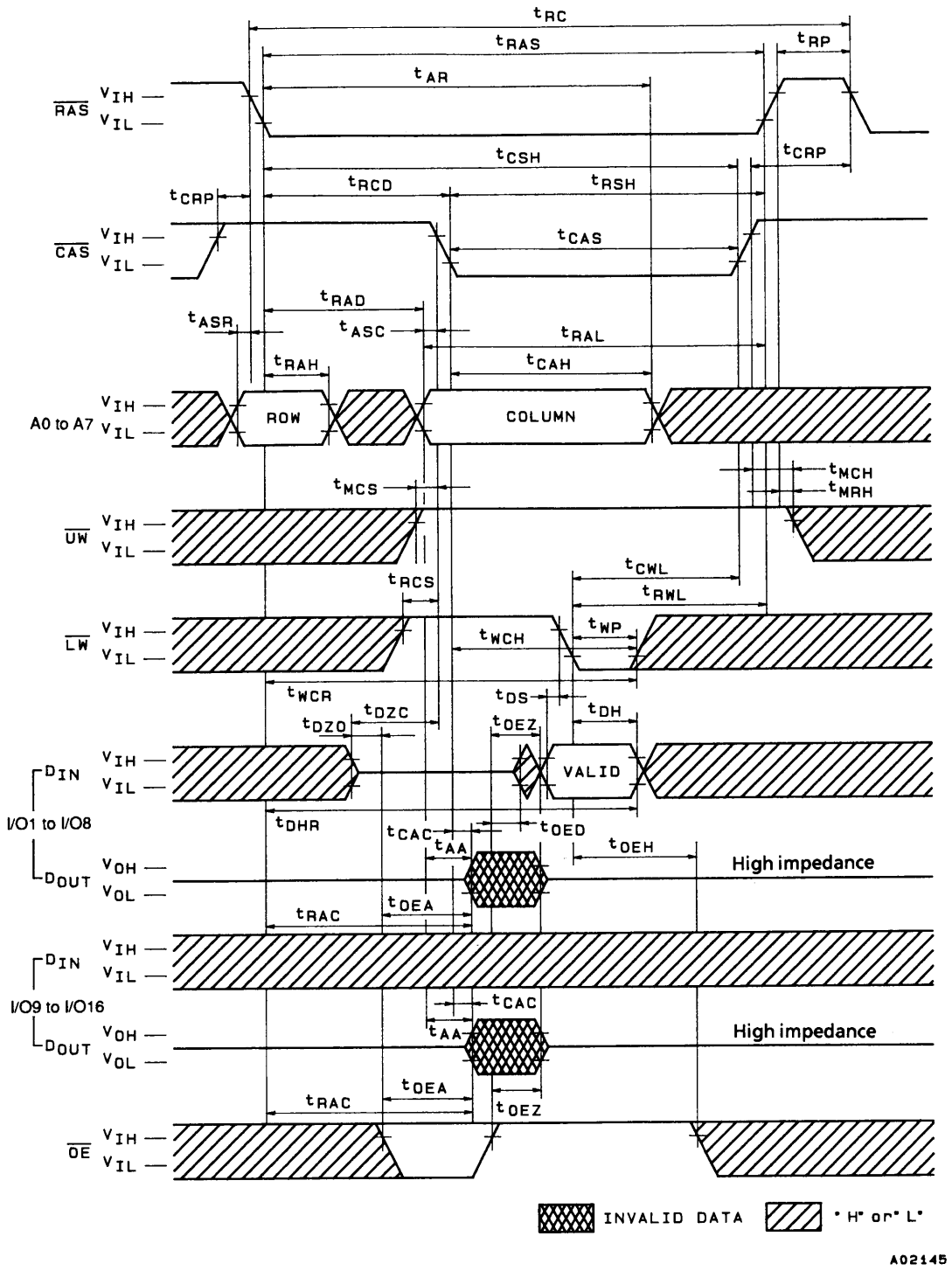
Write Cycle ($\overline{OE}$ Control)



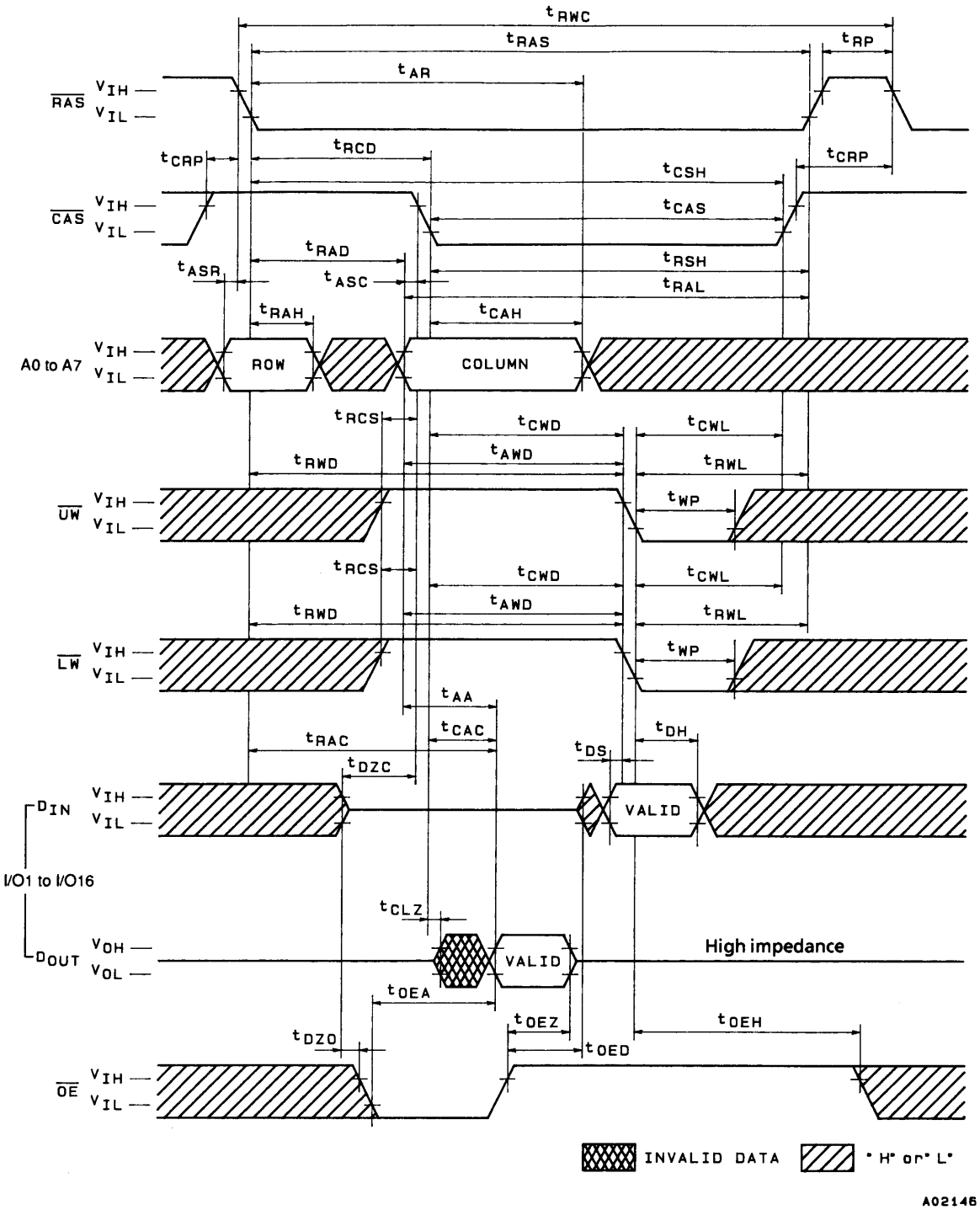
Upper Byte Write Cycle ($\overline{OE}$ Control)



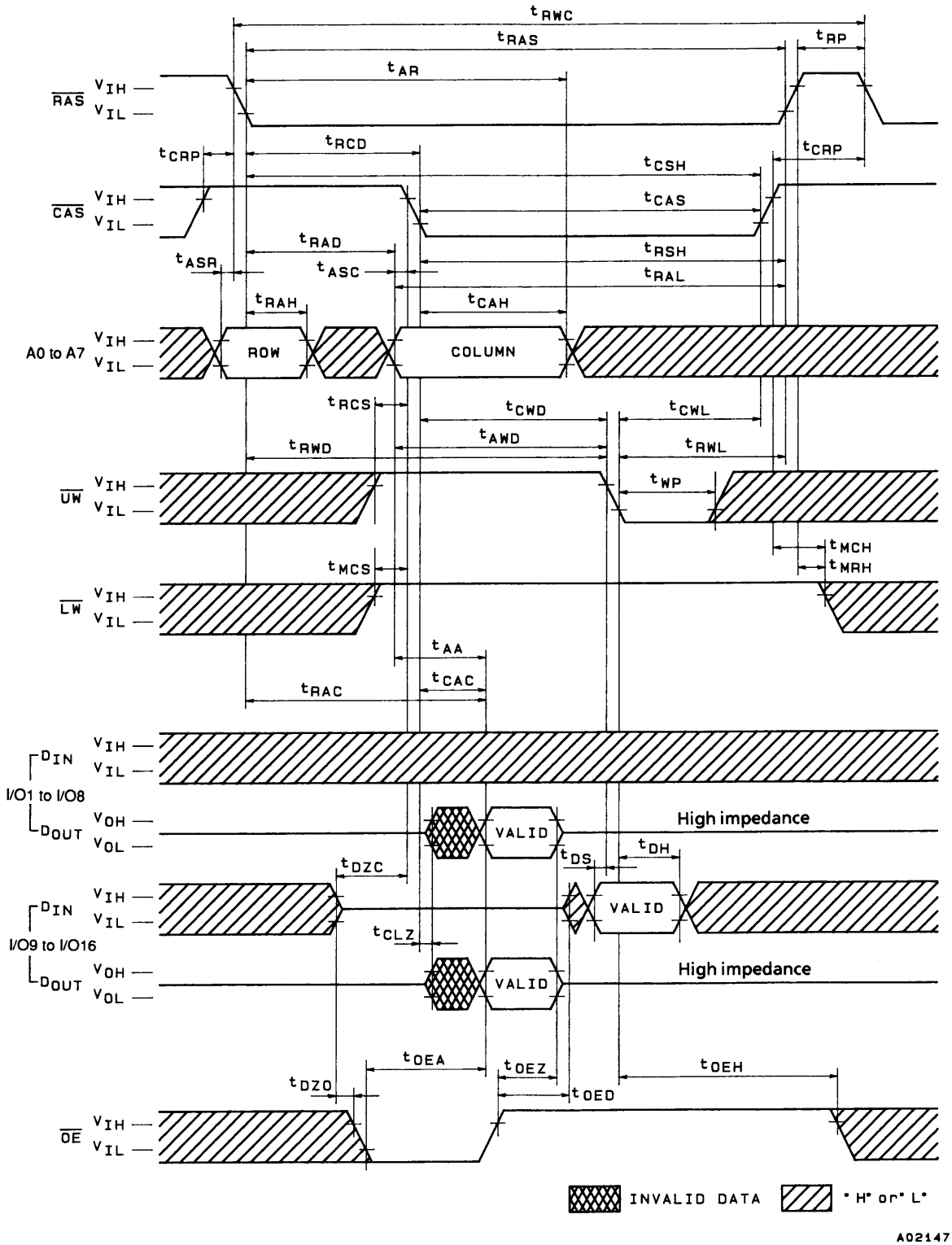
Lower Byte Write Cycle ($\overline{OE}$ Control)



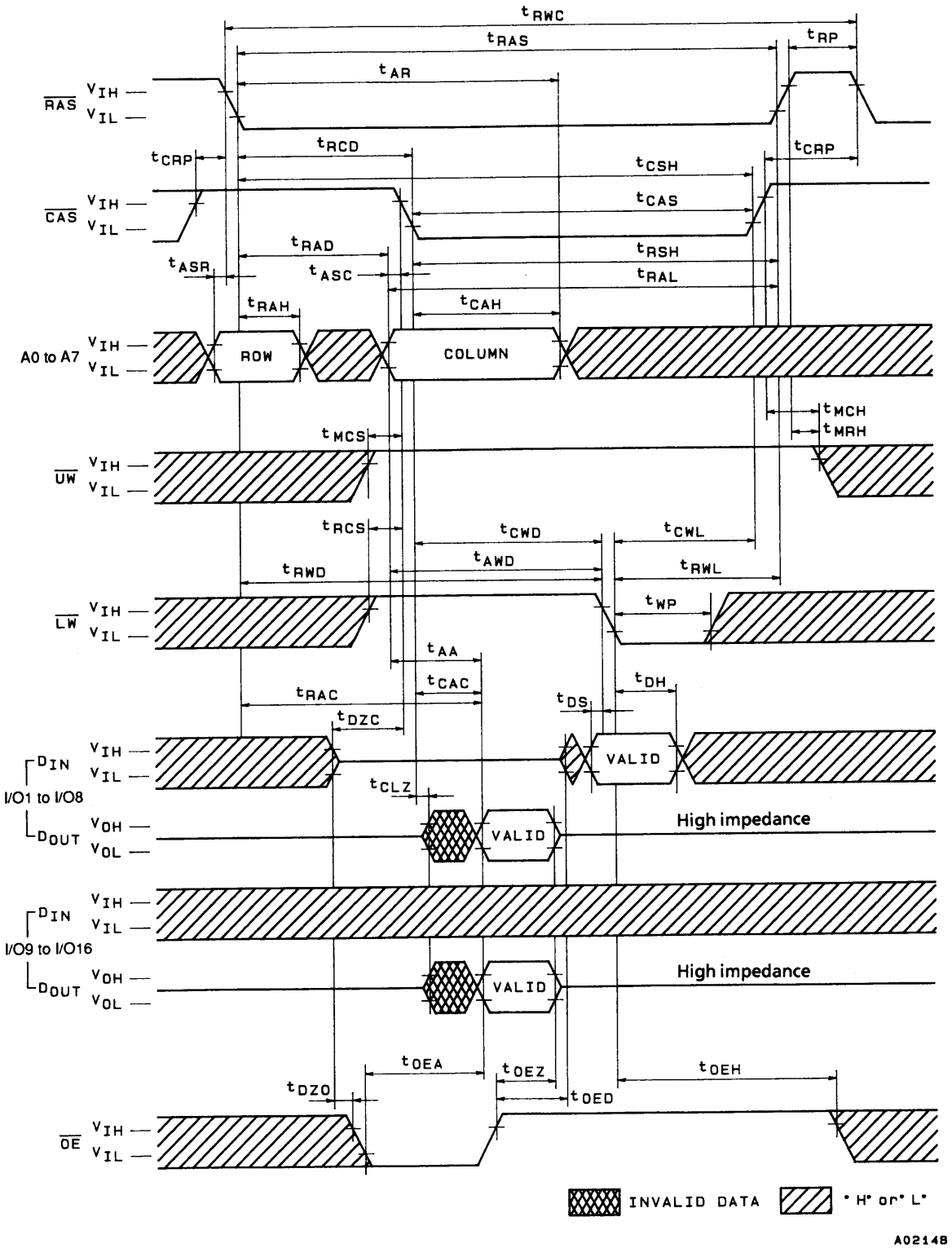
Read-Modify-Write Cycle



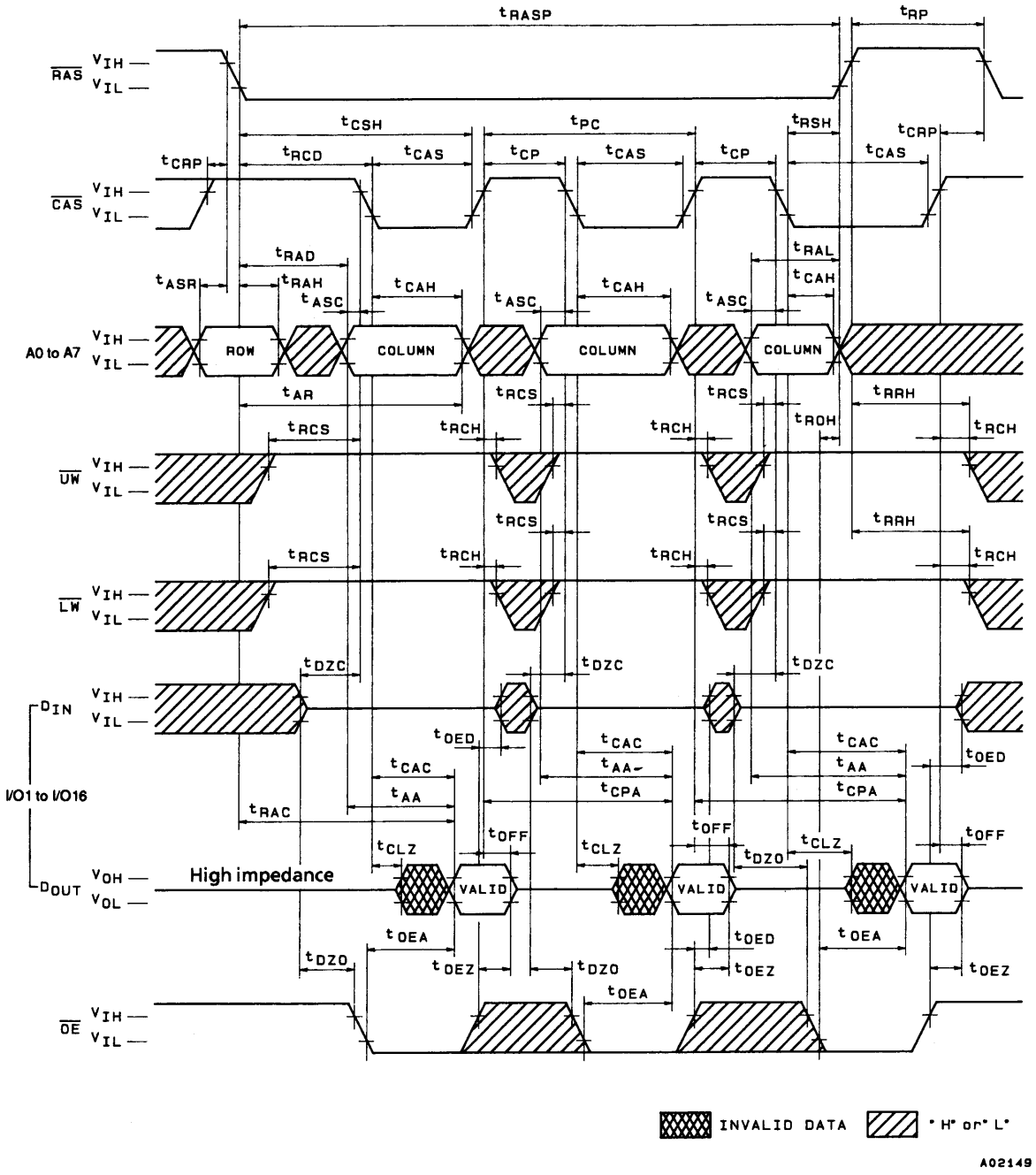
Read-Modify Upper Byte Write Cycle



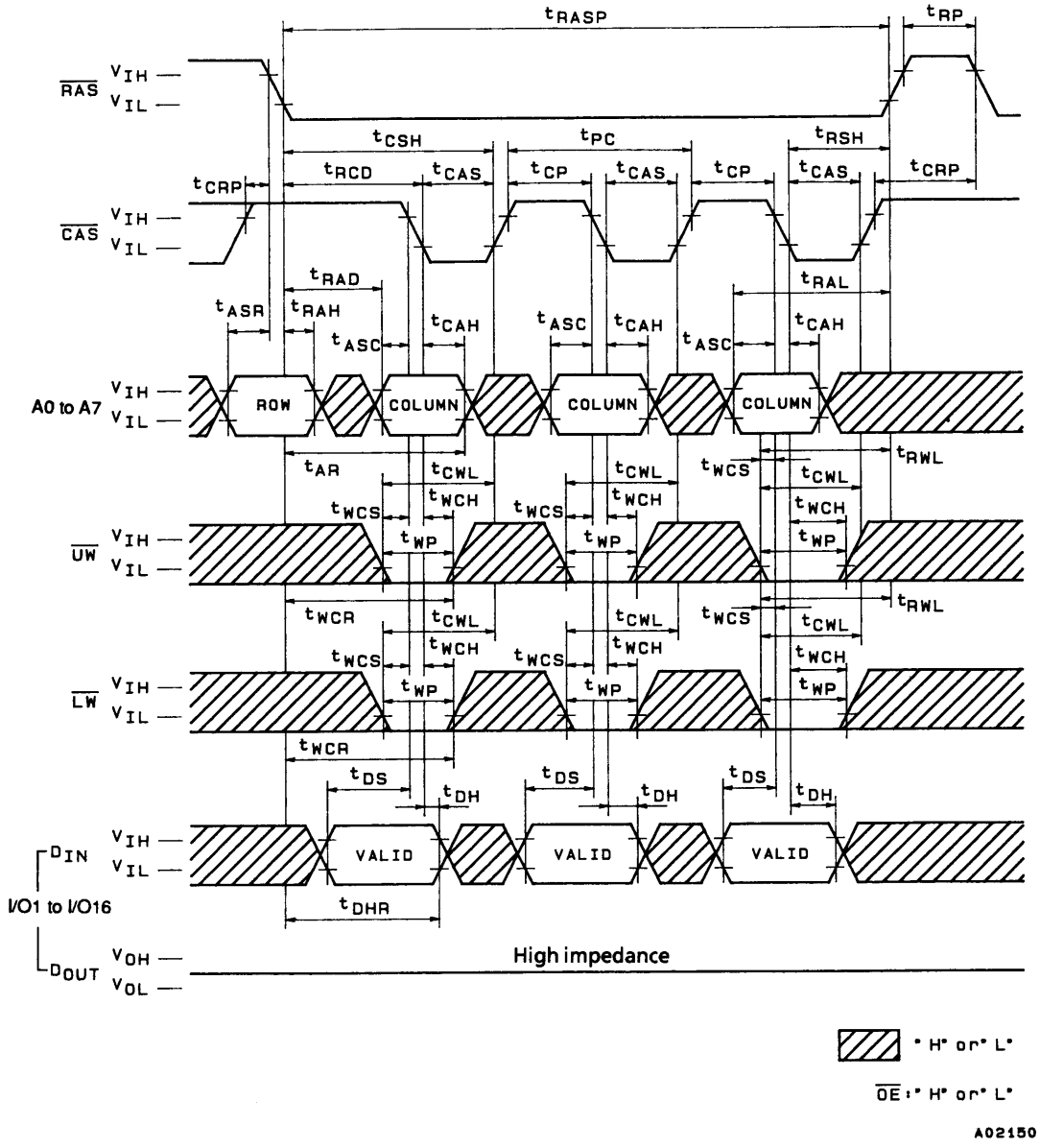
Read-Modify Lower Byte Write Cycle



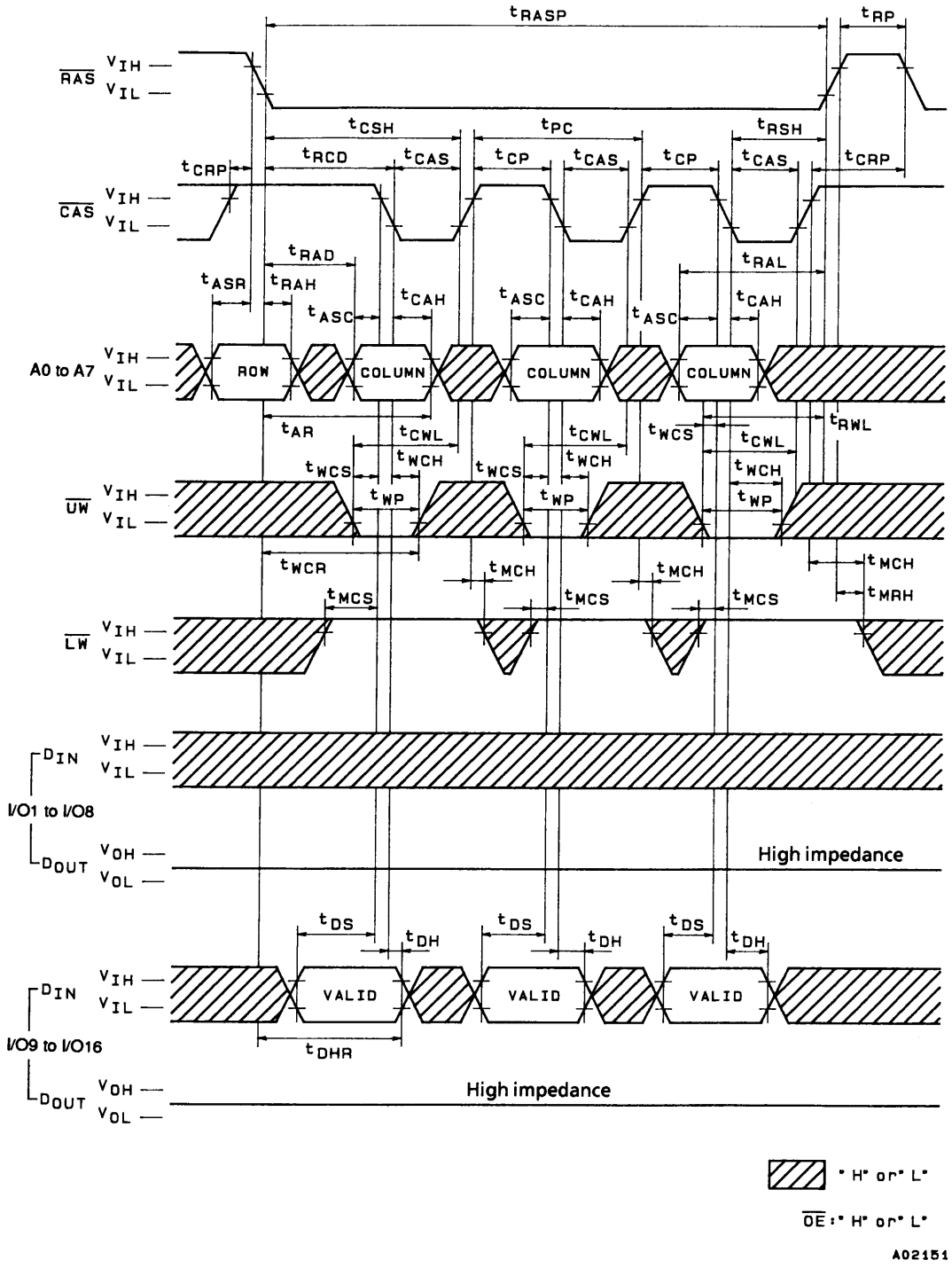
Fast Page Mode Read Cycle



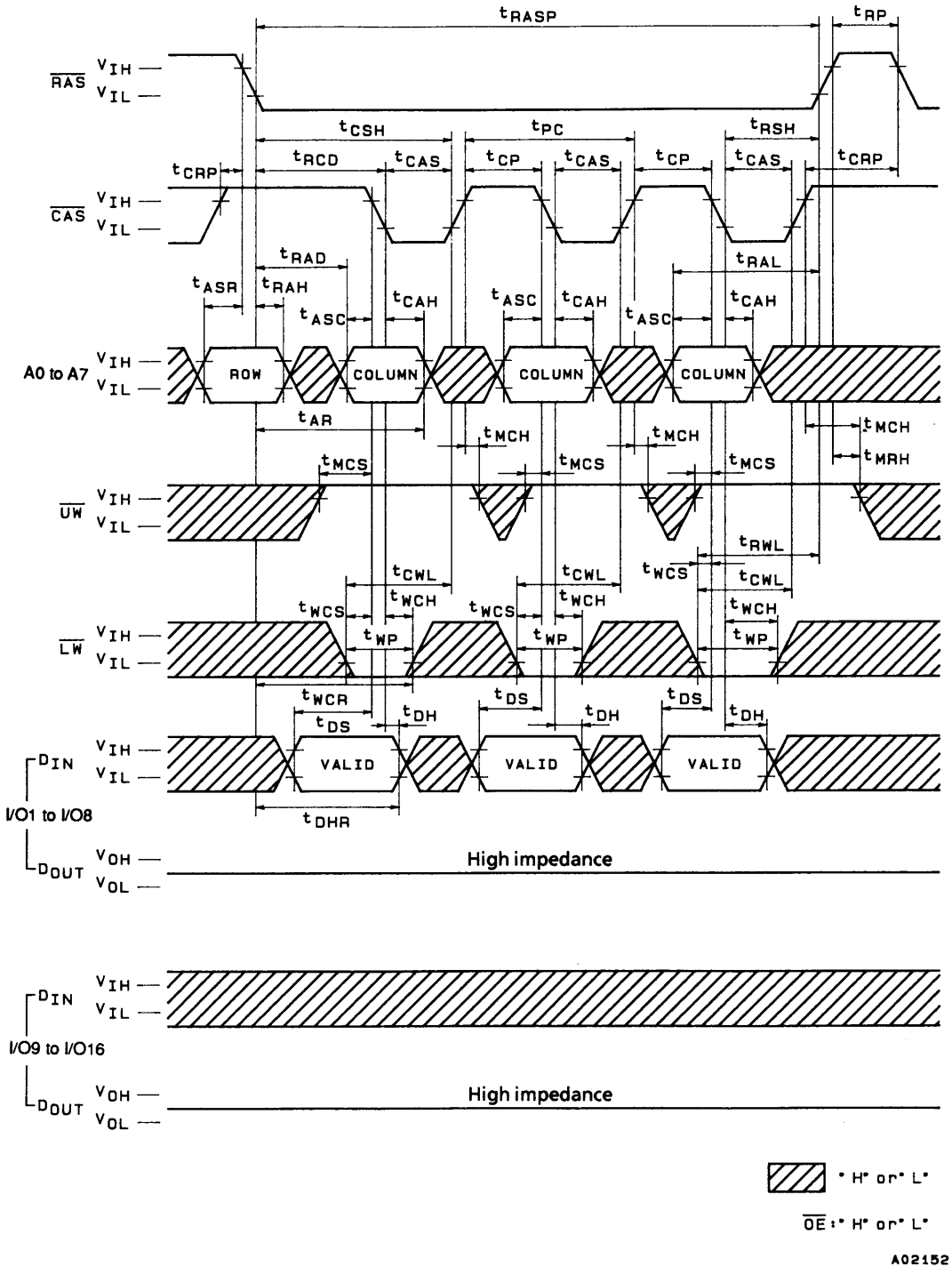
Fast Page Mode Early Write Cycle



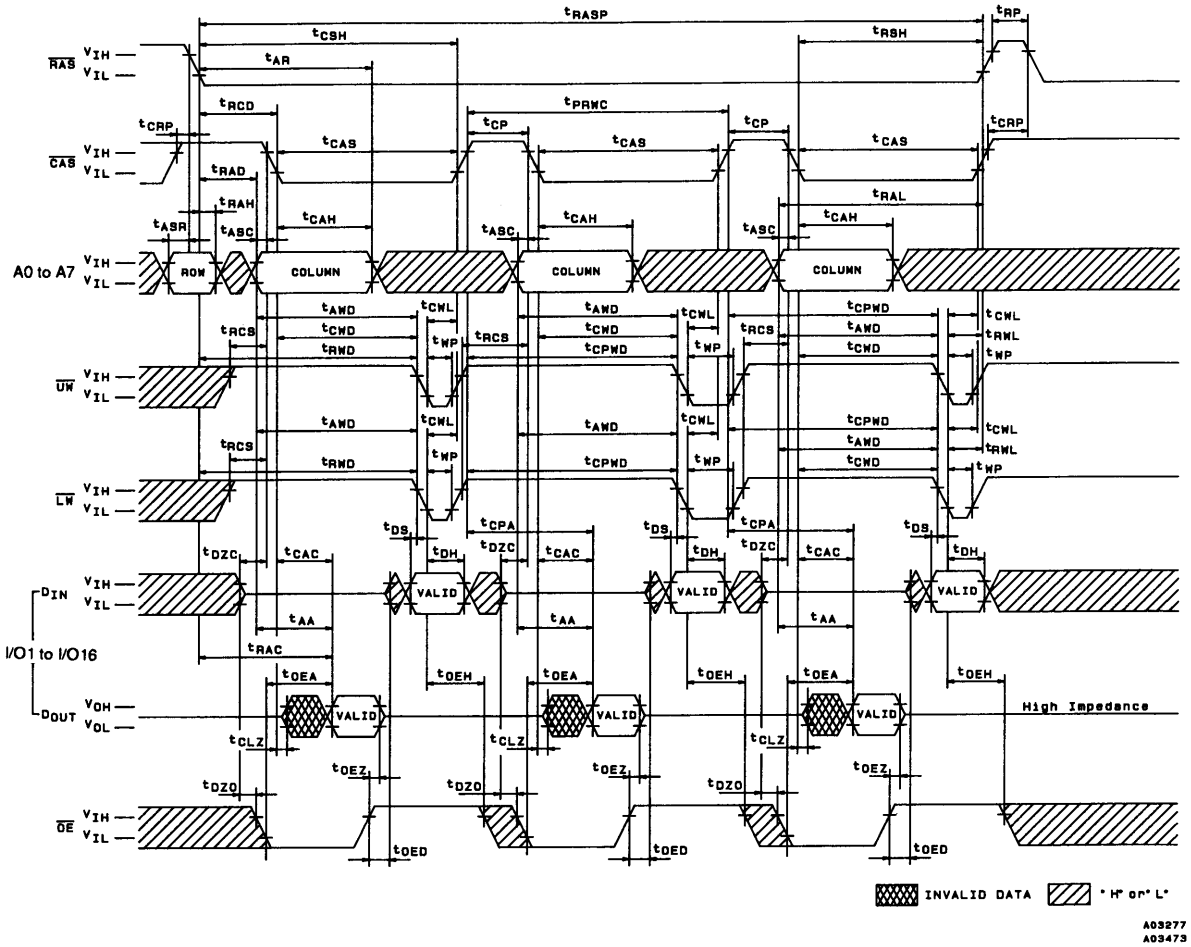
Fast Page Mode Upper Byte Early Write Cycle



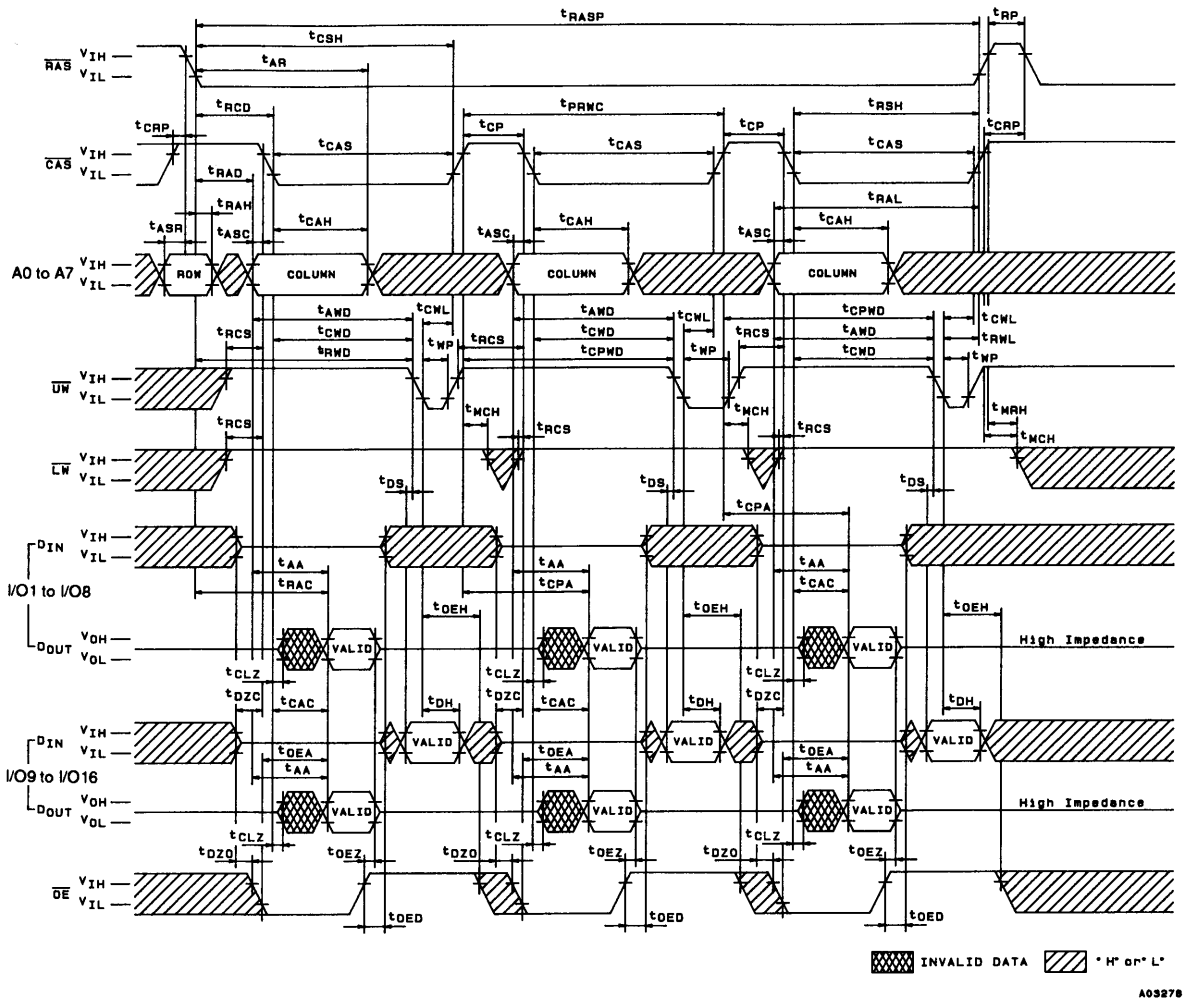
Fast Page Mode Lower Byte Early Write Cycle



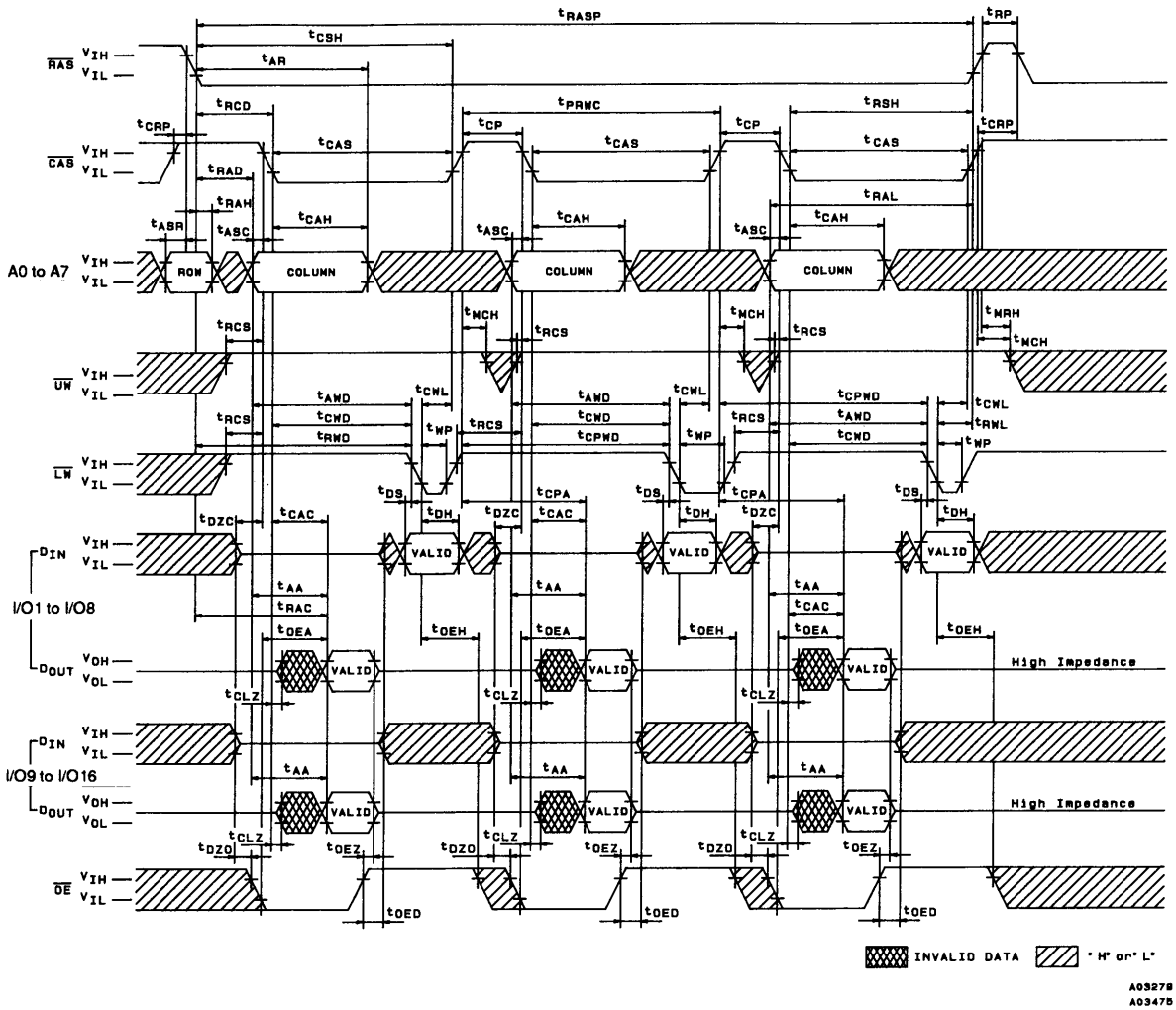
Fast Page Mode Read-Modify-Write Cycle



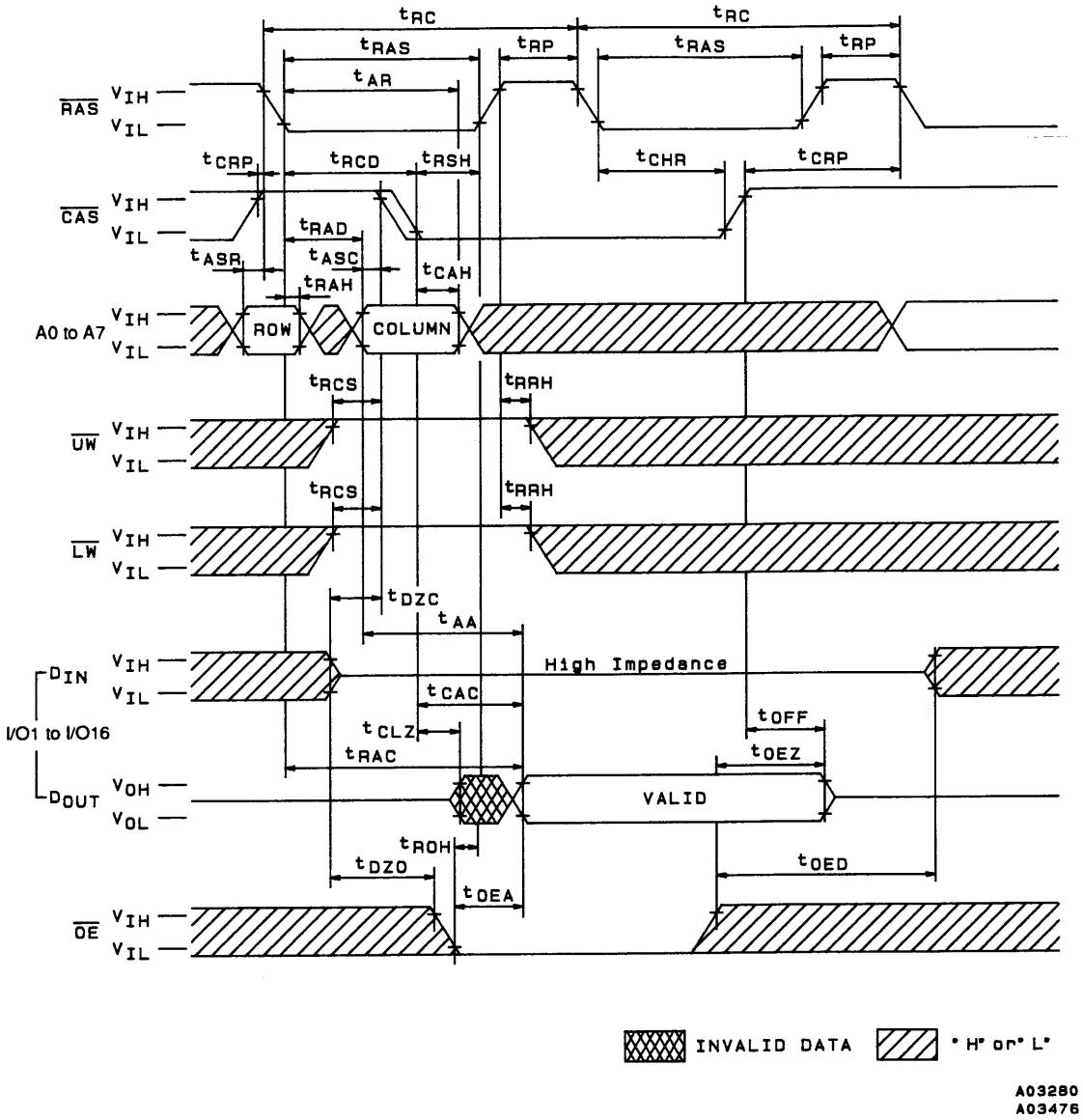
Fast Page Mode Read-Modify Upper Byte Write Cycle



Fast Page Mode Read-Modify Lower Byte Write Cycle

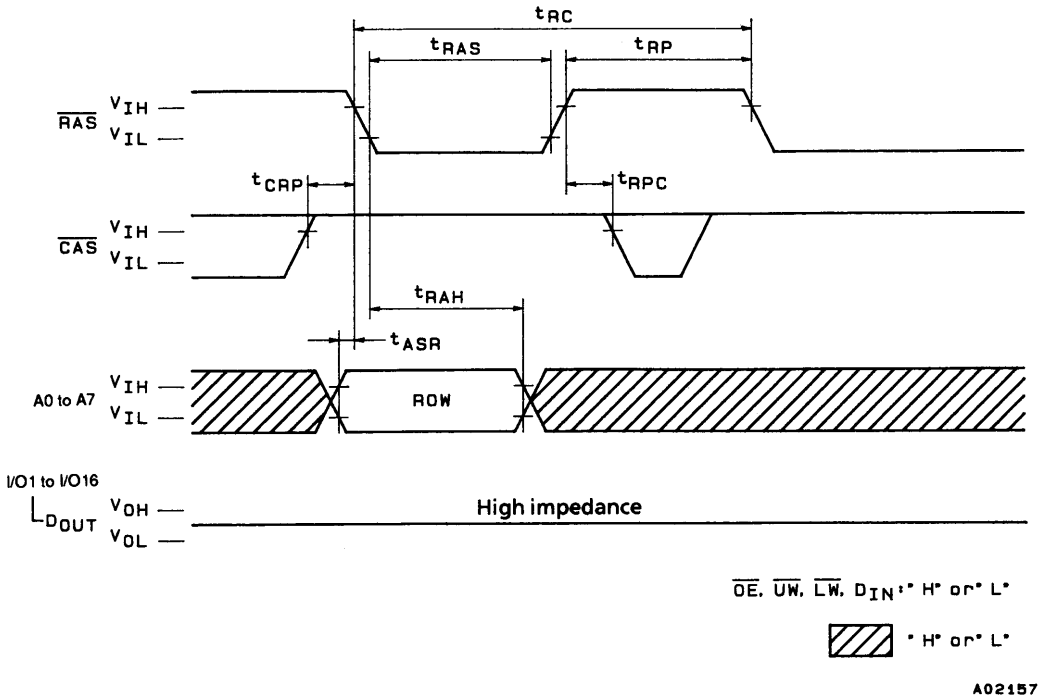


Hidden Refresh Cycle

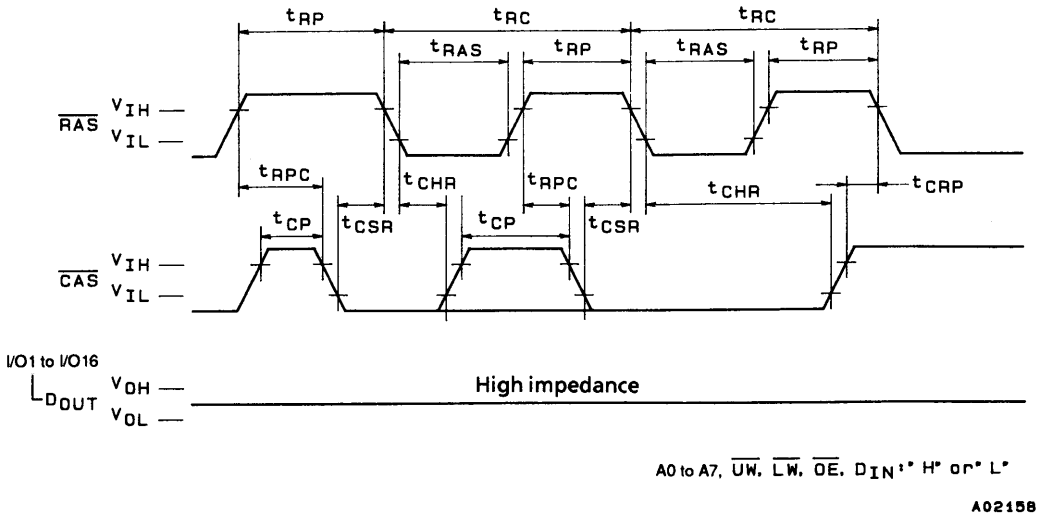


A03280
A03476

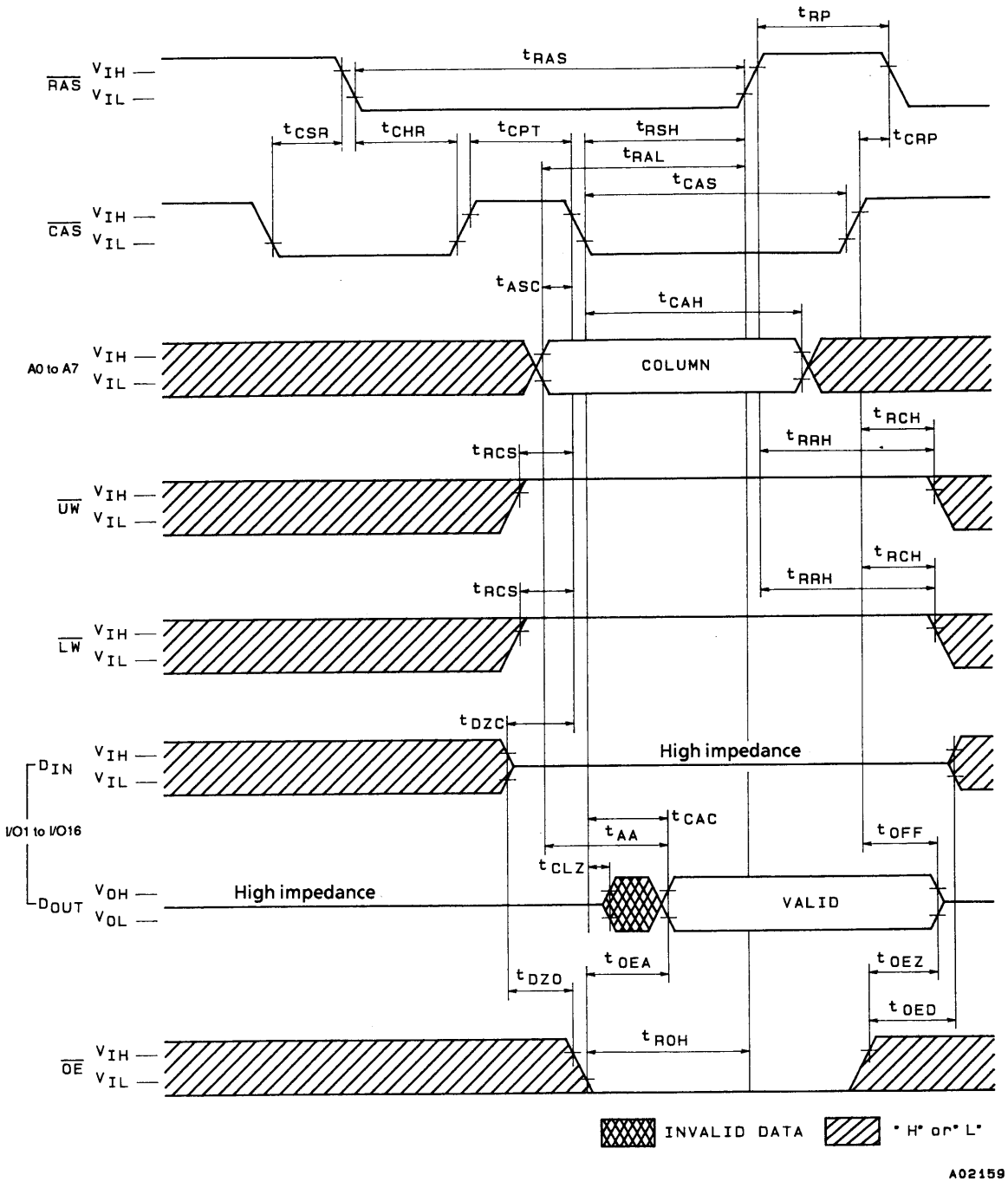
$\overline{\text{RAS}}$-Only Refresh Cycle



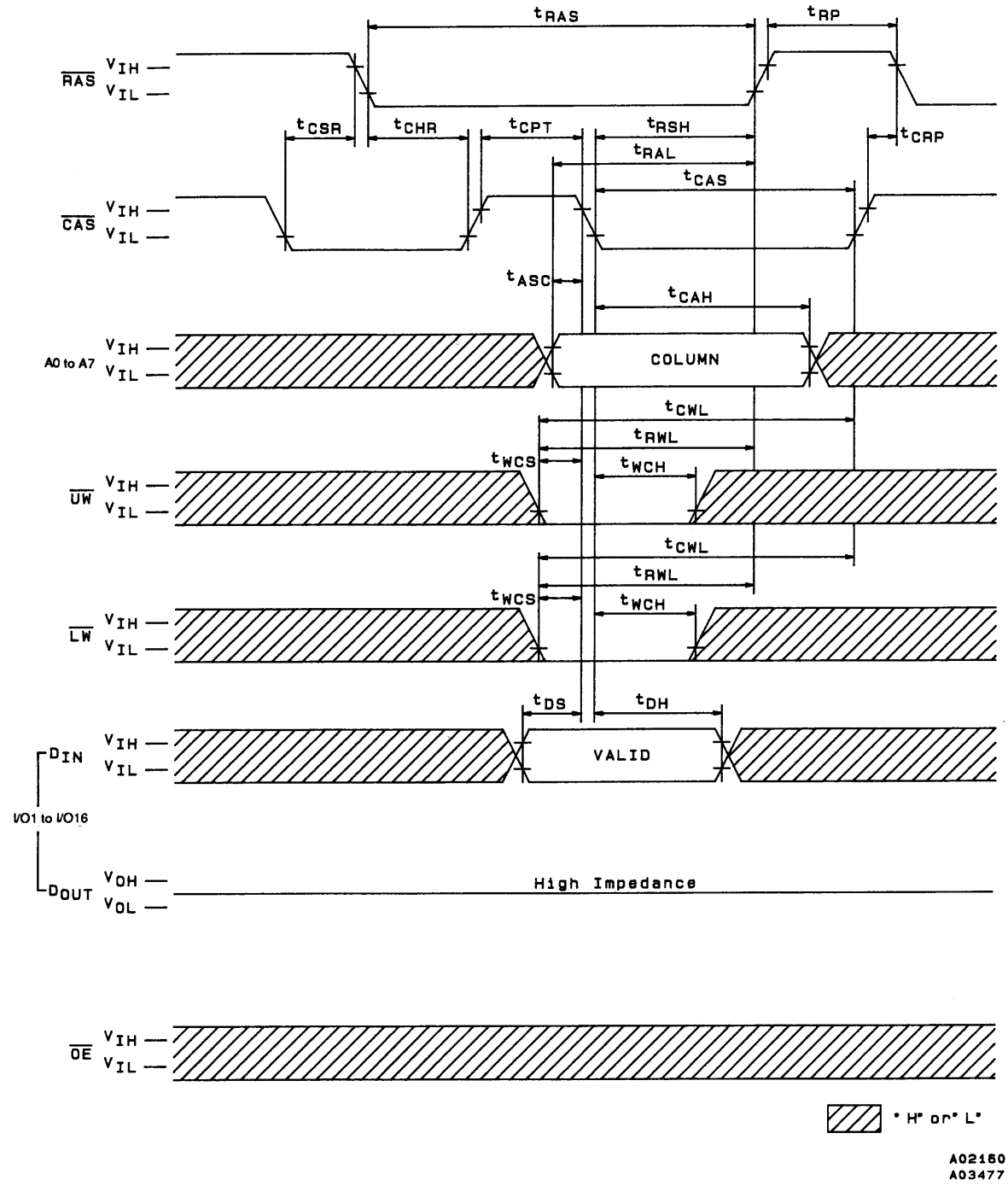
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



CAS-Before-RAS Refresh Counter Test Cycle (read)



$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle (write)



$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle (read-modify-write)