

SANYO	No.4794B	LC3564S, SS, SM, ST-70/85/10
		64K (8192words×8 bits)SRAM

Overview

The LC3564S, LC3564SS, LC3564SM, and LC3564ST are asynchronous silicon gate CMOS static RAMs with an 8192-word X 8-bit organization. These SRAMs are full CMOS type SRAMs with a six-transistor memory cell and feature high-speed access, a low operating current, and an ultra-low standby current. Control signal inputs include an \overline{OE} input for high-speed memory access and two chip enable inputs, $\overline{CE1}$ and $\overline{CE2}$, for power-down and device selection. Thus these products are optimal for systems that require low power and/or battery backup and they support easy expansion of memory capacities. The ultra-low standby mode current drain allows capacitors to be used for backup and 3V operation makes these devices an excellent choice for use in battery operated portable equipment.

Features

- Supply voltage : 2.7 to 5.5V
 - 5V operation : $5.0V \pm 10\%$
 - 3V operation : $3.0V \pm 10\%$
- Address access time (t_{AA})
 - 5V operation
 - LC3564S, SS, SM, ST-70 : 70ns (max.)
 - LC3564S, SS, SM, ST-85 : 85ns (max.)
 - LC3564S, SS, SM, ST-10 : 100ns (max.)
 - 3V operation
 - LC3564S, SS, SM, SS-70 : 200ns (max.)
 - LC3564S, SS, SM, SS-85 : 250ns (max.)
 - LC3564S, SS, SM, SS-10 : 500ns (max.)
- Ultra-low standby current
 - 5V operation : $1.0\mu A$ ($T_a \leq 70^\circ C$)
 - $3.0\mu A$ ($T_a \leq 85^\circ C$)
 - 3V operation : $0.8\mu A$ ($T_a \leq 70^\circ C$)
 - $2.5\mu A$ ($T_a \leq 85^\circ C$)
- Operating temperature
 - 3V operation : $-40^\circ C$ to $+85^\circ C$
 - 5V operation : $-40^\circ C$ to $+85^\circ C$
- Data retention voltage : 2.0 to 5.5V
- All I/O levels
 - 5V operation : TTL compatible
 - 3V operation : $V_{CC} - 0.2V/0.2V$
- Three control inputs (\overline{OE} , $\overline{CE1}$, $\overline{CE2}$)
- Common input/output pins, three-state outputs
- No clock or timing signals required

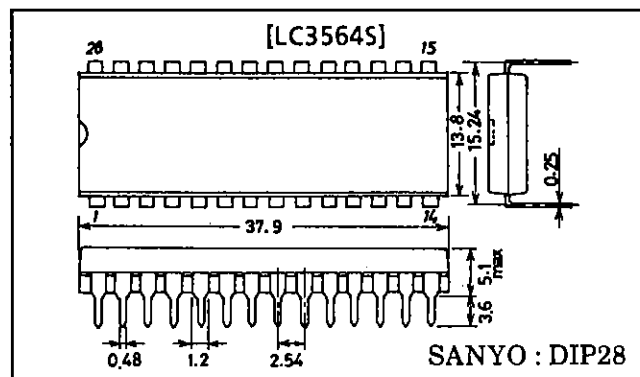
Package :

- 28-pin DIP (600mil)plastic package : LC3564S
- 28-pin DIP (300mil)plastic package : LC3564SS
- 28-pin SOP (450mil)plastic package : LC3564SM
- 28-pin TSOP (8×13.4 mm)plastic package : LC3564ST

Package Dimensions

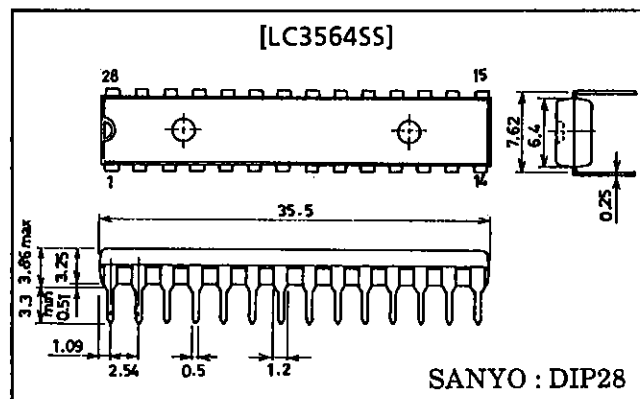
unit : mm

3012A-DIP28



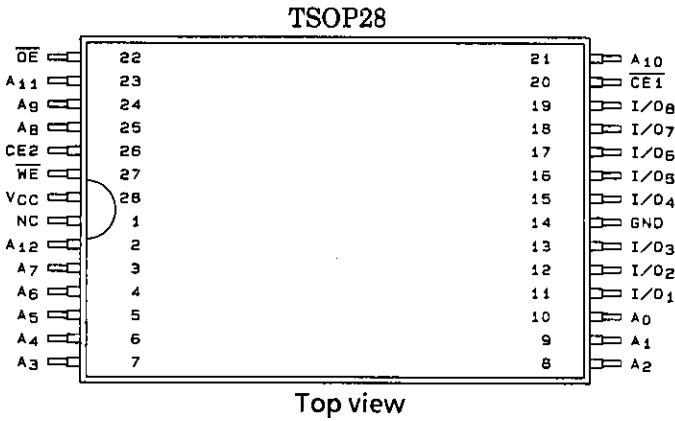
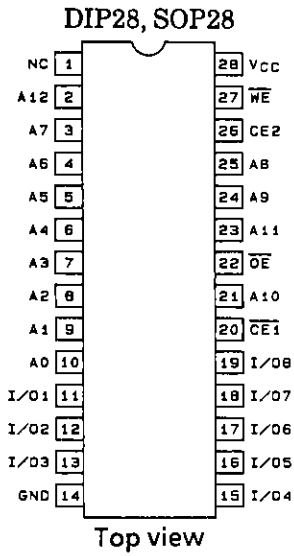
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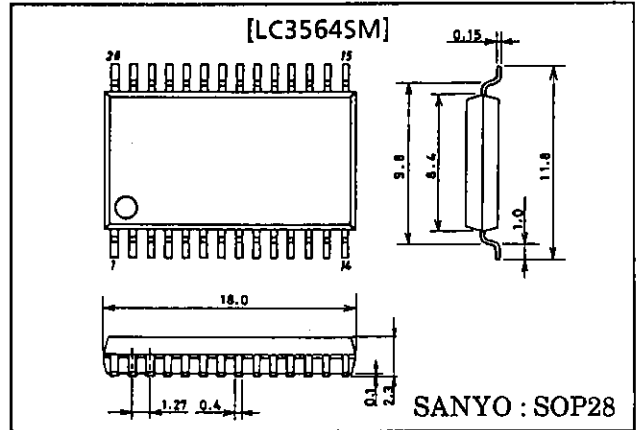
SANYO Electric Co., Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

Pin Assignments

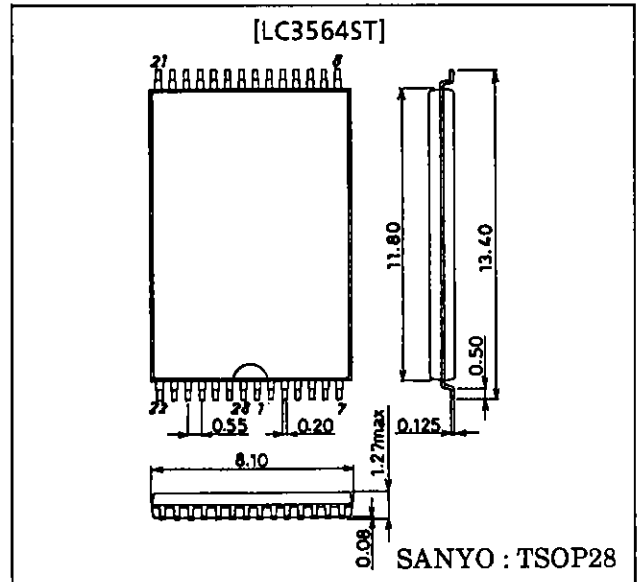


Package Dimensions

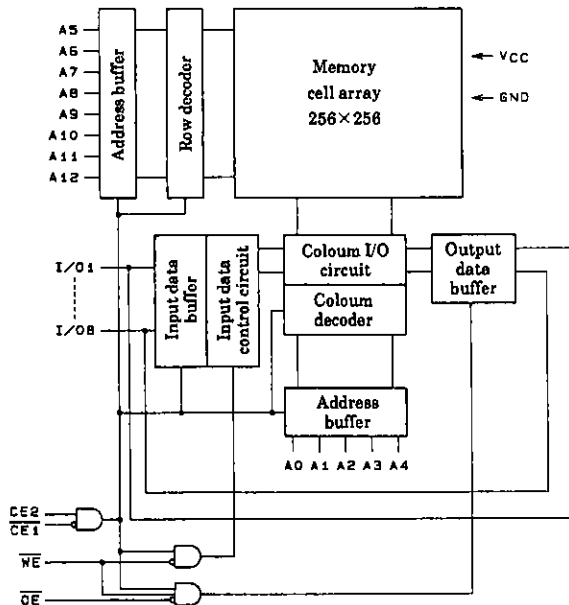
unit : mm
3187-SOP28



unit : mm
3221-TSOP28



Block Diagram



A0 to A12	Address input
\overline{WE}	Write enable
\overline{OE}	Output enable
$\overline{CE1}$, $\overline{CE2}$	Chip enable
I/O ₁ to I/O ₈	Data input/output
VCC, GND	Power, ground

Pin Functions

Mode	$\overline{CE1}$	CE2	\overline{OE}	\overline{WE}	I/O	Current
Read Cycle	L	H	L	H	Data output	I_{CCA}
Write Cycle	L	H	×	L	Data input	I_{CCA}
Output Disable	L	H	H	H	High impedance	I_{CCA}
Unselected	H	×	×	×	High impedance	I_{CCS}
	×	L	×	×	High impedance	I_{CCS}

× : Arbitrary H or L

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Max supply voltage	$V_{CC\ max}$		7.0	V
Input voltage	V_{IN}		-0.3* to $V_{CC} + 0.3$	V
I/O voltage	$V_{I/O}$		-0.3 to $V_{CC} + 0.3$	V
Operating temperature range	T_{opr}		-40 to +85	°C
Storage temperature range	T_{stg}		-55 to +125	°C

*) The inputs may undershoot to -3.0V (min.) for periods less than 30ns.

I/O Capacitance at $T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Input/output capacitance	$C_{I/O}$	$V_{I/O} = 0\text{V}$		6	10	pF
Input capacitance	C_I	$V_{IN} = 0\text{V}$		6	10	pF

(Note) This parameter is sampled and not 100% tested.

5V Operation

DC Recommended Operating Ranges at $T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 4.5$ to 5.5V

Parameter	Symbol	min	typ	max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		$V_{CC} + 0.3$	V
	V_{IL}	-0.3*		+0.8	V

*) The inputs may undershoot to -3.0V (min.) for periods less than 30ns.

DC Electrical Characteristics at $T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 4.5$ to 5.5V

Parameter	Symbol	Conditions	min	typ*	max	Unit		
Input leakage current	I_{LI}	$V_{IN} = 0$ to V_{CC}	-1.0		+1.0	μA		
I/O leakage current	I_{LO}	$V_{\overline{CE1}} = V_{IH}$ or $V_{CE2} = V_{IL}$ or $V_{\overline{OE}} = V_{IH}$ or $V_{\overline{WE}} = V_{IL}$, $V_{I/O} = 0$ to V_{CC}	-1.0		+1.0	μA		
Output high level voltage	V_{OH}	$I_{OH} = -1.0\text{mA}$	2.4			V		
Output low level voltage	V_{OL}	$I_{OL} = 2.0\text{mA}$			0.4	V		
Operating current	$V_{CC} - 0.2\text{V}/$ 0.2V input	I_{CCA1}	$V_{\overline{CE1}} \cong 0.2\text{V}$, $V_{CE2} \cong V_{CC} - 0.2\text{V}$, $I_{I/O} = 0\text{mA}$, $V_{IN} \cong 0.2\text{V}$ or $V_{IN} \cong V_{CC} - 0.2\text{V}$	$T_a \leq 70^\circ\text{C}$	0.01	1.0	μA	
				$T_a \leq 85^\circ\text{C}$		3.0		
	I_{CCA4}	$V_{\overline{CE1}} \cong 0.2\text{V}$, $V_{CE2} \cong V_{CC} - 0.2\text{V}$, $I_{I/O} = 0\text{mA}$, DUTY 100%	min cycle	LC3564S, SS, SM, ST-70		35	mA	
				LC3564S, SS, SM, ST-85		35		
				LC3564S, SS, SM, ST-10		30		
				1 μs cycle		4	mA	
	TTL input	I_{CCA2}	$V_{\overline{CE1}} = V_{IL}$, $V_{CE2} = V_{IH}$, $I_{I/O} = 0\text{mA}$, $V_{IN} = V_{IH}$ or V_{IL}	min cycle	LC3564S, SS, SM, SS-70		7	mA
					LC3564S, SS, SM, SS-85		40	
		I_{CCA3}	$V_{\overline{CE1}} = V_{IL}$, $V_{CE2} = V_{IH}$, $I_{I/O} = 0\text{mA}$, DUTY 100%	min cycle	LC3564S, SS, SM, SS-85		40	mA
					LC3564S, SS, SM, SS-10		35	
			1 μs cycle		7	mA		
Standby current	$V_{CC} - 0.2\text{V}/$ 0.2V input	I_{CCS1}	$V_{CE2} \cong 0.2\text{V}$ or $V_{\overline{CE1}} \cong V_{CC} - 0.2\text{V}$ $V_{CE2} \cong V_{CC} - 0.2\text{V}$	$T_a \leq 70^\circ\text{C}$	0.01	1.0	μA	
				$T_a \leq 85^\circ\text{C}$		3.0		
	TTL input	I_{CCS2}	$V_{CE2} = V_{IL}$ or $V_{\overline{CE1}} = V_{IH}$, $V_{IN} = 0$ to V_{CC}			2.0	mA	

*) Reference value at $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$

LC3564S, SS, SM, ST-70/85/10

AC Electrical Characteristics at Ta = -40 to +85°C, V_{CC} = 4.5 to 5.5V

AC test conditions

- Input pulse levels : V_{IH} = 2.4V, V_{IL} = 0.6V
- Input rise and fall time : 5ns
- Input and output timing reference levels : 1.5V
- Output load LC3564S, SS, SM, ST-70 : 30pF + 1TTL gate
(including jig capacitance)
- LC3564S, SS, SM, ST-85/10 : 100pF + 1TTL gate
(including jig capacitance)

Read Cycle

Parameter	Symbol	LC3564S, SS, SM, ST						Unit
		-70		-85		-10		
		min	max	min	max	min	max	
Read cycle time	t _{RC}	70		85		100		ns
Address access time	t _{AA}		70		85		100	ns
$\overline{\text{CE1}}$ access time	t _{CA1}		70		85		100	ns
CE2 access time	t _{CA2}		70		85		100	ns
$\overline{\text{OE}}$ access time	t _{OA}		35		45		50	ns
Output hold time	t _{OH}	10		10		10		ns
$\overline{\text{CE1}}$ - output enable time	t _{COE1}	10		10		10		ns
CE2 - output enable time	t _{COE2}	10		10		10		ns
$\overline{\text{OE}}$ - output enable time	t _{OOE}	5		5		5		ns
$\overline{\text{CE1}}$ - output disable time	t _{COD1}		30		35		35	ns
CE2 - output disable time	t _{COD2}		30		35		35	ns
$\overline{\text{OE}}$ - output disable time	t _{OOD}		25		25		25	ns

Write Cycle

Parameter	Symbol	LC3564S, SS, SM, ST						Unit
		-70		-85		-10		
		min	max	min	max	min	max	
Write cycle time	t _{WC}	70		85		100		ns
Address setup time	t _{AS}	0		0		0		ns
Write pulse width	t _{WP}	50		55		55		ns
$\overline{\text{CE1}}$ setup time	t _{CW1}	60		65		65		ns
CE2 setup time	t _{CW2}	60		65		65		ns
Write recovery time	t _{WR}	0		0		0		ns
$\overline{\text{CE1}}$ write recovery time	t _{WR1}	0		0		0		ns
CE2 write recovery time	t _{WR2}	0		0		0		ns
Data setup time	t _{DS}	35		40		40		ns
Data hold time	t _{DH}	0		0		0		ns
$\overline{\text{CE1}}$ data hold time	t _{DH1}	0		0		0		ns
CE2 data hold time	t _{DH2}	0		0		0		ns
$\overline{\text{WE}}$ - output enable time	t _{WOE}	5		5		5		ns
$\overline{\text{WE}}$ - output disable time	t _{WOD}		30		35		35	ns

3V Operation

DC Recommended Operating Ranges at $T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 2.7$ to 3.3V

Parameter	Symbol	min	typ	max	Unit
Supply voltage	V_{CC}	2.7	3.0	3.3	V
Input voltage	V_{IH}	$V_{CC} - 0.2$		V_{CC}	V
	V_{IL}	0		0.2	V

DC Electrical Characteristics at $T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 2.7$ to 3.3V

Parameter		Symbol	Conditions		min	typ*	max	Unit	
Input leakage current		I_{LI}	$V_{IN} = 0$ to V_{CC}		-1.0		+1.0	μA	
I/O leakage current		I_{LO}	$V_{CE1} = V_{IH}$ or $V_{CE2} = V_{IL}$ or $V_{OE} = V_{IH}$ or $V_{WE} = V_{IL}$, $V_{I/O} = 0$ to V_{CC}		-1.0		+1.0	μA	
Output high level voltage		V_{OH}	$I_{OH} = -0.5\text{mA}$		$V_{CC} - 0.2\text{V}$			V	
Output low level voltage		V_{OL}	$I_{OL} = 1.0\text{mA}$				0.2	V	
Operating current	$V_{CC} - 0.2\text{V}/0.2\text{V}$ input	I_{CCA1}	$V_{CE1} \leq V_{IL}$, $V_{CE2} \geq V_{IH}$, $I_{I/O} = 0\text{mA}$, $V_{IN} \leq V_{IL}$, $V_{IN} \geq V_{IH}$		$T_a \leq 70^\circ\text{C}$	0.01	0.8	μA	
					$T_a \leq 85^\circ\text{C}$		2.5		
		I_{CCA4}	$V_{CE1} \leq V_{IL}$, $V_{CE2} \geq V_{IH}$, $I_{I/O} = 0\text{mA}$, DUTY = 100%	min cycle	LC3564S, SS, SM, ST-70			20	mA
					LC3564S, SS, SM, ST-85			20	
					LC3564S, SS, SM, ST-10			10	
				1 μs cycle		3	mA		
Standby current	$V_{CC} - 0.2\text{V}/0.2\text{V}$ input	I_{CCS1}	$V_{CE2} \leq V_{IL}$ or $V_{CE1} \geq V_{IH}$ $V_{CE2} \geq V_{IH}$		$T_a \leq 70^\circ\text{C}$	0.01	0.8	μA	
					$T_a \leq 85^\circ\text{C}$		2.5		

*) Reference value at $V_{CC} = 3\text{V}$, $T_a = 25^\circ\text{C}$

LC3564S, SS, SM, ST-70/85/10

AC Electrical Characteristics at $T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 2.7$ to 3.3V

AC test conditions

Input pulse levels	: $V_{IH} = V_{CC} - 0.2\text{V}$, $V_{IL} = 0.2\text{V}$
Input rise and fall time	: 10ns
Input and output timing reference levels	: 1.5V
Output load	LC3564S, SS, SM, ST-70 : 30pF (including scope and jig)
	LC3564S, SS, SM, ST-85/10 : 100pF (including scope and jig)

Read Cycle

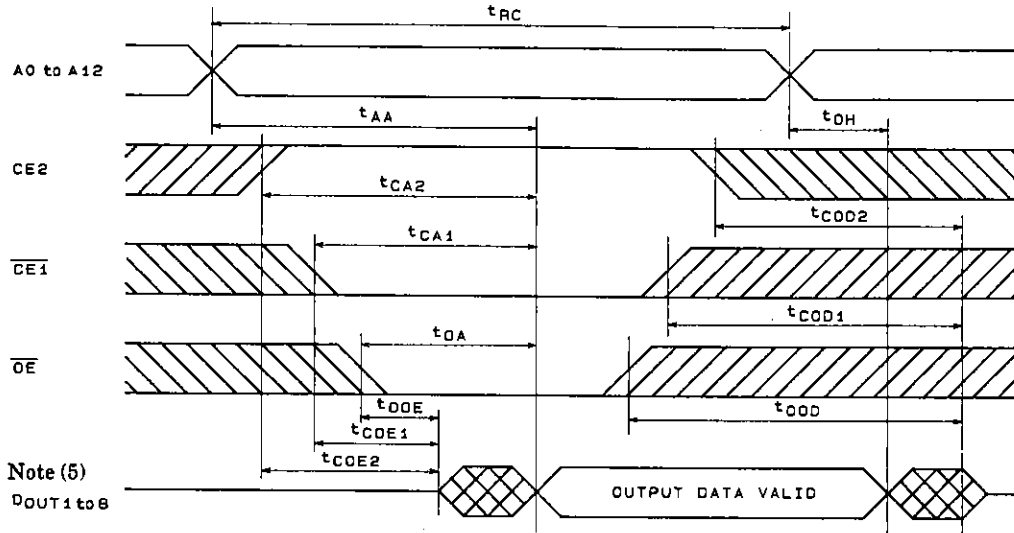
Parameter	Symbol	LC3564S, SS, SM, ST						Unit
		-70		-85		-10		
		min	max	min	max	min	max	
Read cycle time	t_{RC}	200		250		500		ns
Address access time	t_{AA}		200		250		500	ns
$\overline{CE1}$ access time	t_{CA1}		200		250		500	ns
CE2 access time	t_{CA2}		200		250		500	ns
\overline{OE} access time	t_{OA}		100		130		250	ns
Output hold time	t_{OH}	20		20		20		ns
$\overline{CE1}$ – output enable time	t_{COE1}	20		20		20		ns
CE2 – output enable time	t_{COE2}	20		20		20		ns
\overline{OE} – output enable time	t_{OOE}	10		10		10		ns
$\overline{CE1}$ – output disable time	t_{COD1}		60		80		120	ns
CE2 – output disable time	t_{COD2}		60		80		120	ns
\overline{OE} – output disable time	t_{OOD}		50		70		100	ns

Write Cycle

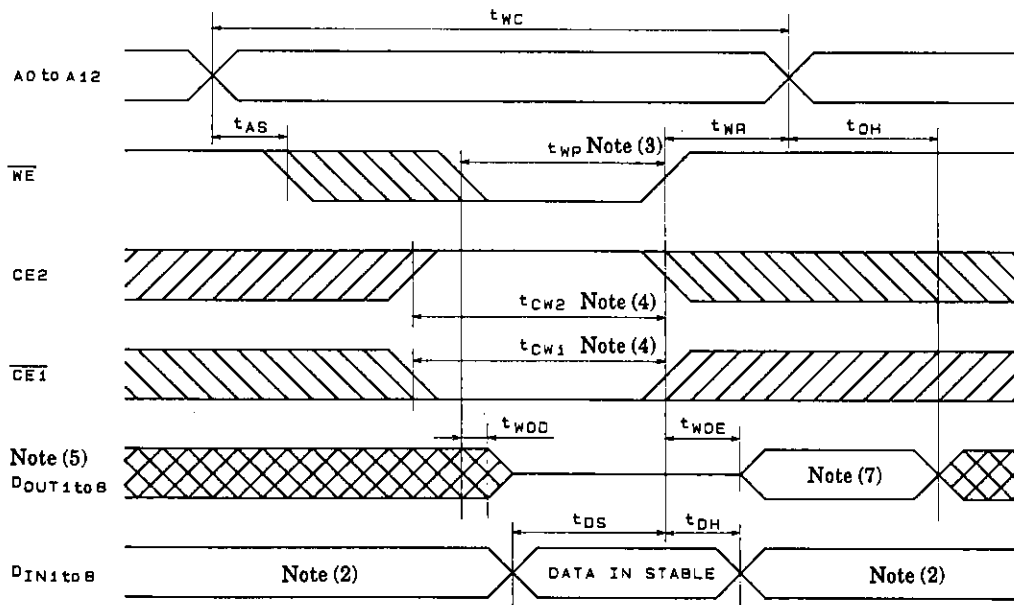
Parameter	Symbol	LC3564S, SS, SM, ST						Unit
		-70		-85		-10		
		min	max	min	max	min	max	
Write cycle time	t_{WC}	200		250		500		ns
Address setup time	t_{AS}	0		0		0		ns
Write pulse width	t_{WP}	140		160		200		ns
$\overline{CE1}$ setup time	t_{CW1}	150		180		250		ns
CE2 setup time	t_{CW2}	150		180		250		ns
Write recovery time	t_{WR}	0		0		0		ns
$\overline{CE1}$ write recovery time	t_{WR1}	0		0		0		ns
CE2 write recovery time	t_{WR2}	0		0		0		ns
Data setup time	t_{DS}	130		150		180		ns
Data hold time	t_{DH}	0		0		0		ns
$\overline{CE1}$ data hold time	t_{DH1}	0		0		0		ns
CE2 data hold time	t_{DH2}	0		0		0		ns
\overline{WE} – output enable time	t_{WOE}	10		10		10		ns
\overline{WE} – output disable time	t_{WOD}		60		80		120	ns

Timing Waveform

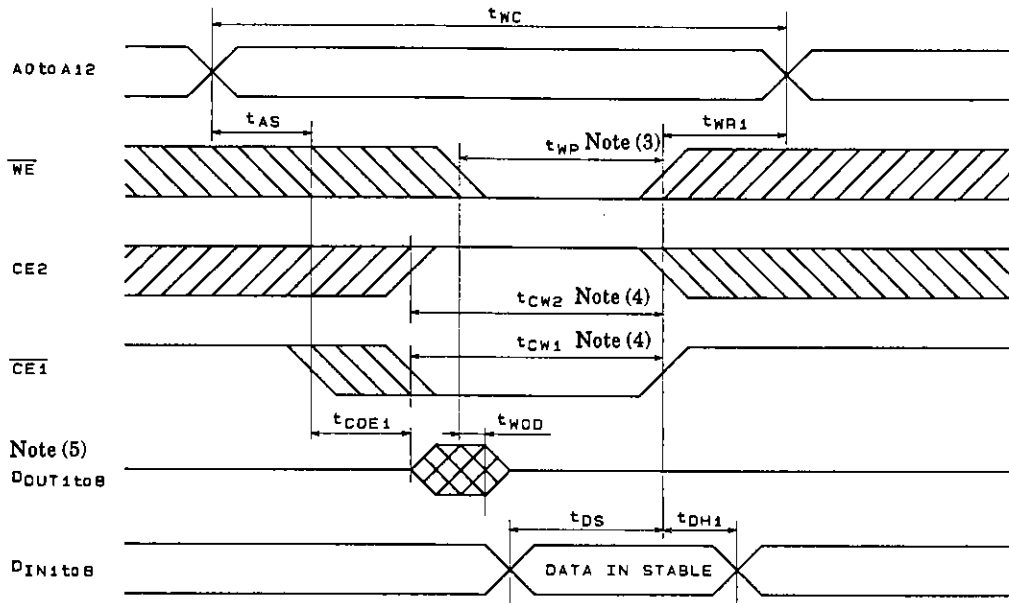
Read Cycle Note (1)



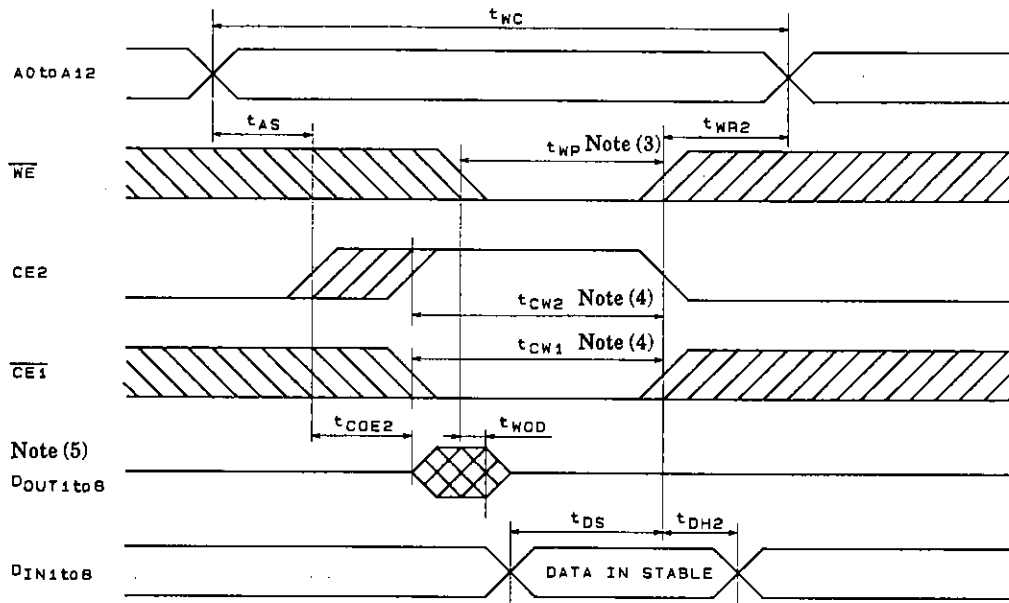
Write Cycle 1 (\overline{WE} Write) Note (6)



Write Cycle 2 ($\overline{CE1}$ Write) Note (6)



Write Cycle 3 (CE2 Write) Note (6)



Notes : (1) In Read Cycle, \overline{WE} should be high.

(2) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

(3) A write occurs during the overlap of a low $\overline{CE1}$, a high CE2 and a low \overline{WE} .
 A write begins at the latest transition among $\overline{CE1}$ going low, CE2 going high and \overline{WE} going low.
 A write ends at the earliest transition among $\overline{CE1}$ going high, CE2 going low and \overline{WE} going high.

t_{WP} is measured from the beginning of write to the end of write.

(4) t_{CW1} , t_{CW2} are measured from the later of $\overline{CE1}$ going low or CE2 going high to the end of write.

(5) If one of these conditions (\overline{OE} is high, $\overline{CE1}$ is high, CE2 is low, \overline{WE} is low) at least is satisfied, D_{OUT} goes to high impedance state.

(6) In Write Cycle, $\overline{OE} = V_{IH}$ or V_{IL} .

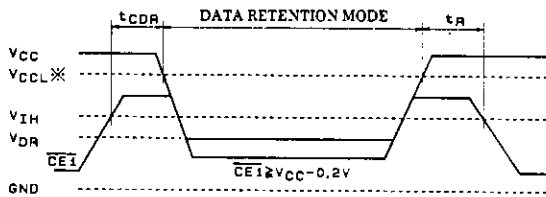
(7) D_{OUT} is in the same phase of written data of this cycle.

Data Retention Characteristics at $T_a = -40$ to $+85^\circ\text{C}$

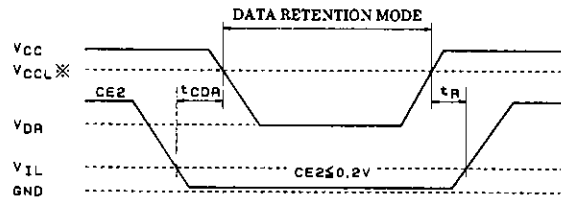
Parameter	Symbol	Conditions	min	typ	max	Unit
Date retention supply voltage	V_{DR}	$V_{CE2} \leq 0.2\text{V}$, or $V_{CE1} \geq V_{CC} - 0.2\text{V}$ or $V_{CE2} \geq V_{CC} - 0.2\text{V}$	2.0		5.5	V
Data retention current	I_{CCDR}	$V_{CC} = 3\text{V}$, $V_{CE2} \leq 0.2\text{V}$, or $V_{CE1} \geq V_{CC} - 0.2\text{V}$ or $V_{CE2} \geq V_{CC} - 0.2\text{V}$	$T_a \leq 70^\circ\text{C}$		0.8	μA
			$T_a \leq 85^\circ\text{C}$		2.5	
Chip enable setup time	t_{CDR}		0			ns
Chip enable hold time	t_R		t_{RC}^*			ns

*) t_{RC} = Read Cycle Time

Data Retention Waveform (1) ($\overline{CE1}$ CONTROL)



Data Retention Waveform (2) (CE2 CONTROL)



*) V_{CCL} — $\begin{cases} 5\text{V operation} : 4.5\text{V} \\ 3\text{V operation} : 2.7\text{V} \end{cases}$

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