



# LC35V1000BM, BTS-70U

## Asynchronous Silicon Gate 1M (131,072 words ×8 bits) SRAM

### Preliminary

### Overview

The LC35V1000BM and LC35V1000BTS-70U are asynchronous silicon gate CMOS static RAM devices with a 131,072-word by 8-bit structure. They provide two chip enable pins (CE1 and CE2) for device select/deselect control and one output enable pin (OE) for output control. They feature high speed, low power, and a wide operating temperature range. This makes them optimal for use in systems that require high speed, low power, and battery backup. They also support easy memory expansion.

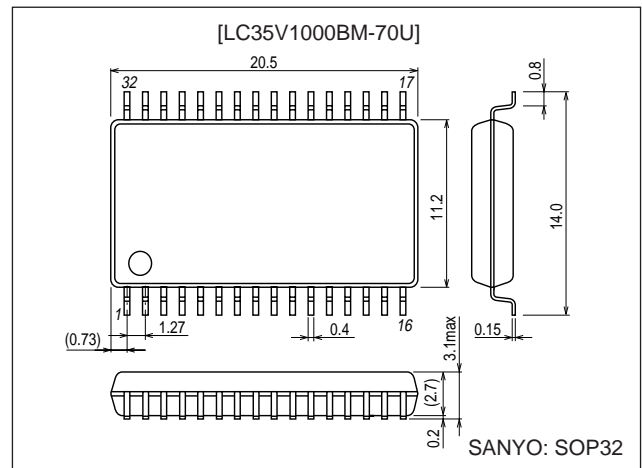
### Features

- Low-voltage operation: 3.0 to 3.6 V
- Wide operating temperature range: -40 to +85°C
- Access time: 70 ns (maximum): LC35V1000BM and LC35V1000BTS-70U.
- Low current drain  
Standby mode: 0.05  $\mu$ A (typical\*) at Ta = +25°C \*:  
When V<sub>CC</sub> = 3.0 V  
10.0  $\mu$ A (maximum) at Ta = +70°C  
20.0  $\mu$ A (maximum) at Ta = +85°C
- Data retention voltage: 2.0 to 3.6 V
- No clock required (fully static circuits)
- Input/output shared function pins, 3-state output pins
- Package  
32-pin SOP (525 mil) plastic package:  
LC35V1000BM  
32-pin TSOP (8 ×14 mm) plastic package:  
LC35V1000BTS

### Package Dimensions

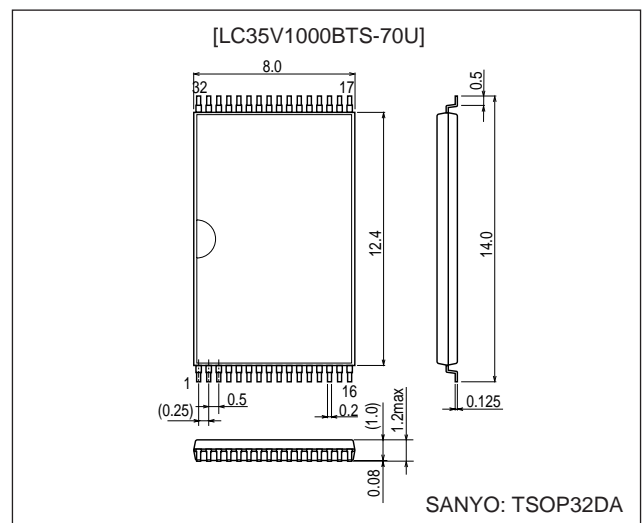
unit: mm

#### 3205A-SOP32



unit: mm

#### 3228A-TSOP32DA



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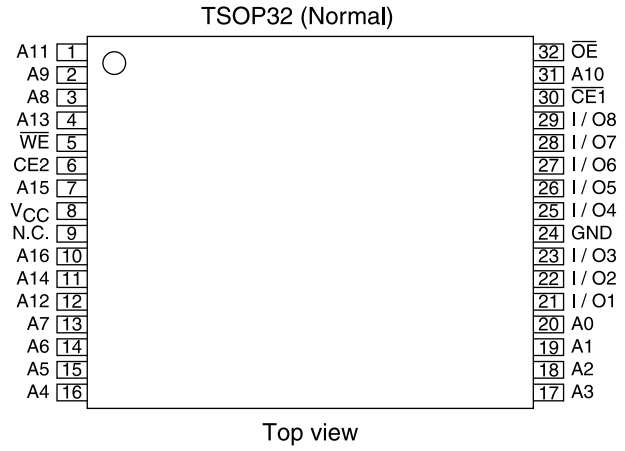
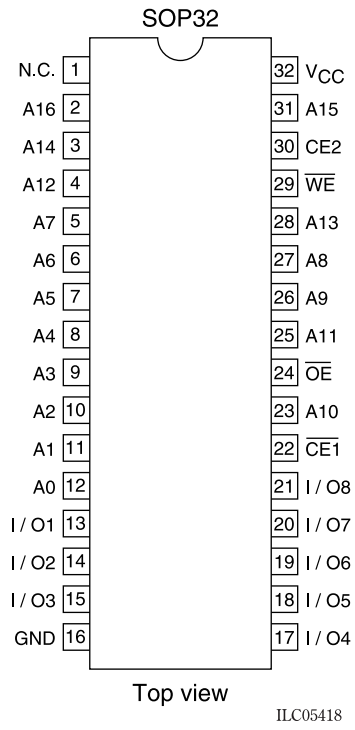
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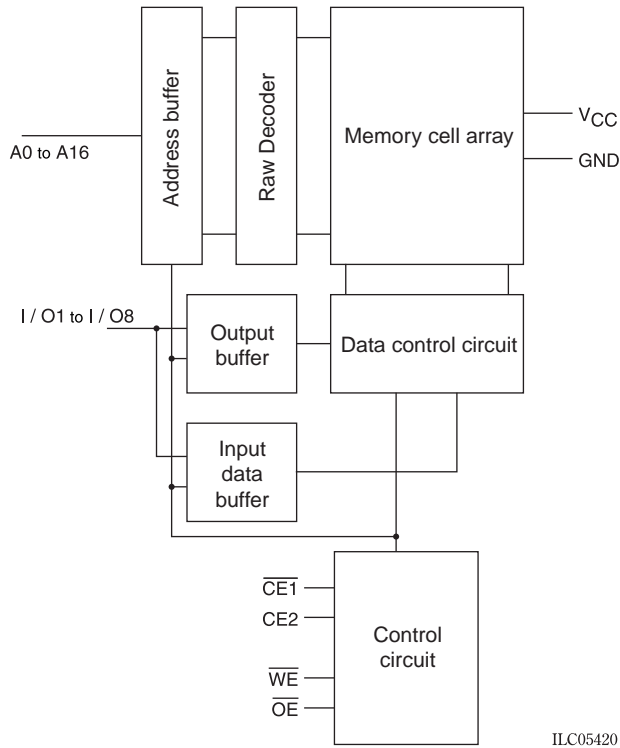
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## Pin Assignment



# LC35V1000BM, BTS-70U

## Block Diagram



ILC05420

## Pin Functions

A0 to A16	Address input
$\overline{WE}$	Ready/write control input
$\overline{OE}$	Output enable input
$\overline{CE1}$ , $CE2$	Chip enable input
I/O1 to I/O8	Data I/O
$V_{CC}$ , GND	Power supply, ground

## Function Table

Mode	$\overline{CE1}$	$CE2$	$\overline{OE}$	$\overline{WE}$	I/O	Supply current
Ready cycle	L	H	L	H	Data output	$I_{CCA}$
Write cycle	L	H	X	L	Data input	$I_{CCA}$
Output disable	L	H	H	H	High impedance	$I_{CCA}$
Unselected	H	X	X	X	High impedance	$I_{CCS}$
	X	L	X	X	High impedance	$I_{CCS}$

Note: X indicates H or L.

## Specifications

### Maximum Ratings at $T_a = 25^\circ C$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC \max}$		4.6	V
Input pin voltage	$V_{IN}$		-0.3* to $V_{CC} + 0.3$	V
I/O pin voltage	$V_{I/O}$		-0.3 to $V_{CC} + 0.3$	V
Operating temperature	$T_{opr}$		-40 to +85	$^\circ C$
Storage temperature	$T_{stg}$		-55 to +125	$^\circ C$

\*: For pulse widths under 30 ns: -2.0 V

Note: This chip may be destroyed if any stress in excess of the absolute maximum ratings is applied.

### I/O Capacitances at $T_a = 25^\circ C$ , $f = 1 \text{ MHz}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input capacitance	$C_{IN}$	$V_{IN} = 0 \text{ V}$		6	10	pF
I/O capacitance	$C_{I/O}$	$V_{I/O} = 0 \text{ V}$		6	10	pF

Note: These parameters are not measured for all devices, but are sampled values.

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### DC Allowable Operating Range at Ta = -40 to +85°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{CC}$		3.0	3.3	3.6	V
High-level input voltage	$V_{IH}$		$0.8V_{CC}$		$V_{CC} + 0.3$	V
Low-level input voltage	$V_{IL}$		-0.3*		$0.2V_{CC}$	V

Note: \* The minimum value is -2.0 V for pulse width under 30 ns.

### DC Electrical Characteristics at Ta = -40 to +85°C, V<sub>CC</sub> = 3.0 to 3.6 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input leakage current	$I_{LI}$	$V_{IN} = 0$ to $V_{CC}$	-1.0		+1.0	μA
I/O leakage current	$I_{LO}$	$\overline{V_{CE1}} = V_{IH}$ or $V_{CE2} = V_{IL}$ or $\overline{V_{OE}} = V_{IH}$ or $\overline{V_{WE}} = V_{IL}$ , $V_{I/O} = 0$ to $V_{CC}$	-1.0		+1.0	μA
Output high-level voltage	$V_{OH1}$	$V_{OH1} = -2.0$ mA	$V_{CC} - 0.4$			V
	$V_{OH2}$	$V_{OH2} = -100$ μA	$V_{CC} - 0.1$			V
Output low-level voltage	$V_{OL1}$	$V_{OL1} = 2.0$ mA			0.4	V
	$V_{OL2}$	$V_{OL2} = -100$ μA			0.1	V
Operating supply current (CMOS inputs)	$I_{CCA2}$	$\overline{V_{CE1}} = V_{IL}$ , $V_{CE2} = V_{IH}$ , $I_{I/O} = 0$ mA, $V_{IN} = V_{IH}$ or $V_{IL}$			1.2	mA
	$I_{CCA3}$	$\overline{V_{CE1}} = V_{IL}$ , $V_{CE2} = V_{IH}$ , $I_{I/O} = 0$ mA, $V_{IN} = V_{IH}$ or $V_{IL}$ , DUTY 100%	min cycle 1 μs cycle		25 2	mA
Standby mode supply current (V <sub>CC</sub> - 0.2 V/0.2 V inputs) (CMOS inputs)	$I_{CCS1}$	$V_{CE2} \leq 0.2$ V or $(\overline{V_{CE1}} \geq V_{CC} - 0.2$ V, $V_{CE2} \geq V_{CC} - 0.2$ V)	Ta ≤ 85°C		20	μA
			Ta ≤ 70°C		10	
			Ta ≤ 25°C		0.05	
$I_{CCS2}$	$\overline{V_{CE1}} = V_{IH}$ or $V_{CE2} = V_{IL}$ , $V_{IN} = 0$ to $V_{CC}$				0.4	mA

Note: \* Reference values when V<sub>CC</sub> = 3.0 V and Ta = 25°C.

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### AC Electrical Characteristics at $T_a = -40$ to $+85^\circ\text{C}$ , $V_{CC} = 3.0$ to $3.6$ V

AC test conditions

Input pulse voltage levels:  $V_{IL} = 0.2 V_{CC}$ ,  $V_{IH} = 0.8 V_{CC}$

Input rise and fall times: 5 ns

Input and output timing levels:  $0.5 V_{CC}$

Output load: 30 pF (including the jig capacitance)

#### Read cycle

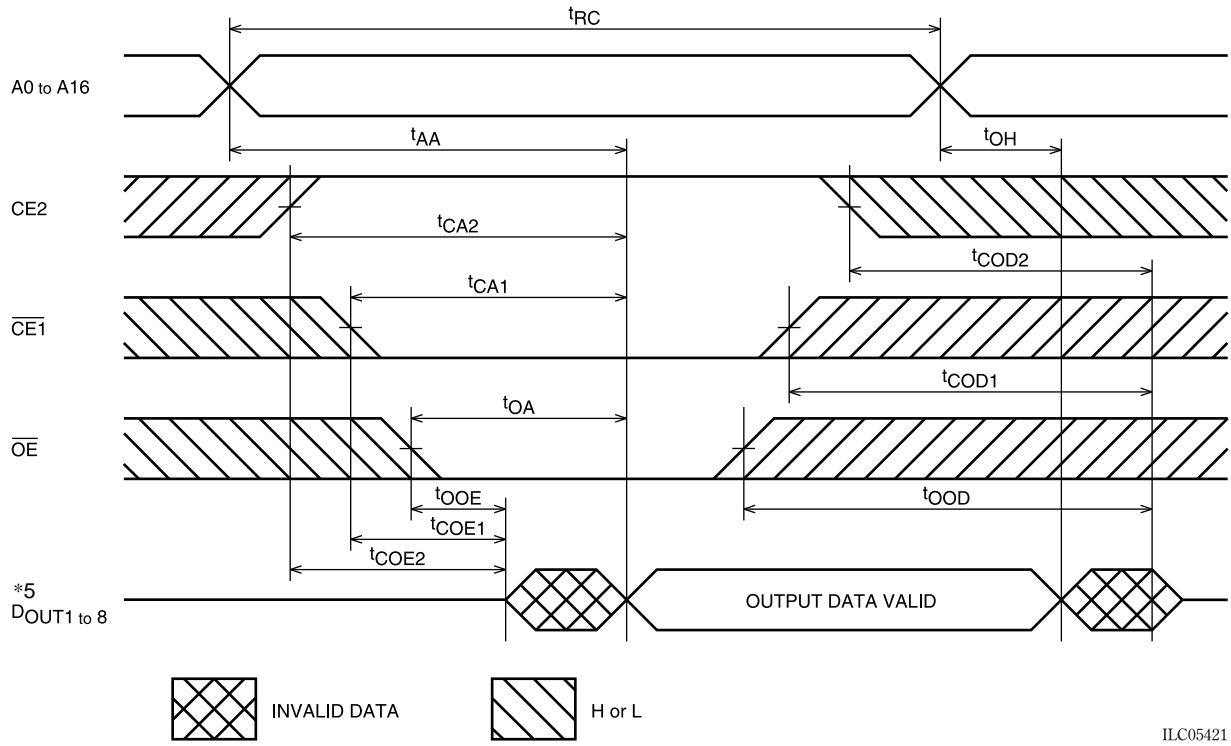
Parameter	Symbol	min	max	Unit
Read cycle time	$t_{RC}$	70		ns
Address access time	$t_{AA}$		70	ns
$\overline{CE1}$ access time	$t_{CA1}$		70	ns
CE2 access time	$t_{CA2}$		70	ns
$\overline{OE}$ access time	$t_{OA}$		40	ns
Output hold time	$t_{OH}$	10		ns
$\overline{CE1}$ output enable time	$t_{COE1}$	5		ns
CE2 output enable time	$t_{COE2}$	5		ns
$\overline{OE}$ output enable time	$t_{OCE}$	0		ns
$\overline{CE1}$ output disable time	$t_{COD1}$		35	ns
CE2 output disable time	$t_{COD2}$		35	ns
$\overline{OE}$ output disable time	$t_{OOD}$		30	ns

#### Write cycle

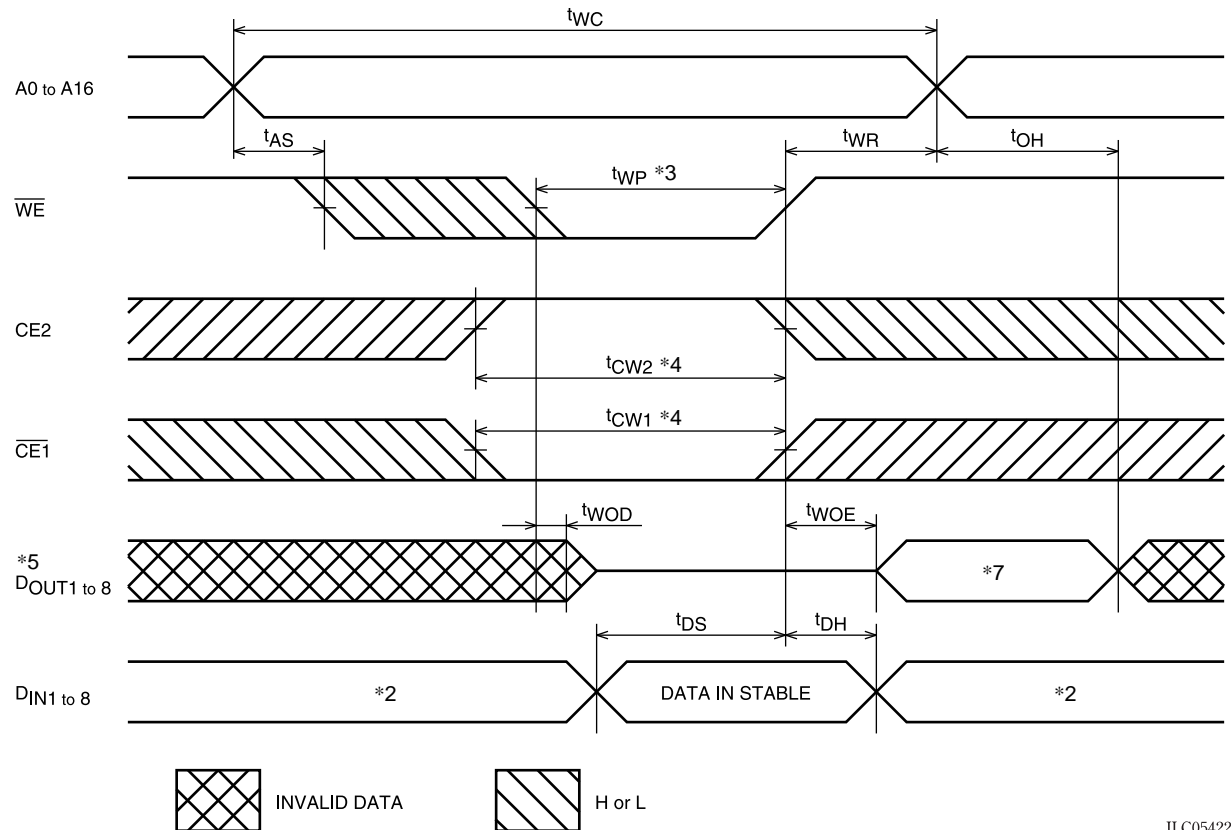
Parameter	Symbol	min	max	Unit
Write cycle time	$t_{WC}$	70		ns
Address setup time	$t_{AS}$	0		ns
Write pulse width	$t_{WP}$	50		ns
$\overline{CE1}$ setup time	$t_{CW1}$	60		ns
CE2 setup time	$t_{CW2}$	60		ns
Write recovery time	$t_{WR}$	0		ns
$\overline{OE1}$ write recovery time	$t_{WR1}$	0		ns
CE2 write recovery time	$t_{WR2}$	0		ns
Data setup time	$t_{DS}$	40		ns
Data hold time	$t_{DH}$	0		ns
$\overline{OE1}$ data hold time	$t_{DH1}$	0		ns
CE2 data hold time	$t_{DH2}$	0		ns
$\overline{WE}$ output enable time	$t_{WOE}$	5		ns
$\overline{WE}$ output disable time	$t_{WOD}$		35	ns

Timing Charts

Read cycle (1)

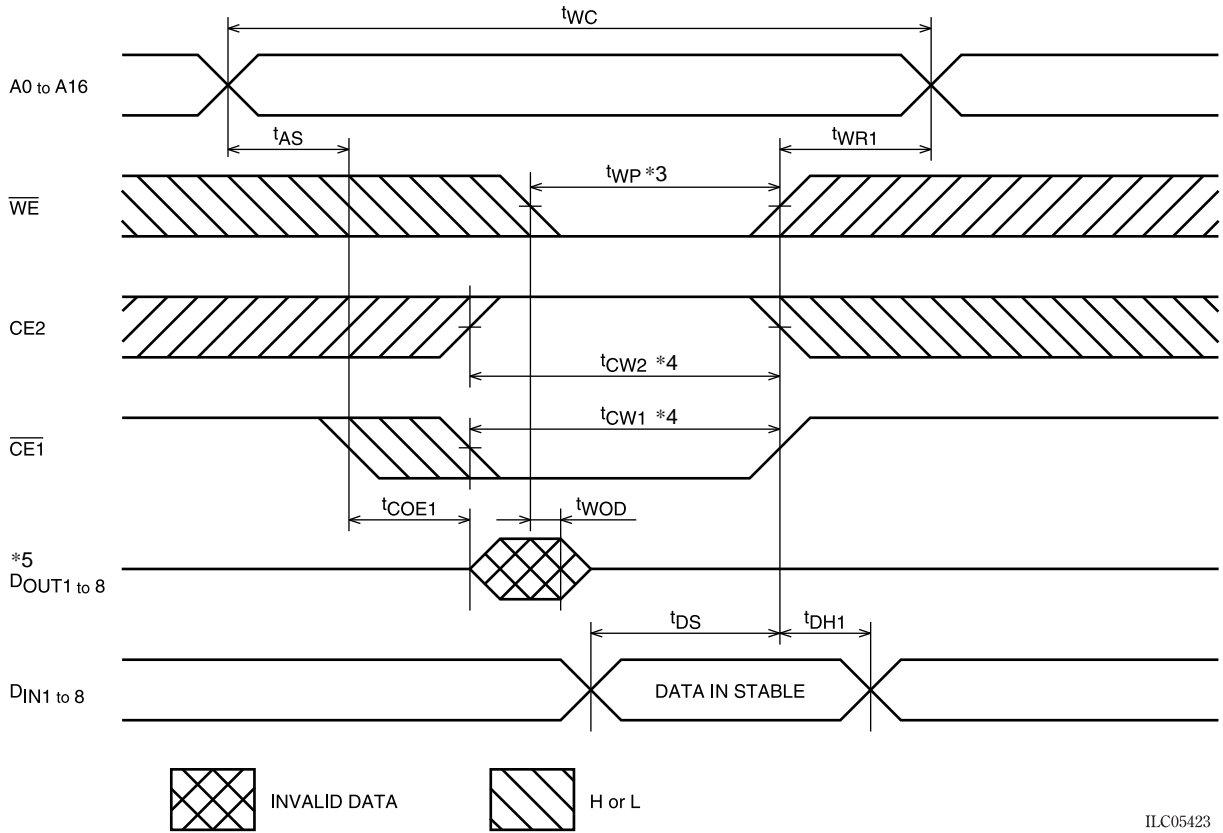


Write cycle (1) ( $\overline{WE}$  write)



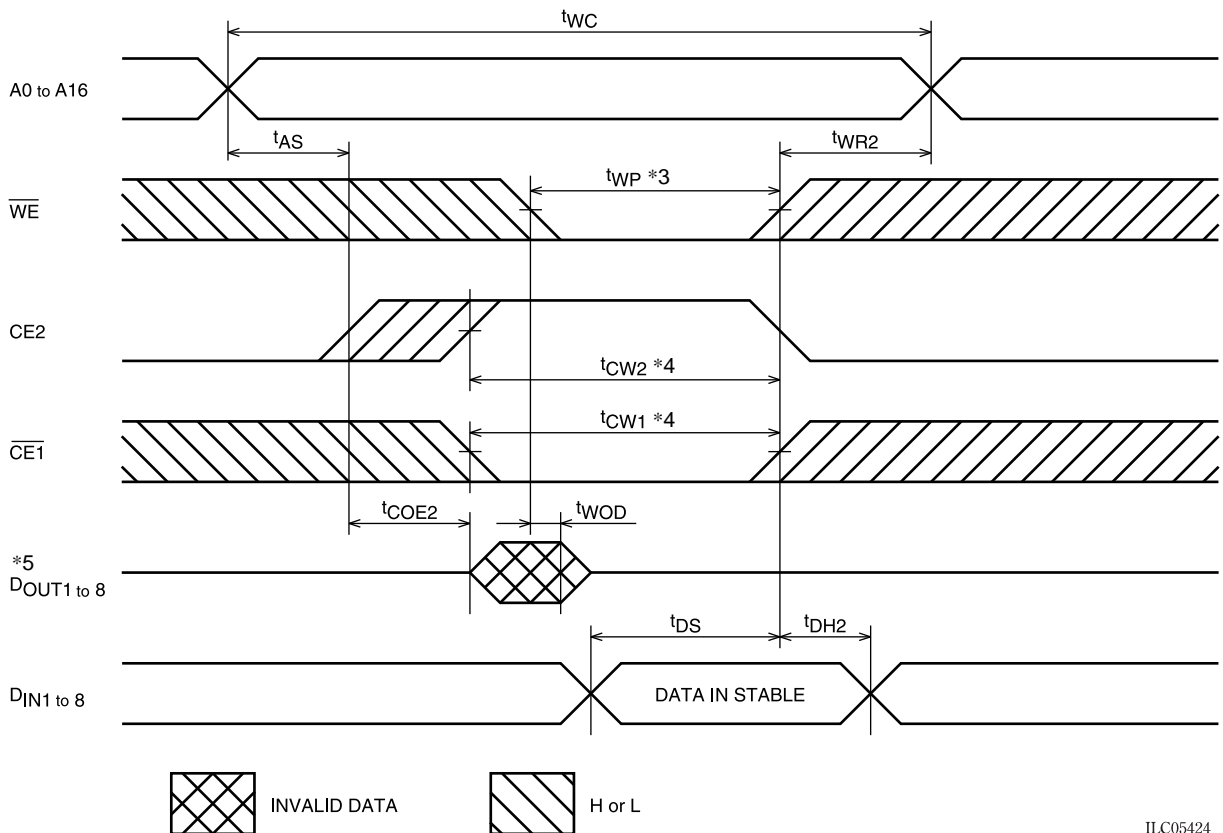
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Write cycle (2) ( $\overline{\text{CE1}}$  write)



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Write cycle (2) ( $\text{CE2}$  write)



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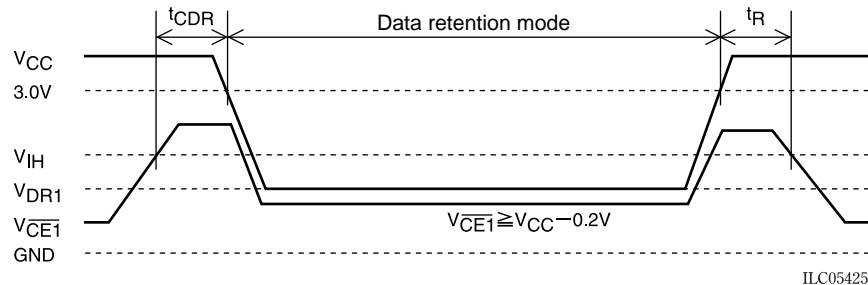
- Notes:
1. The times  $t_{COD1}$ ,  $t_{COD2}$ ,  $t_{OOD}$ , and  $t_{WOD}$  are stipulated as the times until the output reaches the high-impedance state. They are not stipulated by output voltage level.
  2. Do not apply reverse phase signals to the data outputs when the data outputs are in the output state.
  3.  $t_{WP}$  is the period that  $\overline{CE1}$  and  $\overline{WE}$  are at the low level and CE2 is at the high level, and is defined as the time from the fall of  $\overline{WE}$  until the rise of  $\overline{CE1}$  or  $\overline{WE}$  or the fall of CE2, whichever occurs first.
  4.  $t_{CW1}$  and  $t_{CW2}$  are the period that  $\overline{CE1}$  and  $\overline{WE}$  are at the low level and CE2 is at the high level, and are defined as the time from the fall of  $\overline{CE1}$  or the rise of CE2 to the rise of either  $\overline{CE1}$  or  $\overline{WE}$  or the fall of CE2, whichever occurs first.
  5. The data outputs go to the high-impedance state when any one of the following states hold:  $\overline{OE}$  is at the high level,  $\overline{CE1}$  is at the high level, CE2 is at the low level, or  $\overline{WE}$  is at the low level.
  6. If  $\overline{OE}$  is at the high level during the write cycle, the data outputs will go to the high-impedance state.

### Data Retention Characteristics at $T_a = -40$ to $+85^\circ\text{C}$

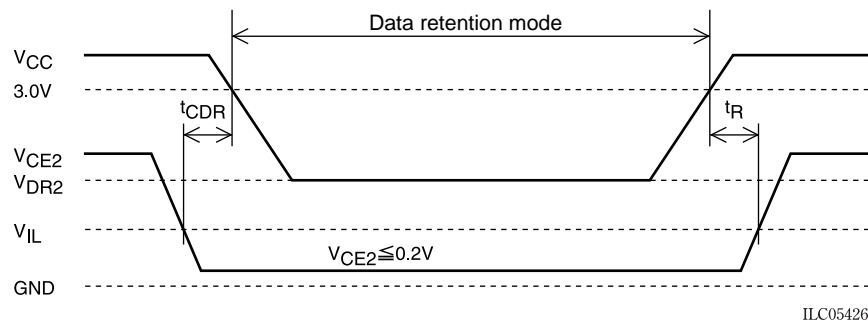
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Data retention supply voltage	$V_{DR1}$	$V_{\overline{CE1}} \geq V_{CC} - 0.2\text{ V}$ , $V_{CE2} \geq V_{CC} - 0.2\text{ V}$ or $V_{CE2} \leq 0.2\text{ V}$	2.0		3.6	V
	$V_{DR2}$	$V_{CE2} \leq 0.2\text{ V}$	2.0		3.6	V
Data retention supply current	$I_{CCDR1}$	$V_{CC} = 3.0\text{ V}$ , $V_{\overline{CE1}} \geq V_{CC} - 0.2\text{ V}$ , $V_{CE2} \geq V_{CC} - 0.2\text{ V}$ , or $V_{CE2} \leq 0.2\text{ V}$			16	$\mu\text{A}$
			-40°C to +85°C			
			-40°C to +70°C		8	
Chip enable setup time	$t_{CDR}$		0			ns
Chip enable hold time	$t_R$		5			ms

Note: \*  $T_a = +25^\circ\text{C}$

### Data Retention Waveforms (1) ( $\overline{CE1}$ control)



### Data Retention Waveforms (2) ( $CE2$ control)





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