



## LC35V256EM, ET-70W

256K (32K words × 8 bits) SRAM  
Control pins:  $\overline{OE}$  and  $\overline{CE}$

### Overview

The LC35V256EM-70W and LC35V256ET-70W are asynchronous silicon-gate CMOS SRAMs with a 32768-word by 8-bit structure. These are full-CMOS devices with 6 transistors per memory cell, and feature ultralow-voltage operation, a low operating current drain, and an ultralow standby current. Control inputs include  $\overline{OE}$  for fast memory access and  $\overline{CE}$  for power saving and device selection. This makes these devices optimal for systems that require low power or battery backup, and makes memory expansion easy. The ultralow standby current allows these devices to be used with capacitor backup as well.

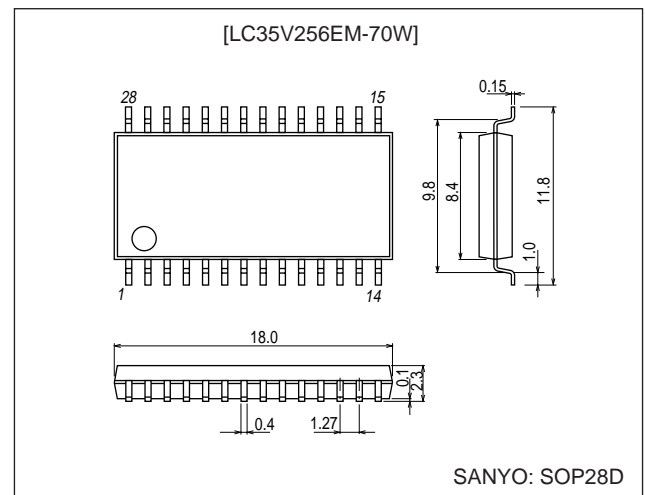
### Features

- Supply voltage range: 3.0 to 3.6 V
- Access time: 70 ns (maximum)
- Standby current: 0.8  $\mu$ A ( $T_a \leq 60^\circ\text{C}$ )  
4.0  $\mu$ A ( $T_a \leq 70^\circ\text{C}$ )
- Operating temperature:  $-10$  to  $+70^\circ\text{C}$
- Data retention voltage: 2.0 to 3.6 V
- All I/O levels: CMOS compatible (0.8  $V_{CC}$ , 0.2  $V_{CC}$ )
- Input/output shared function pins, 3-state output pins
- No clock required (fully static circuits)
- Package
  - 28-pin SOP (450 mil) plastic package:  
LC35V256EM-70W
  - 28-pin TSOP (8 × 13.4 mm) plastic package:  
LC35V256ET-70W

### Package Dimensions

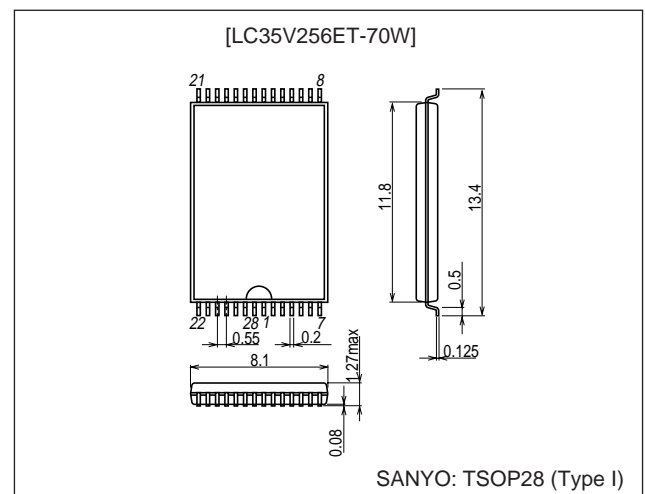
unit: mm

#### 3187A-SOP28D



unit: mm

#### 3221-TSOP28 (Type I)



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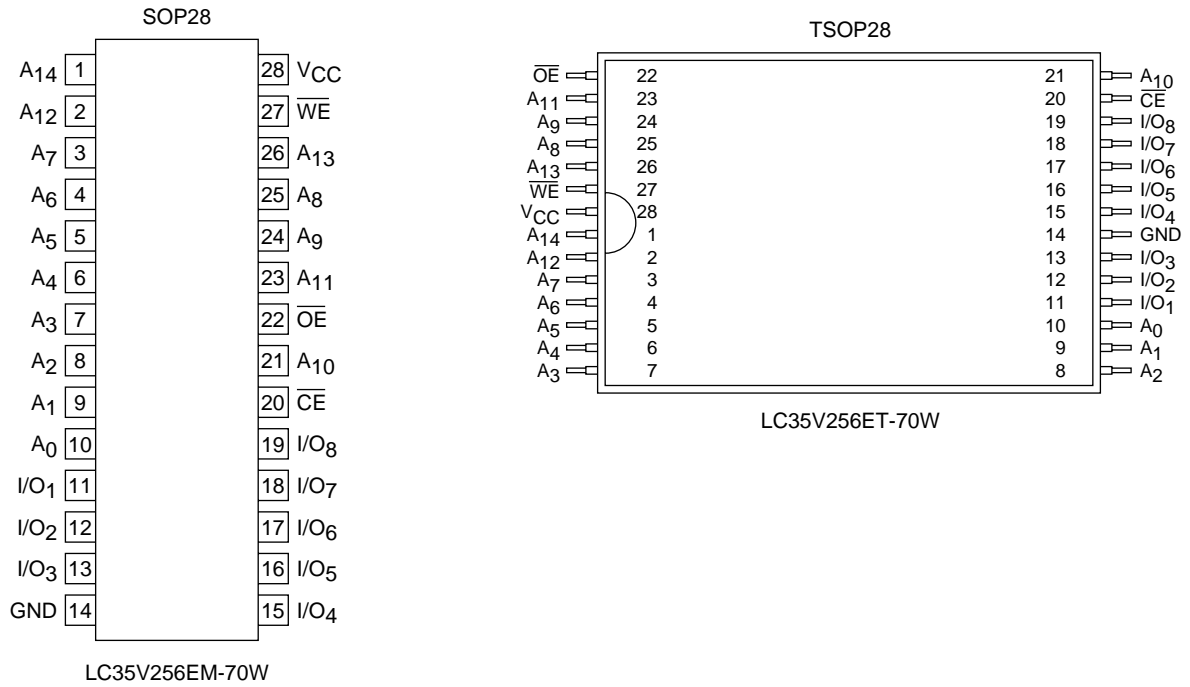
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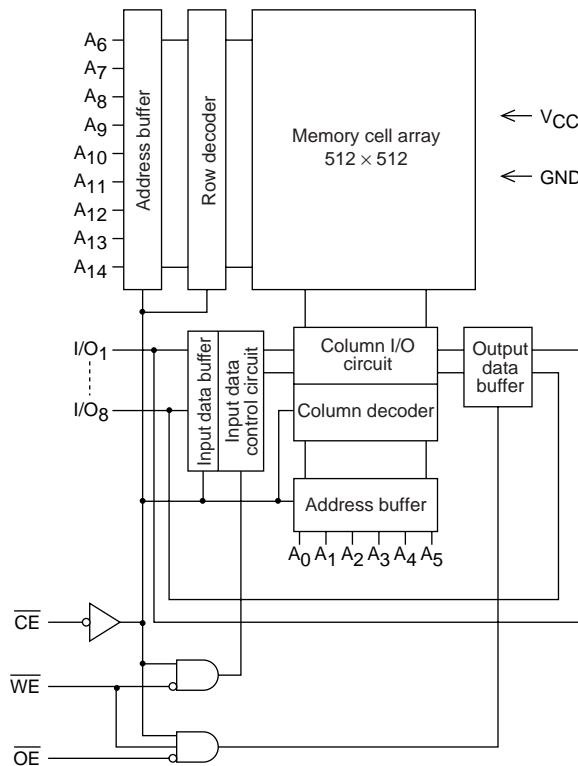
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# LC35V256EM, ET70W

## Pin Assignment (Top view)



## Block Diagram



## LC35V256EM, ET70W

### Pin Functions

A0 to A14	Address input
$\overline{WE}$	Read/write control input
$\overline{OE}$	Output enable input
$\overline{CE}$	Chip enable input
I/O1 to I/O8	Data I/O
$V_{CC}$ , GND	Power supply, ground

### Function Table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Supply current
Read cycle	L	L	H	Data output	$I_{CCA}$
Write cycle	L	X	L	Data input	$I_{CCA}$
Output disable	L	H	H	High impedance	$I_{CCA}$
Unselected	H	X	X	High impedance	$I_{CCS}$

Note: X indicates H or L.

## Specifications

### Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC\ max}$		4.6	V
Input pin voltage	$V_{IN}$		-0.3* to $V_{CC} + 0.3$	V
I/O pin voltage	$V_{I/O}$		-0.3 to $V_{CC} + 0.3$	V
Operating temperature	$T_{opr}$		-10 to +70	°C
Storage temperature	$T_{stg}$		-55 to +125	°C

Note: \* The minimum value is -2.0 V for pulse widths under 30 ns.

### I/O Capacitances at $T_a = 25^\circ\text{C}$ , $f = 1\ \text{MHz}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
I/O pin capacitance	$C_{I/O}$	$V_{I/O} = 0\ \text{V}$		6	10	pF
Input pin capacitance	$C_I$	$V_{IN} = 0\ \text{V}$		6	10	pF

Note: All units are not tested; only samples are tested.

### DC Allowable Operating Ranges at $T_a = -10\ \text{to}\ +70^\circ\text{C}$ , $V_{CC} = 3.0\ \text{to}\ 3.6\ \text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{CC}$		3.0	3.3	3.6	V
Input voltage	$V_{IH}$		$0.8V_{CC}$		$V_{CC} + 0.3$	V
	$V_{IL}$		-0.3*		$0.2V_{CC}$	V

Note: \* The minimum value is -2.0 V for pulse widths under 30 ns.

## LC35V256EM, ET70W

### DC Electrical Characteristics at Ta = -10 to +70°C, VCC = 3.0 to 3.6 V

Parameter	Symbol	Conditions	Ratings			Unit		
			min	typ	max			
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = 0 to V <sub>CC</sub>	-1.0		+1.0	μA		
Output leakage current	I <sub>LO</sub>	V <sub>CE</sub> = V <sub>IH</sub> or V <sub>OE</sub> = V <sub>IH</sub> or V <sub>WE</sub> = V <sub>IL</sub> V <sub>I/O</sub> = 0 to V <sub>CC</sub>	-1.0		+1.0	μA		
Output high-level voltage	V <sub>OH1</sub>	I <sub>OH1</sub> = -2.0 mA	V <sub>CC</sub> - 0.4			V		
	V <sub>OH2</sub>	I <sub>OH2</sub> = -100 μA	V <sub>CC</sub> - 0.1			V		
Output low-level voltage	V <sub>OL1</sub>	I <sub>OL1</sub> = 2.0 mA			0.4	V		
	V <sub>OL2</sub>	I <sub>OL2</sub> = 100 μA			0.4	V		
Operating current drain	CMOS inputs	I <sub>CCA2</sub>	V <sub>CE</sub> = V <sub>IL</sub> , I <sub>I/O</sub> = 0 mA, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>		1.2	mA		
		I <sub>CCA3</sub>	V <sub>CE</sub> = V <sub>IL</sub> , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>I/O</sub> = 0 mA, DUTY 100 %	min cycle 1 μs cycle	20 1.5	25 2.5	mA mA	
Standby mode current drain	V <sub>CC</sub> - 0.2 V/ 0.2 V inputs	I <sub>CCS1</sub>	V <sub>CE</sub> ≥ V <sub>CC</sub> - 0.2 V, V <sub>IN</sub> = 0 to V <sub>CC</sub>	Ta ≤ 25°C	0.01		μA	
				Ta ≤ 60°C			0.8	μA
				Ta ≤ 70°C			4.0	μA
	CMOS inputs	I <sub>CCS2</sub>	V <sub>CE</sub> = V <sub>IH</sub> , V <sub>IN</sub> = 0 to V <sub>CC</sub>			0.4	mA	

Note: \* Reference values when V<sub>CC</sub> = 3.3 V and Ta = 25°C.

### AC Electrical Characteristics at Ta = -10 to +70°C, VCC = 3.0 to 3.6 V

AC test conditions

Input pulse voltage levels: 0.2 V<sub>CC</sub> to 0.8 V<sub>CC</sub>

Input rise and fall times: 5 ns

Input and output timing levels: 1/2 V<sub>CC</sub>

Output load: 30 pF (including the jig capacitance)

#### Read Cycle

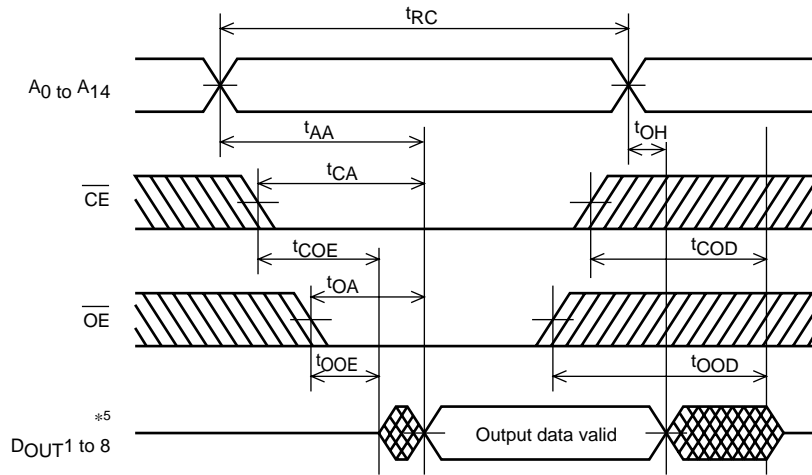
Parameter	Symbol	min	max	Unit
Read cycle time	t <sub>RC</sub>	70		ns
Address access time	t <sub>AA</sub>		70	ns
$\overline{\text{CE}}$ access time	t <sub>CA</sub>		70	ns
$\overline{\text{OE}}$ access time	t <sub>OA</sub>		50	ns
Output hold time	t <sub>OH</sub>	10		ns
$\overline{\text{CE}}$ output enable time	t <sub>COE</sub>	10		ns
$\overline{\text{OE}}$ output enable time	t <sub>OOE</sub>	5		ns
$\overline{\text{CE}}$ output disable time	t <sub>COD</sub>		35	ns
$\overline{\text{OE}}$ output disable time	t <sub>OOD</sub>		30	ns

#### Write Cycle

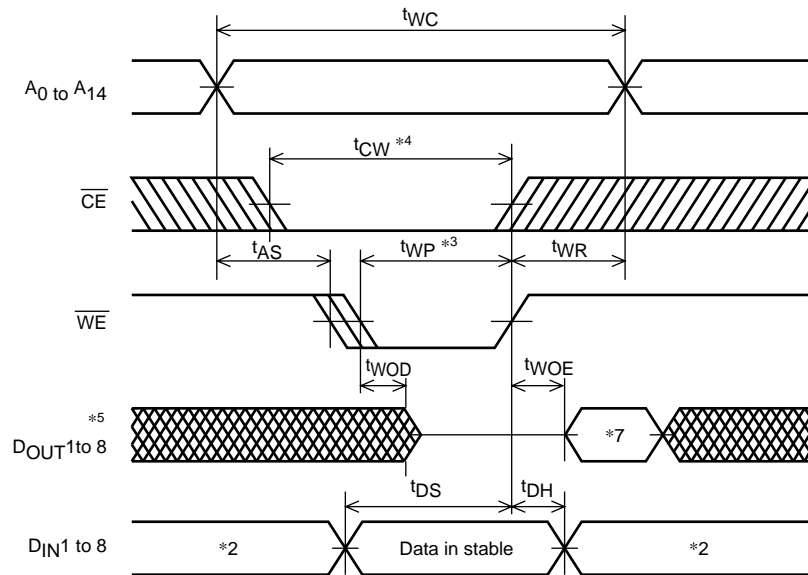
Parameter	Symbol	min	max	Unit
Write cycle time	t <sub>WC</sub>	70		ns
Address setup time	t <sub>AS</sub>	0		ns
Write pulse width	t <sub>WP</sub>	55		ns
$\overline{\text{CE}}$ setup time	t <sub>CW</sub>	60		ns
Write recovery time	t <sub>WR</sub>	0		ns
$\overline{\text{CE}}$ write recovery time	t <sub>WR1</sub>	0		ns
Data setup time	t <sub>DS</sub>	50		ns
Data hold time	t <sub>DH</sub>	0		ns
$\overline{\text{CE}}$ data hold time	t <sub>DH1</sub>	0		ns
$\overline{\text{WE}}$ output enable time	t <sub>WOE</sub>	5		ns
$\overline{\text{WE}}$ output disable time	t <sub>WOD</sub>		35	ns

Timing Charts

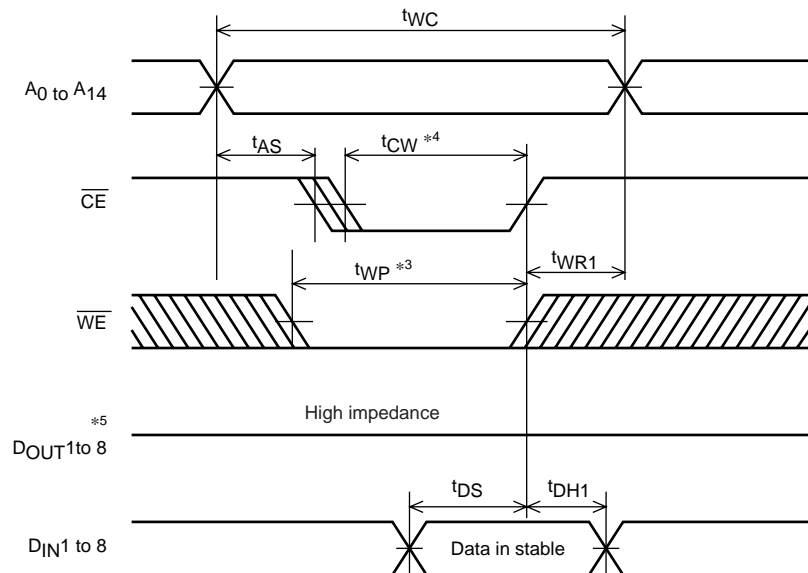
[Read cycle] \*1



[Write cycle 1] ( $\overline{\text{WE}}$  write) \*6



[Write cycle 2] ( $\overline{\text{CE}}$  write) \*6



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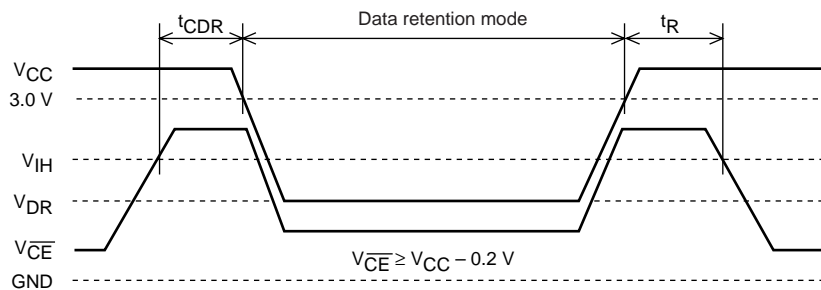
- Notes:
1.  $\overline{WE}$  must be held at the high level during the read cycle.
  2. Do not apply reverse phase signals to the DOUT pins when those pins are in the output state.
  3. The time  $t_{WP}$  is the period when both  $\overline{CE}$  and  $\overline{WE}$  are low. It is defined as the time from the fall of  $\overline{WE}$  to the rise of  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first.
  4. The time  $t_{CW}$  is the period when both  $\overline{CE}$  and  $\overline{WE}$  are low. It is defined as the time from the fall of  $\overline{CE}$  to the rise of  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first.
  5. The DOUT pins will be in the high-impedance state if any one of the following is held:  $\overline{OE}$  is at the high level,  $\overline{CE}$  is at the high level, or  $\overline{WE}$  is at the low level.
  6. The  $\overline{OE}$  pin must be either held high or held low during the write cycle.
  7. DOUT has the same phase as the write data during this write cycle.

### Data Retention Characteristics at $T_a = -10$ to $+70^\circ\text{C}$

Parameter	Symbol	Conditions	min	max	Unit
Data retention supply voltage	$V_{DR}$	$V_{\overline{CE}} \geq V_{CC} - 0.2\text{ V}$	2.0	3.6	V
Chip enable setup time	$t_{CDR}$		0		ns
Chip enable hold time	$t_R$		$t_{RC}^*$		ns

Note: \*  $t_{RC}$ : Read cycle time

### Data Retention Waveforms ( $\overline{CE}$ control)



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