

No. 4816A

LC36128ML-70/85/10

128 K (16384 words × 8 bits) SRAM

Overview

The LC36128ML are fully asynchronous silicon gate CMOS static RAMs with a 16384 words \times 8 bits configuration.

This series has a $\overline{\text{CE}}$ chip enable pin for device select/non-select control and an $\overline{\text{OE}}$ output enable pin for output control, and features high speed as well as low power dissipation.

For these reasons, the series is especially suited for use in systems requiring high speed, low power, and battery backup, and it is easy to expand memory capacity.

Features

· Access time

70 ns (max.): LC36128ML-70 85 ns (max.): LC36128ML-85 100 ns (max.): LC36128ML-10

· Low current dissipation

During standby

1 $\mu A (max.) / Ta = 25^{\circ}C$

2 $\mu A (max.) / Ta = 0 to +40^{\circ}C$

12 $\mu A \text{ (max.)} / Ta = 0 \text{ to } +70^{\circ}\text{C}$

During data retention

 $0.4 \mu A (max.) / Ta = 25^{\circ}C$

1 $\mu A \text{ (max.)} / Ta = 0 \text{ to } +40^{\circ}C$

5 μ A (max.) / Ta = 0 to +70°C

During operation (DC)

10 mA (max.)

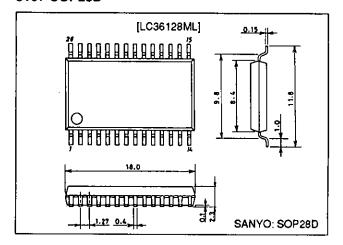
- Single 5 V power supply: $5 V \pm 10\%$
- Data retention power supply voltage: 2.0 to 5.5 V
- No clock required (Fully static memory)
- · All input and output levels are TTL compatible
- · Common input/output pins, with three output states
- Package

SOP 28-pin (450 mil) plastic package: LC36128ML

Package Dimensions

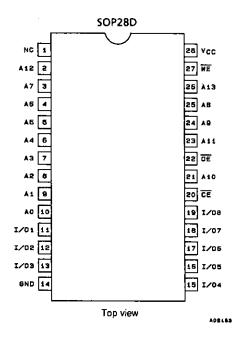
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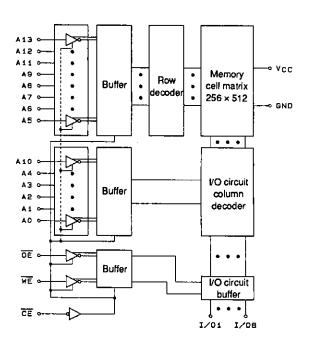
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Pin Assignment

Block Diagram





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Pin Functions

A0 to A13	Address input
WE	Read/write control input
Œ	Output enable input
CE	Chip enable input
I/O1 to I/O8	Data input/output
V _{CC} , GND	Power supply pins

Functions Logic

Mode	CE	ŌĒ	WE	VO	Supply current
Read cycle	L	L	H	Data output	ICCA
Write cycle	L	X	L	Data input	ICCA
Output disable	L	Н	Н	High impedance	ICCA
Non-select	Н	Х	Х	High impedance	lccs

X: H or L

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max		7.0	٧
Input pin voltage	V _{IN}		-0.5* to V _{CC} + 0.5	V
I/O pin voltage	V _{I/O}	· · · · · · · · · · · · · · · · · · ·	-0.5* to V _{CC} + 0.5	V
Allowable power dissipation	Pd max		0.7	W
Operating temperature range	Topr		0 to +70	°C
Storage temperature range	Tstg	• •	-55 to +150	•c

^{* -3.0} V when pulse width is less than 50 ns

DC Recommended Operating Ranges at Ta = 0 to +70°C

Parameter	Symbol	min	typ	max	Unit
Power supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high level voltage	V _{IH}	2.2		V _{CC} + 0.3	v
Input low level voltage	V _{IL}	-0.3*		+0.8	V

^{* -3.0} V when pulse width is less than 50 ns

DC Electrical Characteristics at Ta = 0 to +70°C, V_{CC} = 5 V \pm 10 %

Parameter	Symbol	C	Conditions	7	min	typ*	max	Unit	
Input leakage current	l _{Li}	V _{IN} = 0 to V _{CC}			-1.0		+1.0	μA	
I/O leakage current	¹ LO	$V_{\overline{CE}} = V_{IH}$ or $V_{\overline{OE}} = V_{IH}$, $V_{I/O} = 0$ to $V_{\overline{CC}}$			-1.0		+1.0	μА	
Output high level voltage	V _{OH}	I _{OH} = ~1.0 mA			2.4			V	
Output low level voltage	V _{OL}	! _{OL} = 2.1 mA					0.4	V	
Operating supply current (DC)	lcca1	$V_{\overline{CE}} \le 0.2 \text{ V, } V_{ N} \le 0.2$ $I_{ VO} = 0 \text{ mA}$	$V_{\overline{CE}} \le 0.2 \text{ V}, V_{ N} \le 0.2 \text{ V or } V_{ N} \ge V_{CC} - 0.2 \text{ V},$ $I_{ VO} = 0 \text{ mA}$			1	5	mA	
	I _{CCA2}	VCE = VIL, IVO = 0 mA		3	10	mA			
		min cycle Duty = 100%		70 ns		30	50		
Average operating supply current	I _{CCA3}		Access	85 ns		25	50	mA	
		I _{VO} = 0 mA	une	100 ns		23	50	1	
			0				12	\vdash	
Standby supply current	I _{CCS1}	V _{CE} ≥ V _{CC} - 0.2 V		0 to +40℃	· .		2	ДА	
Startdby supply current	İ		j	25℃	<u> </u>		1	1	
	I _{CCS2}	V _{CE} = V _{IH}			······································	0.4	2	mA	

Reference values at V_{CC} = 5 V, Ta = 25°C

Input/Output Capacitance at Ta = 25°C, f = 1 MHz

Parameter	Symbol	Conditions	min	typ	max	Unit
Input/output capacitance	c _{VO}	V _{I/O} = 0 V			8	pF
Input capacitance	CIN	V _{IN} = 0 V		· ·	6	pF

Note: These parameters were obtained through sampling, and not full-lot measurement.

AC Electrical Characteristics at Ta = 0 to +70°C, V_{CC} = 5 V \pm 10 %

AC testing conditions

Input pulse voltage level : 0.8 V, 2.2 V

Input rise and fall time

5 ns

Input - output timing level : 1.5 V

Output load

1 TTL gate + C_L = 100 pF (85 ns/100 ns)

1 TTL gate + $C_L = 30 \text{ pF} (70 \text{ ns})$

(including scope and jig capacitance)

Read Cycle

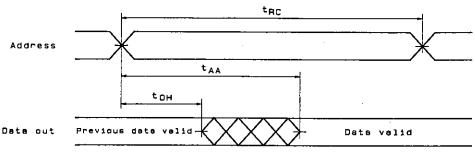
		LC36128ML							
Parameter Symbo	Symbol	-70		-85		-10		Unit	
		min	max	min	max	min	max	1	
Read cycle time	t _{RC}	70		85		100		ns	
Address access time	t _{AA}		70		85		100	ns	
CE access time	¹ CA		70		85		100	ns	
OE access time	t _{OA}		35		45		50	ns	
Output hold time	ЮН	20		20		20		ns	
CE output enable time	†COE	10		10		10		ns	
OE output enable time	¹oo€	5		5		5		ns	
CE output disable time	¹coo	0	30	0	30	0	30	ns	
OE output disable time	toop.	0	30	0	30	0	30	ns	

Write Cycle

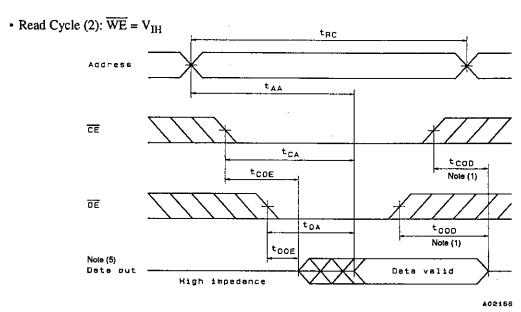
Parameter	Ĺ	LC36128ML						
	Symbol	-70		-85		-10		Unit
		min	max	min	max	min	max	1
Write cycle time	twc	70		85		100		ns
Address valid to end of write	[‡] AW	65		75		80		ns
Address setup time	las	0		0		0		ns
Write pulse width	t _{WP}	50		50		60		กร
CE setup time	lcw	65		75		80		ns
Write recovery time (WE)	twa	0		0		0		ns
Write recovery time (CE)	lwR1	0		0	·	0		ns
Data setup time	tos	30		30		35		ns
Data hold time	t _{DH}	0		0		0		ns
WE output enable time	twoE	10		10		10		ns
WE output disable time	I _{WOD}	0	25	0	25	0	25	ns

Timing Chart

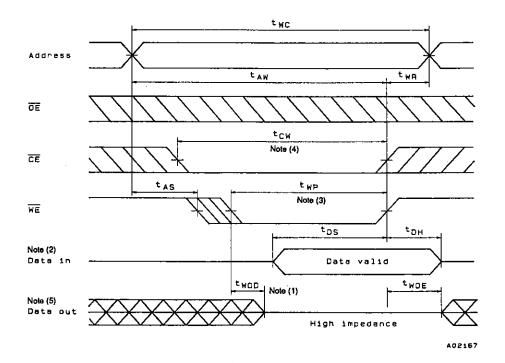
• Read Cycle (1): $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$



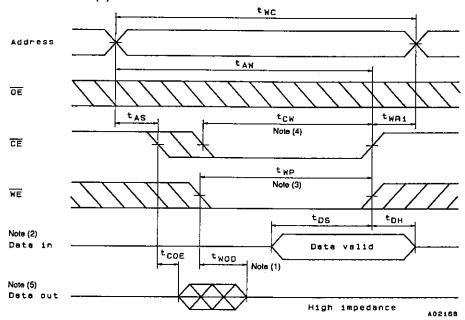
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• Write Cycle (1): WE Control Note (6)



• Write Cycle (2): CE Control Note (6)



Notes: (1) t_{COD}, t_{OOD}, and t_{WOD} are defined as the time at which the outputs becomes the high impedance state and are not referred to output voltage levels.

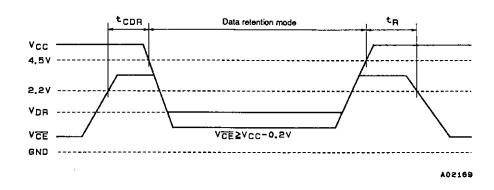
- (2) An external antiphase signal must not be applied when D_{OUT} is in the output state.
- (3) t_{WP} is the time interval that \overline{CE} and \overline{WE} are low-level and is defined as the interval from the falling of \overline{WE} to the rising of \overline{CE} or \overline{WE} , whichever is earlier.
- (4) t_{CW} is the time interval that \overline{CE} and \overline{WE} are low-level and is defined as the time from the falling of \overline{CE} to the rising of \overline{CE} or \overline{WE} , whichever is earlier.
- (5) D_{OUT} goes to the high-impedance state when either \overline{OE} is high-level, \overline{CE} is high-level, or \overline{WE} is low-level.
- (6) When \overline{OE} is high-level during the write cycle, D_{OUT} goes to the high-impedance state.

Data Retention Characteristics at Ta = 0 to +70°C

Parameter	Symbol	Conditions	min	typ	max	Unit	
Data retention supply voltage	V _{DR}	V _{CE} ≥ V _{CC} - 0.2 V	2.0	•	5.5	٧	
Data retention supply current			0 to +70°C			5	<u> </u>
	CCDR1	V _{CC} = 3.0 V, V _{CE} ≥ 2.8 V	0 to +40°C			1	μΑ
			25°C			0.4	1
	I _{CCDR2}	V _{CC} = 2.0 to 5.5 V, V _{CE} ≥ V _{CC} - 0			12	μΑ	
CE setup time	†CDR	-		0			ns
CE hold time	t _A	ļ ————————————————————————————————————		t _{RC} *			ns

^{*} t_{RC} = Read Cycle time

Data Retention Waveform



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