LG Display



# SPECIFICATION
# FOR
# APPROVAL

( ) **Preliminary Specification**

(●) **Final Specification**

| Title | 37.0” WUXGA TFT LCD |
|---|---|

| BUYER | General |
|---|---|
| LCM MODEL | LC370WUD-SBA1 |
| SET MODEL | |

| SUPPLIER | LG Display Co., Ltd. |
|---|---|
| *MODEL | LC370WUH |
| SUFFIX | SBA1(RoHS Verified) |

*When you obtain standard approval,
please use the above model name without suffix

| APPROVED BY | SIGNATURE DATE |
|---|---|
| / | |
| / | |
| / | |

Please return 1 copy for your confirmation with your signature and comments.

| APPROVED BY | SIGNATURE DATE |
|---|---|
| H.S.SONG /Team Leader | |
| **REVIEWED BY** | |
| H.I. JANG / Project Leader | |
| **PREPARED BY** | |
| J.H. Lee/ Engineer | |

**TV Product Development Dept.**
**LG Display Co., Ltd**

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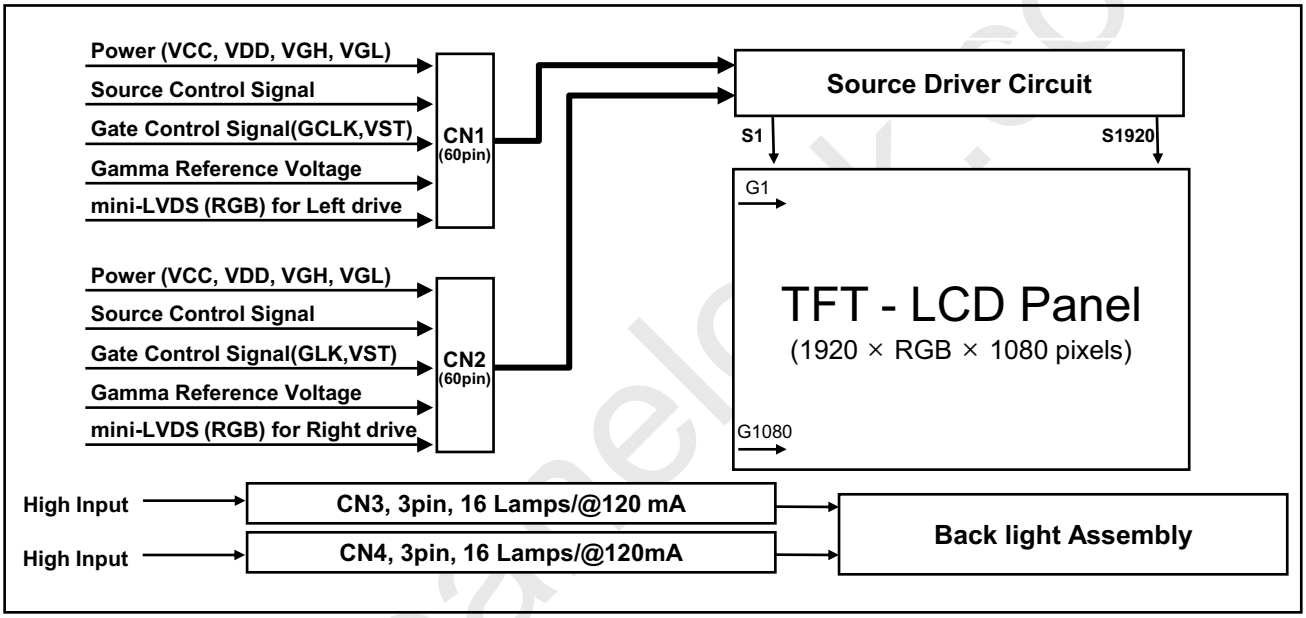
## RECORD OF REVISIONS

| Revision No. | Revision Date | Page | Description |
|---|---|---|---|
| 1.0 | Feb.02.27,2009 | - | Final specification. |

## 1. General Description

The LC370WUH is a Color Active Matrix Liquid Crystal Display with an integral External Electrode Fluorescent Lamp(EEFL) backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive display type which is operating in the normally black mode. It has a 37 inch diagonally measured active display area with WUXGA resolution (1080 vertical by 1920 horizontal pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arrayed in vertical stripes. Gray scale or the luminance of the sub-pixel color is determined with a 10-bit gray scale signal for each dot. Therefore, it can present a palette of more than 1.06Bilion (FRC) colors.
It is intended to support LCD TV, PCTV where high brightness, super wide viewing angle, high color gamut, high color depth and fast response time are important.




## General Features

| | |
|---|---|
| Active Screen Size | 37 inches(940.091mm) diagonal |
| Outline Dimension | 877(H) x 516.8 (V) x 36.4 mm(D) (Typ.) |
| Pixel Pitch | 0.42675 mm x 0.42675 mm |
| Pixel Format | 1920 horiz. by 1080 vert. Pixels, RGB stripe arrangement |
| Color Depth | System output : 8Bit → LCM output : 8Bit , 16.7M color |
| | System output : 10Bit(D) → LCM output : 10Bit , 1.06B color |
| Drive IC Data Interface | Source D-IC : 8-bit mini-LVDS, and control signals TTL<br>Gate D-IC : GIP(Gate D-IC In Panel) |
| Luminance, White | 500 cd/m$^2$ (Center 1point ,Typ.) |
| Viewing Angle (CR>10) | Viewing angle free ( R/L 178 (Typ.), U/D 178 (Typ.)) |
| Power Consumption | Total 133.88W (Typ.) (Logic=8.88W, Back Light=125W with inverter,Control PCB) |
| Weight | 7,400g (Typ.) |
| Display Mode | Transmissive mode, Normally black |
| Surface Treatment | Hard coating(3H), Anti-glare treatment of the front polarizer (Haze 10%) |

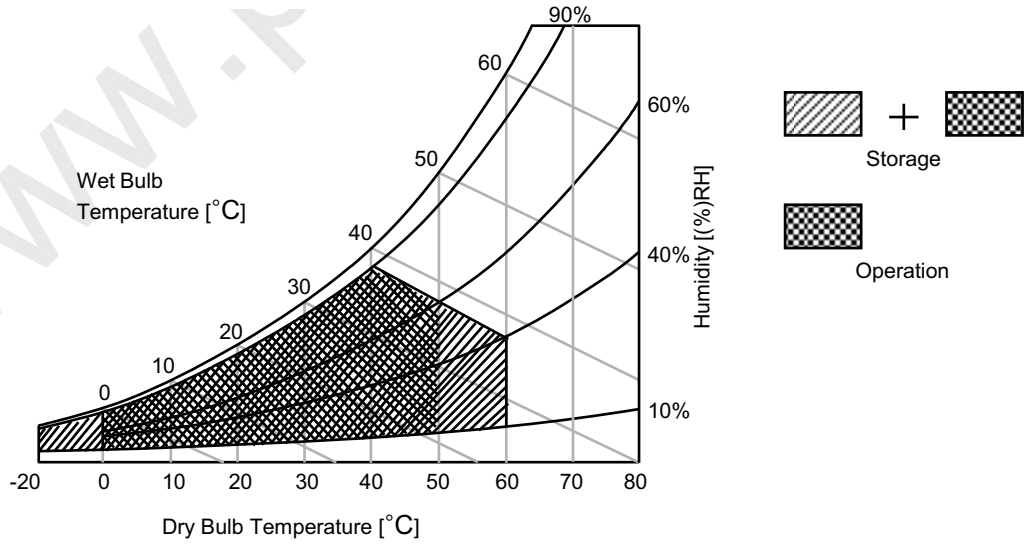
## 2. Absolute Maximum Ratings

The following items are maximum values which, if exceeded, may cause faulty operation or damage to the LCD module.

**Table 1. ABSOLUTE MAXIMUM RATINGS**

| Parameter | | Symbol | Value | | Unit | Remark |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Logic Power Voltage | | VCC | -0.5 | +4.0 | VDC | at 25 ± 2 °C |
| Source D-IC Analog Voltage | | VDD | -0.5 | +20.0 | VDC | |
| Gamma Ref. Voltage (Upper) | | VGMH | ½VDD-0.5 | VDD+0.5 | VDC | |
| Gamma Ref. Voltage (Low) | | VGML | -0.5 | ½ VDD+0.5 | VDC | |
| Gate High Voltage | | VGH | -0.3 | +40.0 | VDC | |
| Gate Low Voltage | | VGL | -14.0 | +0.3 | VDC | |
| Gate drive voltage difference | | VGH-VGL | -0.3 | +38.0 | VDC | |
| B/L Input voltage | Operating Voltage (one side) | VOP | 700 | 1100 | V[ RMS] | |
| Operating Temperature | | TOP | 0 | +50 | °C | Note 1,2 |
| Storage Temperature | | TST | -20 | +60 | °C | |
| Operating Ambient Humidity | | HOP | 10 | 90 | %RH | |
| Storage Humidity | | HST | 10 | 90 | %RH | |

Note : 1. Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be Max 39 °C. and no condensation of water.
2. Gravity mura can be guaranteed below 40℃condition.



## 3. Electrical Specifications

### 3-1. Electrical Characteristics

It requires two power inputs. One is employed to power for the LCD circuit. The other Is used for the EEFL backlight circuit.

**Table 2. ELECTRICAL CHARACTERISTICS**

| Parameter | Symbol | Condition | MIN | TYP | MAX | Units | Note |
|---|---|---|---|---|---|---|---|
| Logic Power Voltage | VCC | - | 3.0 | 3.3 | 3.6 | V | |
| Logic High Level Input Voltage | $V_{IH}$ | | 2.3 | | VCC | V | |
| Logic Low Level Input Voltage | $V_{IL}$ | | 0 | | 0.8 | V | |
| Source D-IC Analog Voltage | VDD | - | - | 16.3 | - | V | |
| Gamma Reference Voltage | $V_{GMH}$ | $V_{GMA}$ (GMA1 ~ GMA9) | ½*VDD | | VDD-0.2 | V | |
| | $V_{GML}$ | $V_{GMA}$ (GMA10 ~ GMA18) | 0.2 | | ½*VDD | V | |
| Common Voltage | Vcom | - | 6.11 | 6.86 | 8.14 | V | |
| Clock frequency | CLK | 3.0V≤VCC ≤3.6V | 250 | | 315 | MHz | |
| mini-LVDS input Voltage (Center) | $V_{IB}$ | Clock and Data | 0.7 + (VID/4) | | (VCC-1.2) − VID /4 | V | |
| mini-LVDS input Voltage Distortion(Center) | $\triangle V_{IB}$ | | - | - | 0.7 | V | 5,6 |
| mini-LVDS differential Voltage range | $V_{ID}$ | | 0.35 | | 1.3 | V(p-p) | 5.6 |
| mini-LVDS differential Voltage range Dip | $\triangle V_{ID}$ | | 0.1 | | 1.3 | V | |
| Gate High Voltage | VGH | - | 24.8 | 25.3 | 25.8 | VDC | Fig1 |
| Gate Low Voltage | VGL | - | -7.1 | -7.5 | -7.9 | VDC | Fig1 |
| VLCD Power Current | $I_{LCD}$ | - | | 740 | 962 | mA | 1,2 |
| VLCD Power Consumption | $PL_{CD}$ | - | | 8.88 | 11.54 | Watt | 1,2 |

Notes : 1. The specified current and power consumption are under the $V_{LCD}$=12V., 25 ± 2°C, $f_V$=120Hz condition whereas mosaic pattern(8 x 6) is displayed and $f_V$ is the frame frequency.
2. The above spec is general value in Base model.
3. All of the typical gate voltage require to control within 1% voltage level
4. Ripple voltage is recommended under 10% level
5. See Fig 2 for the more detailed definition.
6. The above spec will be guaranteed when measure specific point at Fig3.

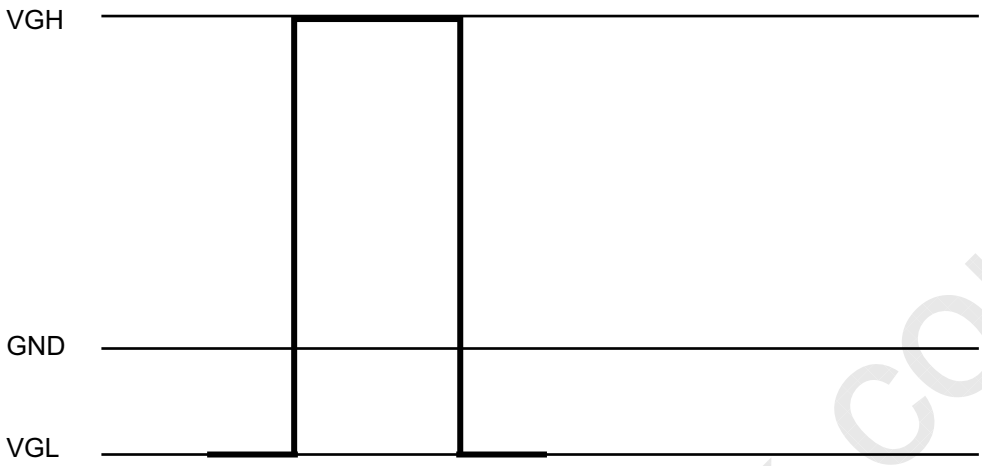



**FIG. 1 Gate Output Wave form**

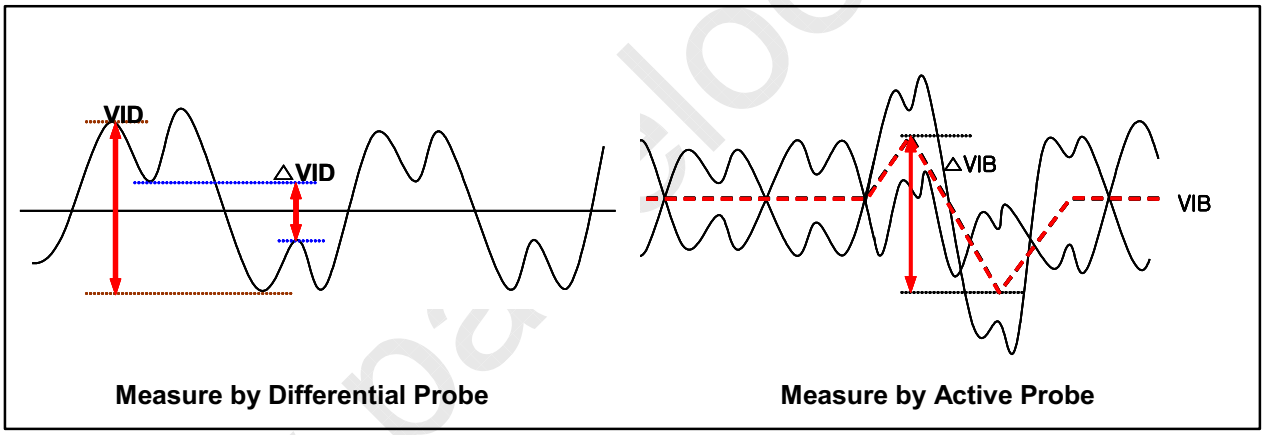



**FIG. 2 Description of VID,VIB, ΔVID, ΔVIB**

* Source PCB

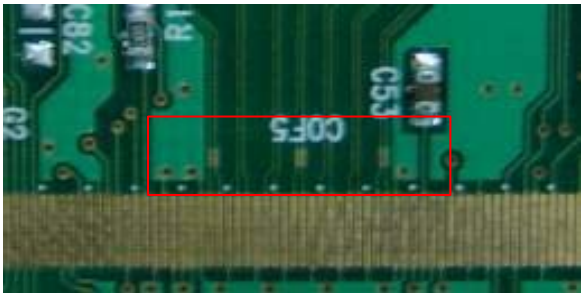


**FIG. 3 Measure point**

**Table 3. ELECTRICAL CHARACTERISTICS of Back Light Assembly & Lamp (Continue)**

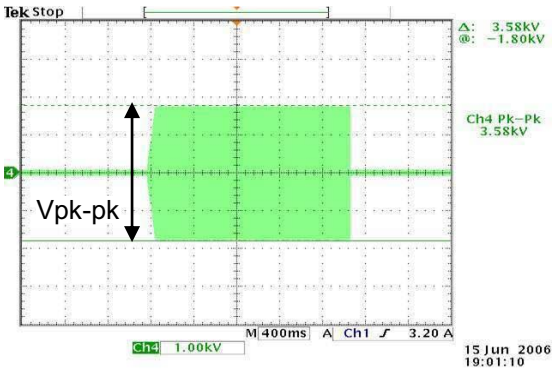
| Parameter | | Symbol | Values | | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **Backlight Assembly :** | | | | | | | |
| Operating Voltage (one side,fBL=45KHz, IBL= 120mArms)) | | VBL | 850 | 980 | 1150 | $V_{RMS}$ | 1, 2 |
| Operating Current (one side) | | IBL | 108 | 120 | 132 | $mA_{RMS}$ | 1 |
| Established Starting Voltage (one side) | 0℃ | VS | - | - | 1120 | $V_{RMS}$ | 1, 3 |
| | 25℃ | | - | - | 960 | | |
| Operating Frequency | | fBL | 43 | 45 | 47 | kHz | 4 |
| Striking Time | | S TIME | - | - | 1.5 | sec | 3 |
| Power Consumption | | PBL | | 125 | | Watt | 6 |
| Burst Dimming Duty | | { a/T } * 100 | 20 | | 100 | % | 9 |
| Burst Dimming Frequency | | 1/T | 95 | - | 182 | Hz | 9 |

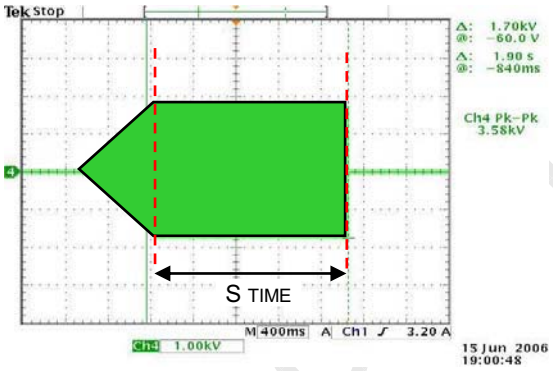
| Parameter | | Symbol | Values | | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **Lamp : APPENDIX-V** | | | | | | | |
| Lamp Voltage (one side) | | VLAMP | 802 | 1082 | 1130 | $V_{RMS}$ | 2 |
| Lamp Current (one side) | | ILAMP | 3.5 | 7.5 | 8.5 | $mA_{RMS}$ | |
| Discharge Stabilization Time | | TS | - | - | 3 | Min | 5 |
| Lamp Frequency | | f LAMP | 40 | 45 | 80 | KHz | |
| Lamp Temperature | | TLAMP | | | 130 | °C | |
| Established Starting Voltage (one side) | 0℃ | VS | | | 1120 | $V_{RMS}$ | 3 |
| | 25℃ | VS | | | 960 | | |
| Life Time | | | 50,000 | | | Hrs | 7 |

Notes : The design of the inverter must have specifications for the lamp in LCD Assembly.
The electrical characteristics of inverter are based on High-High Driving type.
The performance of the lamps in LCM, for example life time or brightness, is extremely influenced by the characteristics of the DC-AC inverter. So, all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.
When you design or order the inverter, please make sure unwanted lighting caused by the mismatch of the lamp and the inverter (no lighting, flicker, etc) has never been occurred. When you confirm it, the LCD– Assembly should be operated in the same condition as installed in your instrument.

※ Do not attach a conductive tape to lamp connecting wire.
If you attach conductive tape to the lamp wire, not only luminance level can be lower than typical one but also inverter operate abnormally on account of leakage current which is generated between lamp wire and conductive tape.

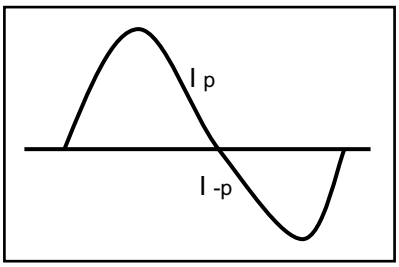
1. Specified values are defined for a Backlight Assembly.( IBL : 16 lamp, 7.5mA/Lamp)
2. Operating voltage is measured at 25 ± 2°C(after 2hr.aging). The variance range for operating voltage is ± 10%.
3. The established starting voltage [ VS ] should be applied to the lamps for more than Striking time (S TIME) for start-up. Inverter open voltage must be more than established starting voltage. Otherwise, the lamps may not be turned on. The used lamp current is typical value.




Vs = (Vpk-pk) / [ 2*root(2)]

4. Lamp frequency may produce interference with horizontal synchronous frequency. As a result, the may cause beat on the display. Therefore, lamp frequency shall be away as much as possible from the horizontal synchronous frequency and its harmonics range in order to prevent interference.
5. The brightness of the lamp after lighted for 5minutes is defined as 100%.
   $T_S$ is the time required for the brightness of the center of the lamp to be not less than 95% at typical current.
   The screen of LCD module may be partially dark by the time the brightness of lamp is stable after turn on.
6. Maximum level of power consumption is measured at initial turn on.
   Typical level of power consumption is measured after 2hrs aging at 25 ± 2°C.
7. The life time is determined as the time at which brightness of the lamp is 50% compared to that of initial value at the typical lamp current on condition of continuous operating at 25 ± 2°C, based on duty 100%.
8. The output of the inverter must have symmetrical(negative and positive) voltage and current waveform (Unsymmetrical ratio is less than 10%). Please do not use the inverter which has not only unsymmetrical voltage and current but also spike wave.
   Requirements for a system inverter design, which is intended to achieve better display performance, power efficiency and more reliable lamp characteristics.
   It can help increase the lamp lifetime and reduce leakage current.
   a. The asymmetry rate of the inverter waveform should be less than 10%.
   b. The distortion rate of the waveform should be within √2 ±10%.
   * Inverter output waveform had better be more similar to ideal sine wave.



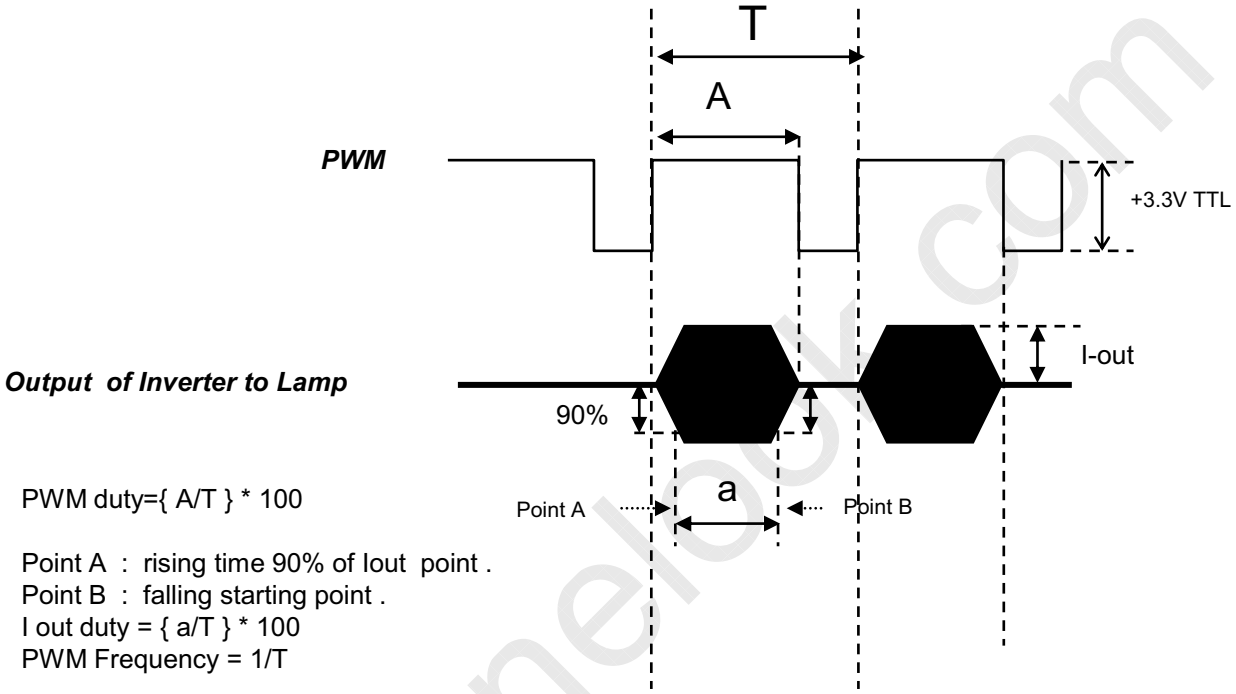

* Asymmetry rate:

$| I_p - I_{-p} | / I_{op} \times 100\%$

* Distortion rate

$I_p$ (or $I_{-p}$) / $I_{op}$

9. The reference method of burst dimming duty ratio.
   It is recommended to use synchronous V-sync frequency to prevent waterfall
   (Vsync x 1 =Burst Frequency)
   Though PWM frequency is over 182Hz(max252Hz), function of lamp is not affected




PWM duty={ A/T } * 100

Point A : rising time 90% of Iout point .
Point B : falling starting point .
I out duty = { a/T } * 100
PWM Frequency = 1/T

※ We recommend not to be much different between PWM duty and Iout duty .
※ Dimming current output rising and falling time may produce humming and inverter trans' sound noise.
※ Burst dimming duty should be 100% for more than 1second after turn on.
※ Equipment
   Oscilloscope :TDS3054B(Tektronix)
   Current Probe : P6022 AC (Tektronix)
   High Voltage Probe: P5100(Tektronix)

10. The Cable between the backlight connector and its inverter power supply should be connected directly with a minimized length. The longer cable between the backlight and the inverter may cause the lower luminance of lamp and may require more higher starting voltage ( Vs ).

11. The operating current must be measured as near as backlight assembly input.

12. The operating current unbalance between left and right must be under 10% of Typical current
   |Left(Master) current – Right(Slave) Current| 〈 10% of typical current

## 3-2. Interface Connections

This LCD module employs two 60pin connector of interface connection, Each 60 pin connectors are used for the module electronics and two 3-pin Balance PCB connectors are used for the integral backlight system.

### 3-2-1. LCD Module

- LCD Connector : AF7601-N2G11 (Manufactured by P-TWO or Equivalent)

**Table 4-1. Source PCB CONNECTOR(CN1) PIN CONFIGURATION**

| No | Symbol | Description | No | Symbol | Description |
|---|---|---|---|---|---|
| 1 | GND | Ground | 31 | NC | No Connection |
| 2 | LTD_OUT | LTD OUTPUT | 32 | LV2B | Left Mini LVDS Receiver Signal(2−) |
| 3 | GND | Ground | 33 | LV2A | Left Mini LVDS Receiver Signal(2+) |
| 4 | VDD | DRIVER POWER SUPPLY VOLTAGE | 34 | LV1B | Left Mini LVDS Receiver Signal(1−) |
| 5 | VDD | DRIVER POWER SUPPLY VOLTAGE | 35 | LV1A | Left Mini LVDS Receiver Signal(1+) |
| 6 | GND | Ground | 36 | LV0B | Left Mini LVDS Receiver Signal(0−) |
| 7 | VCC | LOGIC POWER SUPPLY VOLTAGE | 37 | LV0A | Left Mini LVDS Receiver Signal(0+) |
| 8 | VCC | LOGIC POWER SUPPLY VOLTAGE | 38 | GND | Ground |
| 9 | GND | Ground | 39 | SOE | LEFT SOURE OUTPUT ENABLE |
| 10 | V18_B | GAMMA VOLTAGE 18 | 40 | POL | POLARITY OUTPUT SIGNAL |
| 11 | V16 | GAMMA VOLTAGE 16 | 41 | V9 | GAMMA VOLTAGE 9 |
| 12 | V15 | GAMMA VOLTAGE 15 | 42 | V7 | GAMMA VOLTAGE 7 |
| 13 | V13 | GAMMA VOLTAGE 13 | 43 | V6 | GAMMA VOLTAGE 6 |
| 14 | V12 | GAMMA VOLTAGE 12 | 44 | V4 | GAMMA VOLTAGE 4 |
| 15 | V10 | GAMMA VOLTAGE 10 | 45 | V3 | GAMMA VOLTAGE 3 |
| 16 | GSP | GATE START PULSE | 46 | V1_B | GAMMA VOLTAGE 1 |
| 17 | H_CONV | HORIZONTAL 2 INVERSION SIGNAL | 47 | VCOMIN | LEFT VCOM OUTPUT |
| 18 | CHRSHR | CHRAGE SHARING CONTROL SIGNAL | 48 | VCOMFB | LEFT VCOM FEEDBACK |
| 19 | GND | Ground | 49 | VST | GATE START PULSE FOR GIP |
| 20 | NC | No Connection | 50 | VSS (VGL) | GATE LOW VOLTAGE FOR GIP |
| 21 | NC | No Connection | 51 | VDD_EVEN | DISCHARGING VOLTAGE EVEN FOR GIP |
| 22 | LV6B | Left Mini LVDS Receiver Signal(6−) | 52 | VDD_ODD | DISCHARGING VOLTAGE ODD FOR GIP |
| 23 | LV6A | Left Mini LVDS Receiver Signal(6+) | 53 | VDD (VGH) | GATE HIGH VOLTAGE FOR GIP |
| 24 | LV5B | Left Mini LVDS Receiver Signal(5−) | 54 | CLK6 | GATE SHIFT CLOCK6 FOR GIP |
| 25 | LV5A | Left Mini LVDS Receiver Signal(5+) | 55 | CLK5 | GATE SHIFT CLOCK5 FOR GIP |
| 26 | LV4B | Left Mini LVDS Receiver Signal(4−) | 56 | CLK4 | GATE SHIFT CLOCK4 FOR GIP |
| 27 | LV4A | Left Mini LVDS Receiver Signal(4+) | 57 | CLK3 | GATE SHIFT CLOCK3 FOR GIP |
| 28 | CLKB | Left Mini LVDS Receiver Clock Signal(−) | 58 | CLK2 | GATE SHIFT CLOCK2 FOR GIP |
| 29 | CLKA | Left Mini LVDS Receiver Clock Signal(+) | 59 | CLK1 | GATE SHIFT CLOCK1 FOR GIP |
| 30 | NC | No Connection | 60 | GND | Ground |

**Table 4-2. Source PCB CONNECTOR (CN2) PIN CONFIGURATION**

| No | Symbol | Description | No | Symbol | Description |
|---|---|---|---|---|---|
| 1 | GND | Ground | 31 | LV2A | Right Mini LVDS Receiver Signal(2+) |
| 2 | LTD_OUT | LTD OUTPUT | 32 | LV1B | Right Mini LVDS Receiver Signal(1−) |
| 3 | GND | Ground | 33 | LV1A | Right Mini LVDS Receiver Signal(1+) |
| 4 | VDD | DRIVER POWER SUPPLY VOLTAGE | 34 | LV0B | Right Mini LVDS Receiver Signal(0−) |
| 5 | VDD | DRIVER POWER SUPPLY VOLTAGE | 35 | LV0A | Right Mini LVDS Receiver Signal(0+) |
| 6 | GND | Ground | 36 | GND | Ground |
| 7 | VCC | LOGIC POWER SUPPLY VOLTAGE | 37 | SOE | RIGHT SOURE OUTPUT ENABLE |
| 8 | VCC | LOGIC POWER SUPPLY VOLTAGE | 38 | POL | POLARITY OUTPUT SIGNAL |
| 9 | GND | Ground | 39 | GSP | GATE START PULSE |
| 10 | V18_B | GAMMA VOLTAGE 18 | 40 | H_CONV | HORIZONTAL 2 INVERSION SIGNAL |
| 11 | V16 | GAMMA VOLTAGE 16 | 41 | V9 | GAMMA VOLTAGE 9 |
| 12 | V15 | GAMMA VOLTAGE 15 | 42 | V7 | GAMMA VOLTAGE 7 |
| 13 | V13 | GAMMA VOLTAGE 13 | 43 | V6 | GAMMA VOLTAGE 6 |
| 14 | V12 | GAMMA VOLTAGE 12 | 44 | V4 | GAMMA VOLTAGE 4 |
| 15 | V10 | GAMMA VOLTAGE 10 | 45 | V3 | GAMMA VOLTAGE 3 |
| 16 | CHRSHR | CHRAGE SHARING CONTROL SIGNAL | 46 | V1_B | GAMMA VOLTAGE 1 |
| 17 | GND | Ground | 47 | GND | Ground |
| 18 | NC | No Connection | 48 | CLK6 | GATE SHIFT CLOCK6 FOR GIP |
| 19 | NC | No Connection | 49 | CLK5 | GATE SHIFT CLOCK5 FOR GIP |
| 20 | LV6B | Right Mini LVDS Receiver Signal(6−) | 50 | CLK4 | GATE SHIFT CLOCK4 FOR GIP |
| 21 | LV6A | Right Mini LVDS Receiver Signal(6+) | 51 | CLK3 | GATE SHIFT CLOCK3 FOR GIP |
| 22 | LV5B | Right Mini LVDS Receiver Signal(5−) | 52 | CLK2 | GATE SHIFT CLOCK2 FOR GIP |
| 23 | LV5A | Right Mini LVDS Receiver Signal(5+) | 53 | CLK1 | GATE SHIFT CLOCK1 FOR GIP |
| 24 | LV4B | Right Mini LVDS Receiver Signal(4−) | 54 | VDD (VGH) | GATE HIGH VOLTAGE FOR GIP |
| 25 | LV4A | Right Mini LVDS Receiver Signal(4+) | 55 | VDD_ODD | DISCHARGING VOLTAGE ODD FOR GIP |
| 26 | CLKB | Right Mini LVDS Receiver Clock(−) | 56 | VDD_EVEN | DISCHARGING VOLTAGE EVEN FOR GIP |
| 27 | CLKA | Right Mini LVDS Receiver Clock (+) | 57 | VSS (VGL) | GATE LOW VOLTAGE FOR GIP |
| 28 | NC | No Connection | 58 | VST | GATE START PULSE FOR GIP |
| 29 | NC | No Connection | 59 | VCOMIN | RIGHT VCOM OUTPUT |
| 30 | LV2B | Right Mini LVDS Receiver Signal(2−) | 60 | GND | Ground |


Top view of LCM

Rear view of LCM

[CN1]
- Part/No. : AF7601-N2G11(P-TWO)

[CN2]
- Part/No. : AF7601-N2G11(P-TWO)

### 3-2-2. Backlight Inverter

**[ Master ]**

**1) Balance Connector**

: 65002WS-03 (manufactured by YEONHO)or equivalent

**2) Mating Connector**

: 65002HS-03 (manufactured by YEONHO) or equivalent.

**[ Slave ]**

**1) Balance Connector**

: 65002WS-03 (manufactured by YEONHO)or equivalent

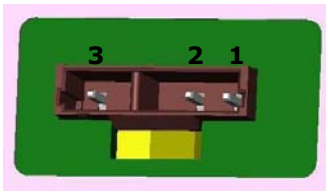
**2) Mating Connector**

: 65002HS-03 (manufactured by YEONHO) or equivalent.

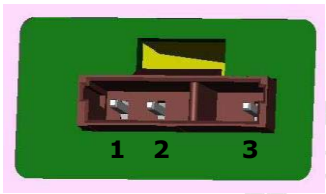
**Table 5. BACKLIGHT CONNECTOR PIN CONFIGURATION(CN2,CN3)**

| No | Symbol | Master | Slave | Note |
|---|---|---|---|---|
| 1 | **H_Input** | High_Input | High_Input | |
| 2 | **H_Input** | High_Input | High_Input | |
| 3 | **FB** | NC | NC | |

## ◆ Rear view of LCM




Master




Slave

## 3-3. Signal Timing Specifications

**TABLE 6. Timing Requirements**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Data clock frequency (Note 1) | t1 | 3.0<VCC<3.6 | | | 330 | MHz |
| Clock pulse low period (Note 1) | t2 | 3.0<VCC<3.6 | 1.35 | - | - | ns |
| Clock pulse high period (Note 1) | t3 | 3.0<VCC<3.6 | 1.35 | - | - | ns |
| Data setup time (Note 1) | t4 | 3.0<VCC<3.6 | 0.65 | - | - | ns |
| Data hold time (Note 1) | t5 | | 0.65 | - | - | ns |
| Reset low to SOE rising time | t6 | | 0 | - | - | ns |
| SOE to Reset input time | t7 | | 150 | - | - | ns |
| Receiver off to SOE timing | t8 | | 9 | - | - | DCLK |
| POL signal SOE setup time | t9 | | -5 | - | - | ns |
| POL signal SOE hold time | t10 | | 6 | - | - | ns |
| Reset High Period | t11 | | 0ver 3 CLK | - | - | - |
| SOE signal GSP setup time | t12 | | 6'CLK | - | - | - |

**Notes :**

1. Setup time and hold time couldn't be satisfied at the same time

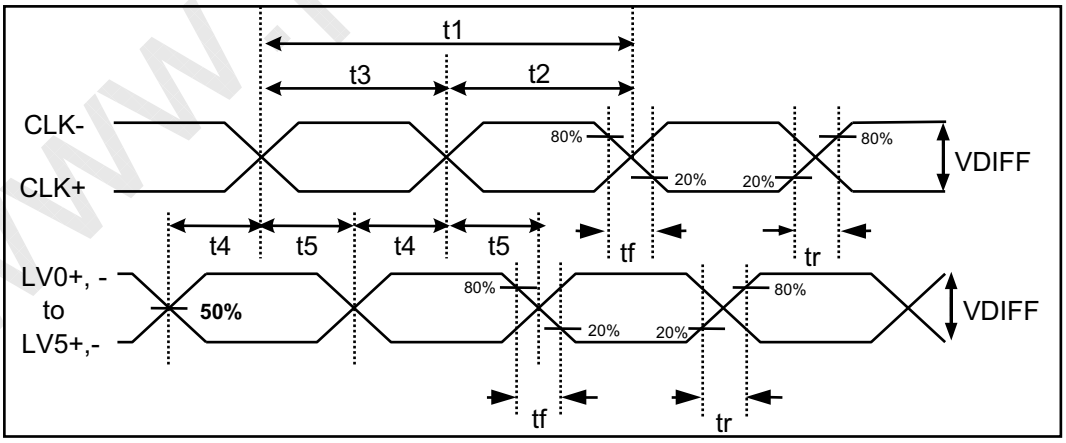
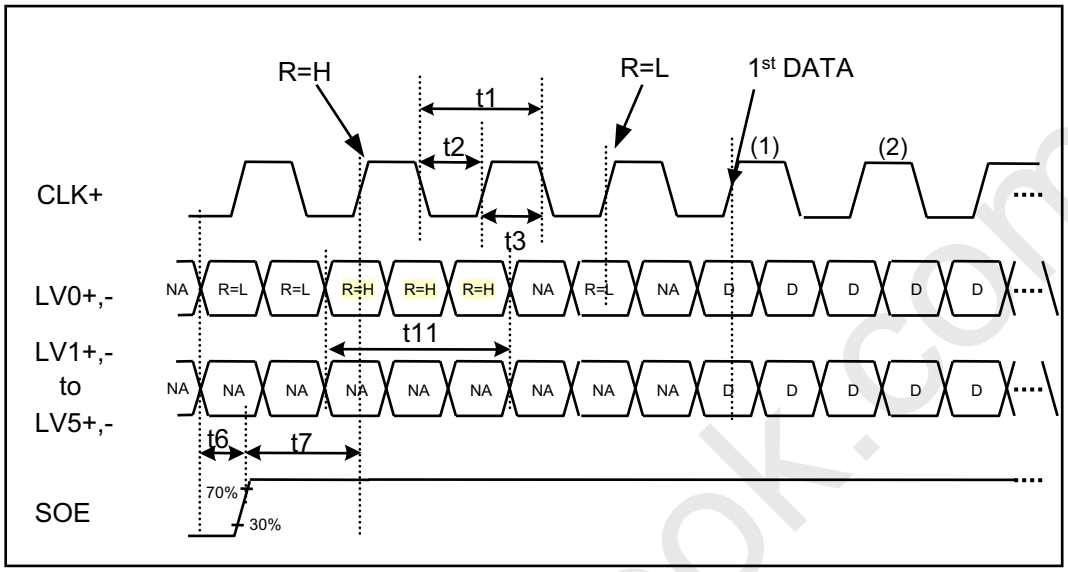



**FIG 2. Clock Timing Waveform**



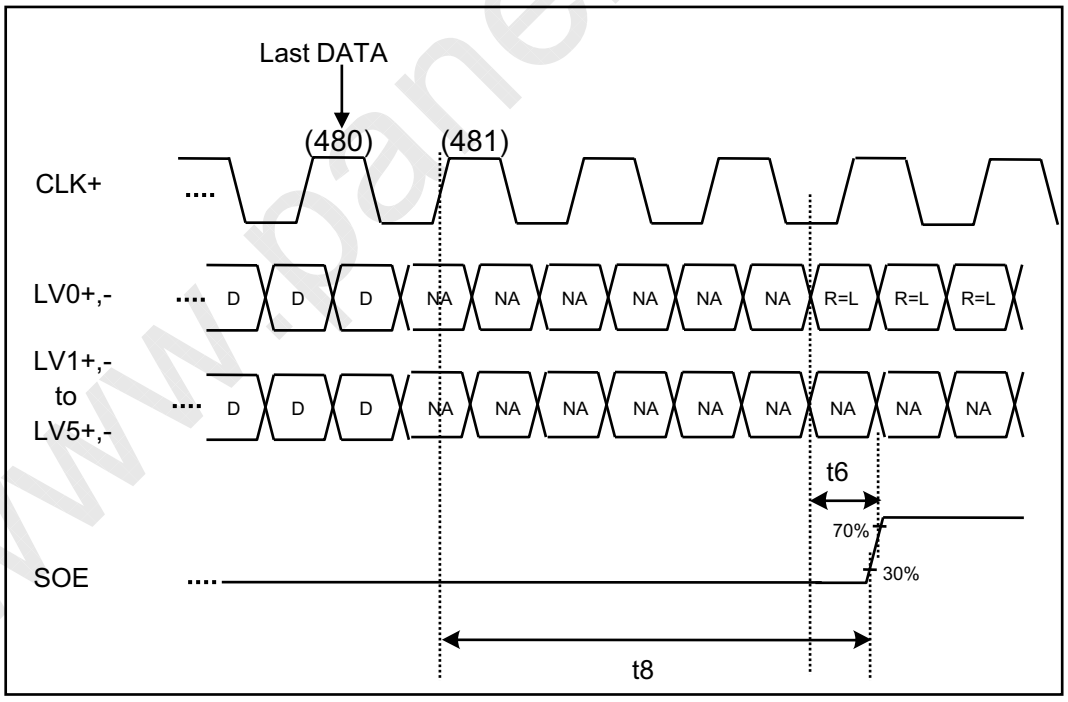




**FIG 3. Clock and SOE Timing Waveform**

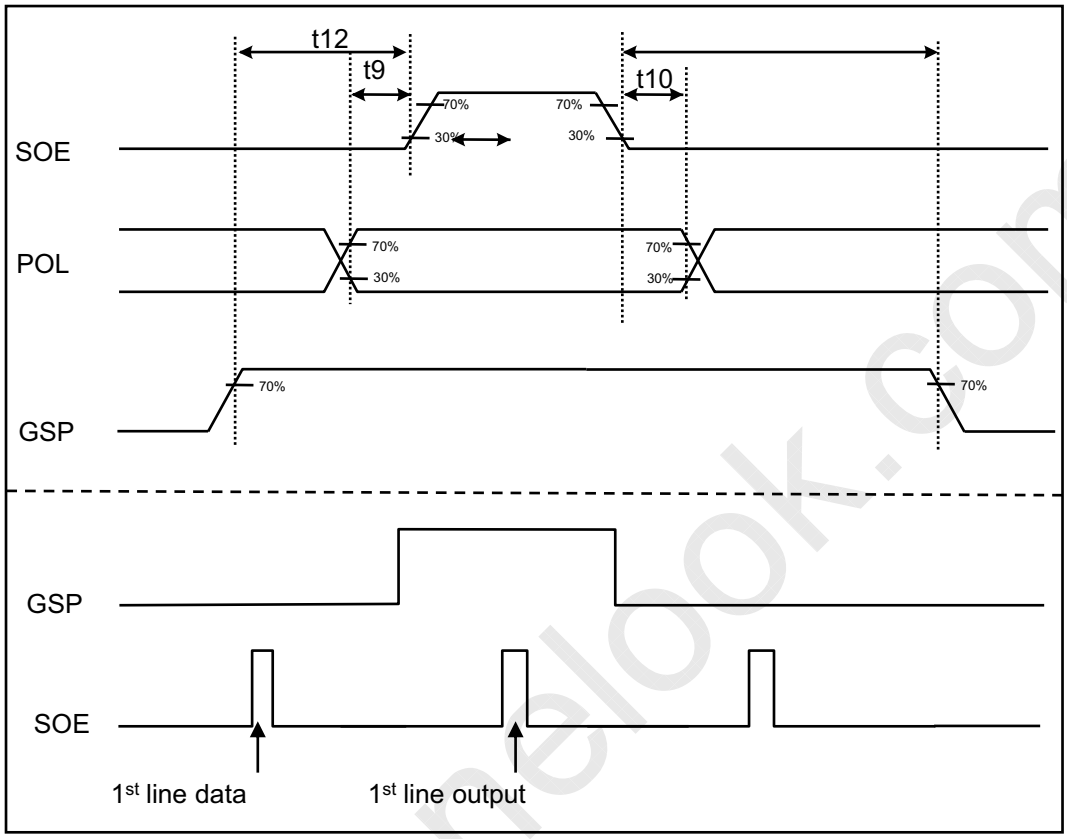
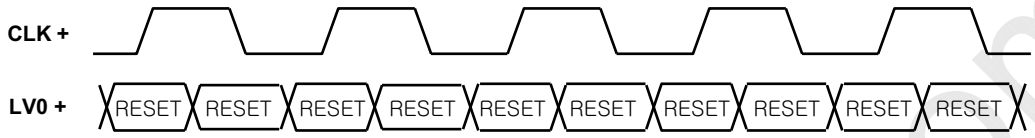



**FIG 4. POL, GSP and SOE Timing Waveform**

## 3-4. Data Mapping and Timing

Display data and control signal (RESET) are input to LV0 to LV7. Data mapping is changed in response to mode, and the mode is changed by mode.

### 3-4-1. Control signal input mode




### 3-4-2. Display data input mode

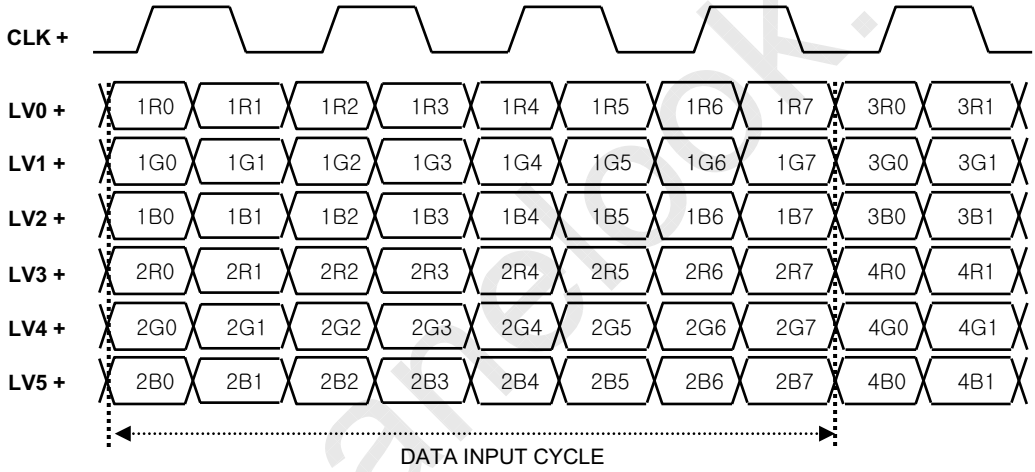



**Fig. 5 Left mini-LVDS Data**

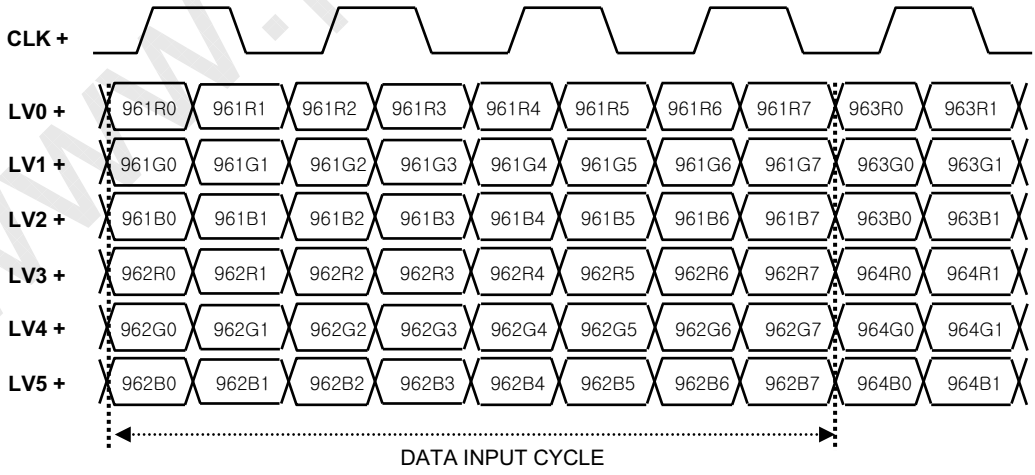



**Fig. 6 Right mini-LVDS Data**

### 3-5. Panel Pixel Structure

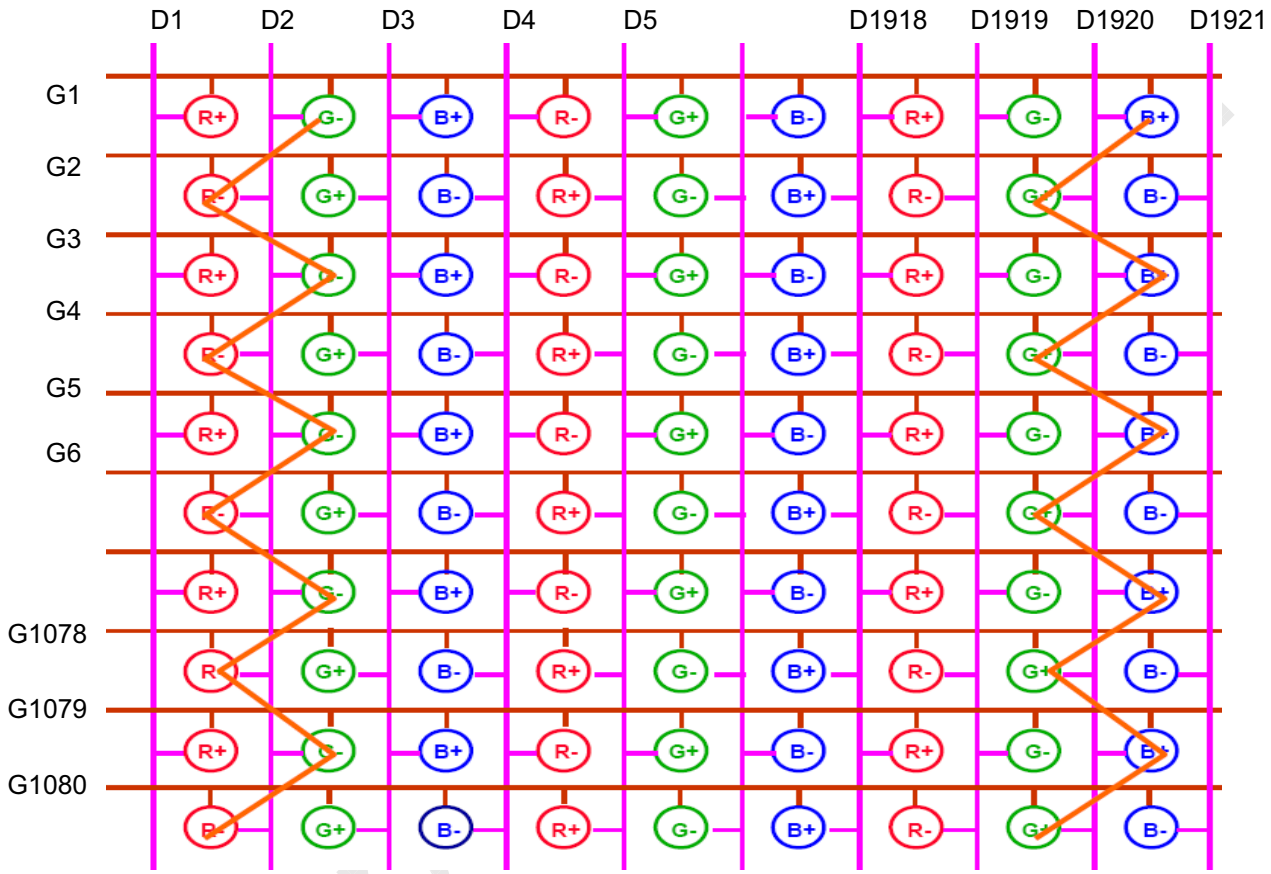



**FIG. 7 Panel Pixel Structure**

## 3-6. Power Sequence

### 3-6-1. LCD Driving circuit

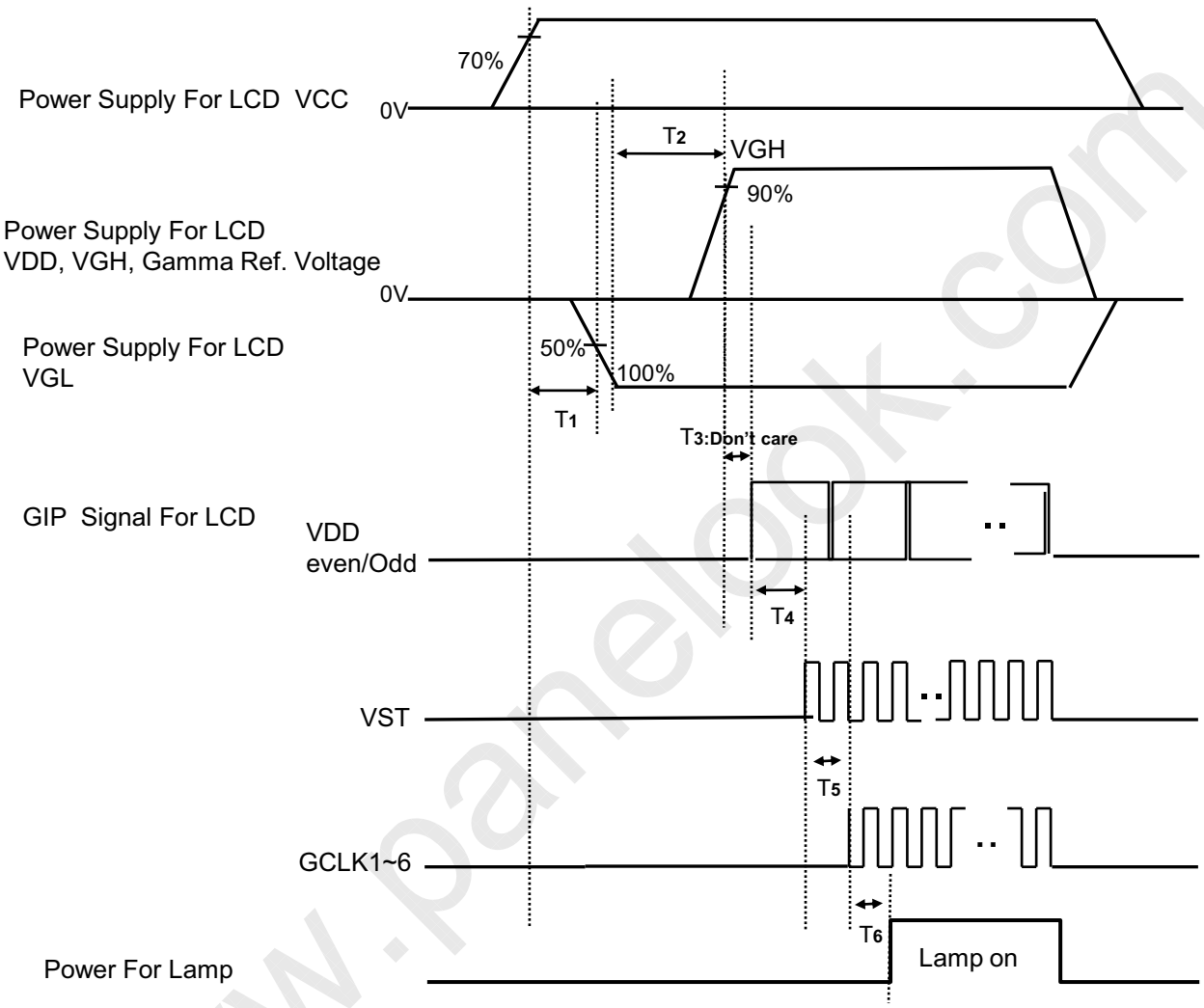



**Table 7. POWER SEQUENCE** Ta= 25±2°C, fv=120Hz, Dclk=297MHz, fH=135kHz

| Parameter | Value | | | Unit | Notes |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| T1 | 0.5 | | - | ms | |
| T2 | 0.5 | | - | ms | |
| T4 | 20(2~3frame) | | - | ms | 4 |
| T5 | 20(2~3frame) | | - | ms | |
| T6 | 20 | | - | ms | |

Note : 1. The Source D-IC power on sequence must be VCC, logic input, VDD & Gamma ref. voltage.
2. GIP specific timing setting is refer to Appendix I
3. VDD Odd signal should be started “High” status.

## 4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable in a dark environment at 25±2°C. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and θ equal to 0 °.
FIG. 8 shows additional information concerning the measurement equipment and method.

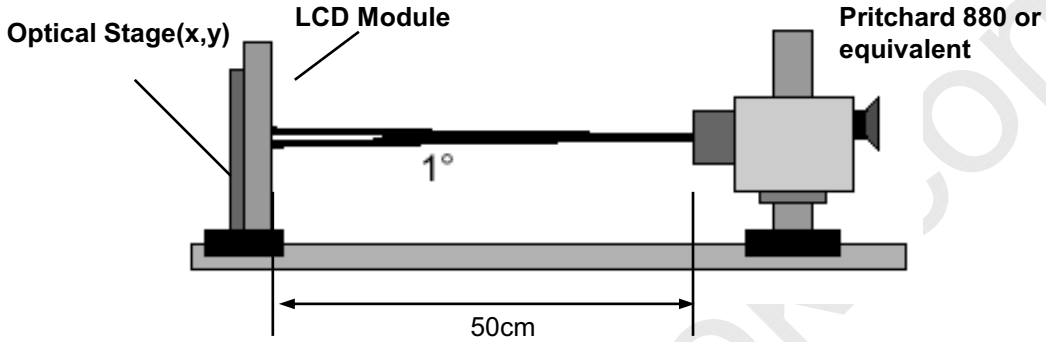



**FIG. 8 Optical Characteristic Measurement Equipment and Method**

Ta= 25±2°C, $V_{LCD}$=12.0V, fv=120Hz, Dclk=297MHz
IBL=120mA

**Table 7. OPTICAL CHARACTERISTICS**

| Parameter | | Symbol | Value | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Contrast Ratio | | CR | 1000 | 1400 | - | | 1 |
| Surface Luminance, white | | $L_{WH}$ | 400 | 500 | | cd/m$^2$ | 2 |
| Uniformity | | | | | | | |
| Response Time | Rising | Tr | - | 8 | 12 | ms | 4 |
| | Falling | Tf | - | 8 | 12 | ms | 4 |
| Color Coordinates [CIE1931] | RED | Rx | Typ -0.03 | 0.639 | Typ +0.03 | | |
| | | Ry | | 0.334 | | | |
| | GREEN | Gx | | 0.289 | | | |
| | | Gy | | 0.606 | | | |
| | BLUE | Bx | | 0.145 | | | |
| | | By | | 0.065 | | | |
| | WHITE | Wx | | 0.279 | | | |
| | | Wy | | 0.292 | | | |
| Viewing Angle (CR>10) | | | | | | | |
| | x axis, right(ϕ=0°) | θr | 89 | - | - | degree | 5 |
| | x axis, left (ϕ=180°) | θl | 89 | - | - | | |
| | y axis, up (ϕ=90°) | θu | 89 | - | - | | |
| | y axis, down (ϕ=270°) | θd | 89 | - | - | | |
| Gray Scale | | | | - | | | 6 |

Notes :1Contrast Ratio(CR) is defined mathematically as :

$$CR = \frac{\text{Surface Luminance at all white pixels}}{\text{Surface Luminance at all black pixels}}$$

It is measured at center 1-point.

2. Surface luminance is determined after the unit has been 'ON' and 1Hour after lighting the backlight in a dark environment at 25±2°C. Surface luminance is the luminance value at center 1-point across the LCD surface 50cm from the surface with all pixels displaying white. For more information see the FIG. 9.

3. The variation in surface luminance , δ WHITE is defined as :
   δ WHITE(5P) = Maximum($L_{on1}$,$L_{on2}$, $L_{on3}$, $L_{on4}$, $L_{on5}$) / Minimum($L_{on1}$,$L_{on2}$, $L_{on3}$, $L_{on4}$, $L_{on5}$)
   Where $L_{on1}$ to $L_{on5}$ are the luminance with all pixels displaying white at 5 locations .
   For more information, see the FIG. 9.

4. Response time is the time required for the display to transit from G(255) to G(0) (Rise Time, $Tr_R$) and from G(0) to G(255) (Decay Time, $Tr_D$).
   ※ Photo Detector : RD-80S / Field : 2 °

5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD module surface. For more information, see the FIG. 11.

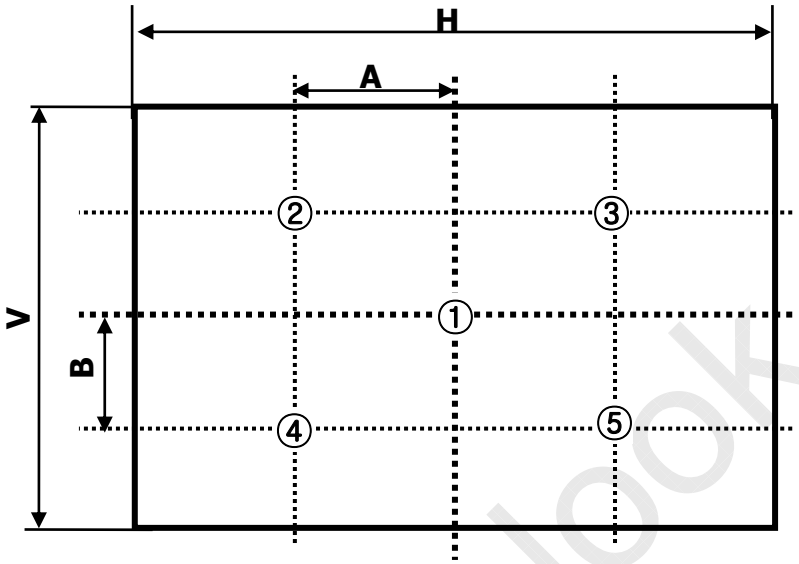
6. Gray scale specification
   Gamma Value is approximately 2.2. For more information, see the Table 8.

**Table 8. GRAY SCALE SPECIFICATION**

| Gray Level | Luminance [%] (Typ.) |
|---|---|
| L0 | 0.07 |
| L63 | 0.24 |
| L127 | 1.04 |
| L191 | 2.49 |
| L255 | 4.68 |
| L319 | 7.66 |
| L383 | 11.5 |
| L447 | 16.1 |
| L511 | 21.6 |
| L575 | 28.1 |
| L639 | 35.4 |
| L703 | 43.7 |
| L767 | 53.0 |
| L831 | 63.2 |
| L895 | 74.5 |
| L959 | 86.7 |
| L1023 | 100 |

| | Gray Level | Gamma Ref. |
|---|---|---|
| Positive Voltage | L0 | Gamma9 |
| | L1 | - |
| | L31 | Gamma7 |
| | L63 | Gamma6 |
| | L127 | - |
| | L191 | Gamma4 |
| | L223 | Gamma3 |
| | L255 | Gamma1 |
| Negative Voltage | L255 | Gamma18 |
| | L223 | Gamma16 |
| | L191 | Gamma15 |
| | L127 | - |
| | L63 | Gamma13 |
| | L31 | Gamma12 |
| | L1 | - |
| | L0 | Gamma10 |

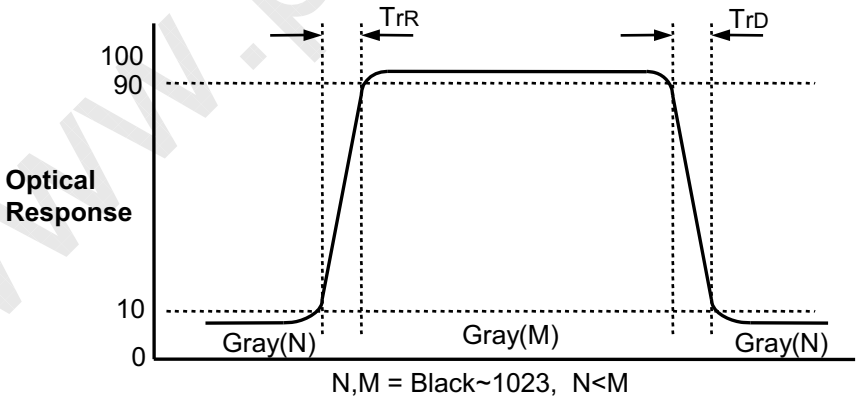
Measuring point for surface luminance & measuring point for luminance variation.




A : H / 4 mm
B : V / 4 mm
@ H,V : Active Area

**FIG. 9 5 Points for Luminance Measure**

Response time is defined as the following figure and shall be measured by switching the input signal for "Gray(N)" and "Gray(M)".




N,M = Black~1023, N<M

**FIG.10 Response Time(G to G)**

Dimension of viewing angle range

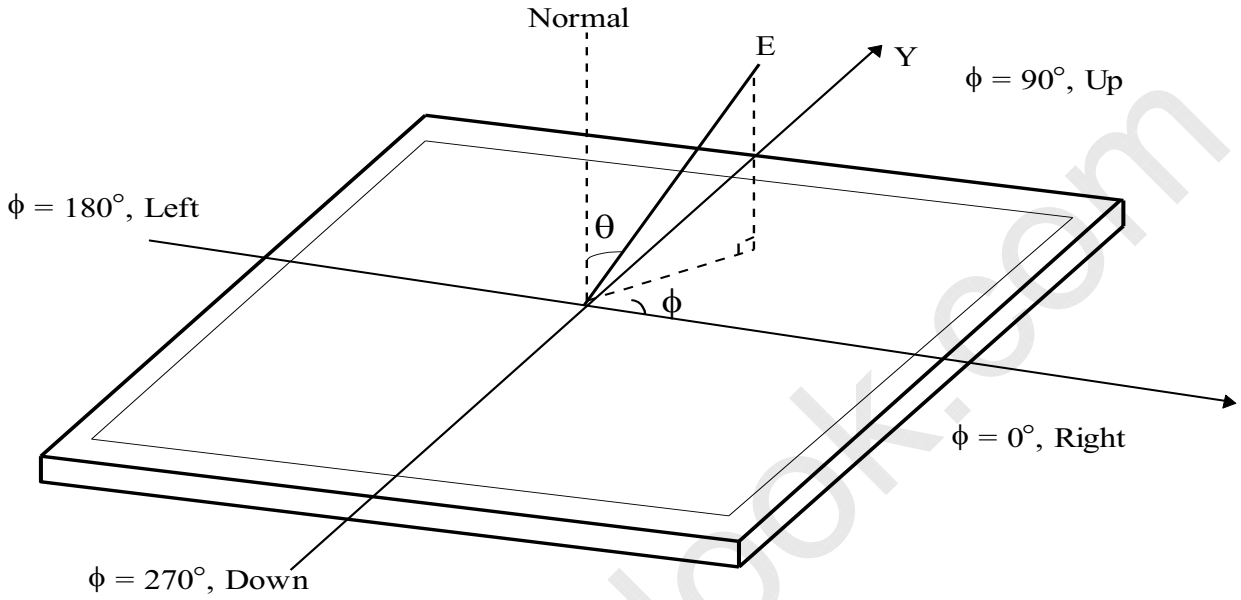



**FIG. 11 Viewing angle**

## 5. Mechanical Characteristics

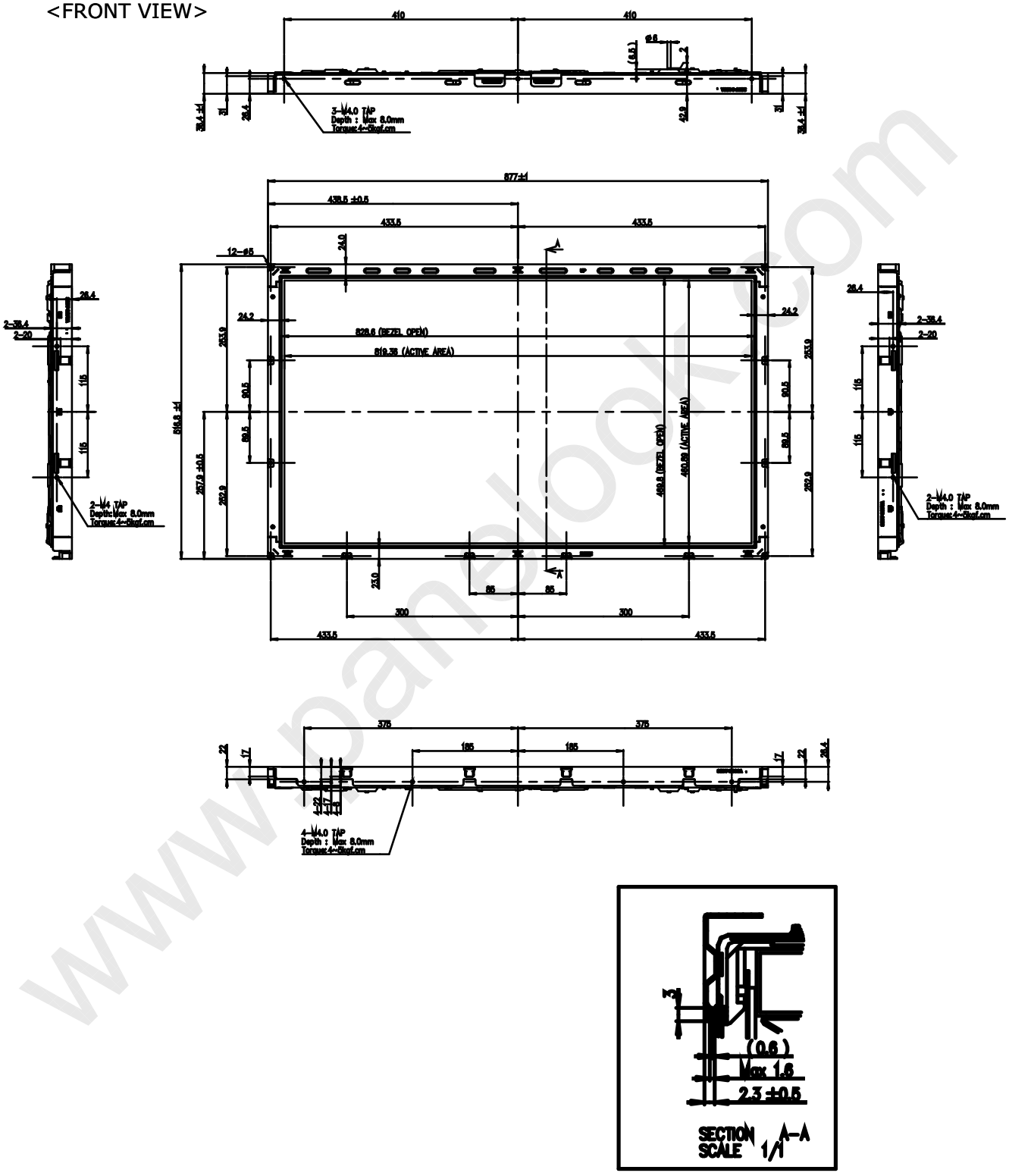
Table 9 provides general mechanical characteristics.

**Table 9. MECHANICAL CHARACTERISTICS**

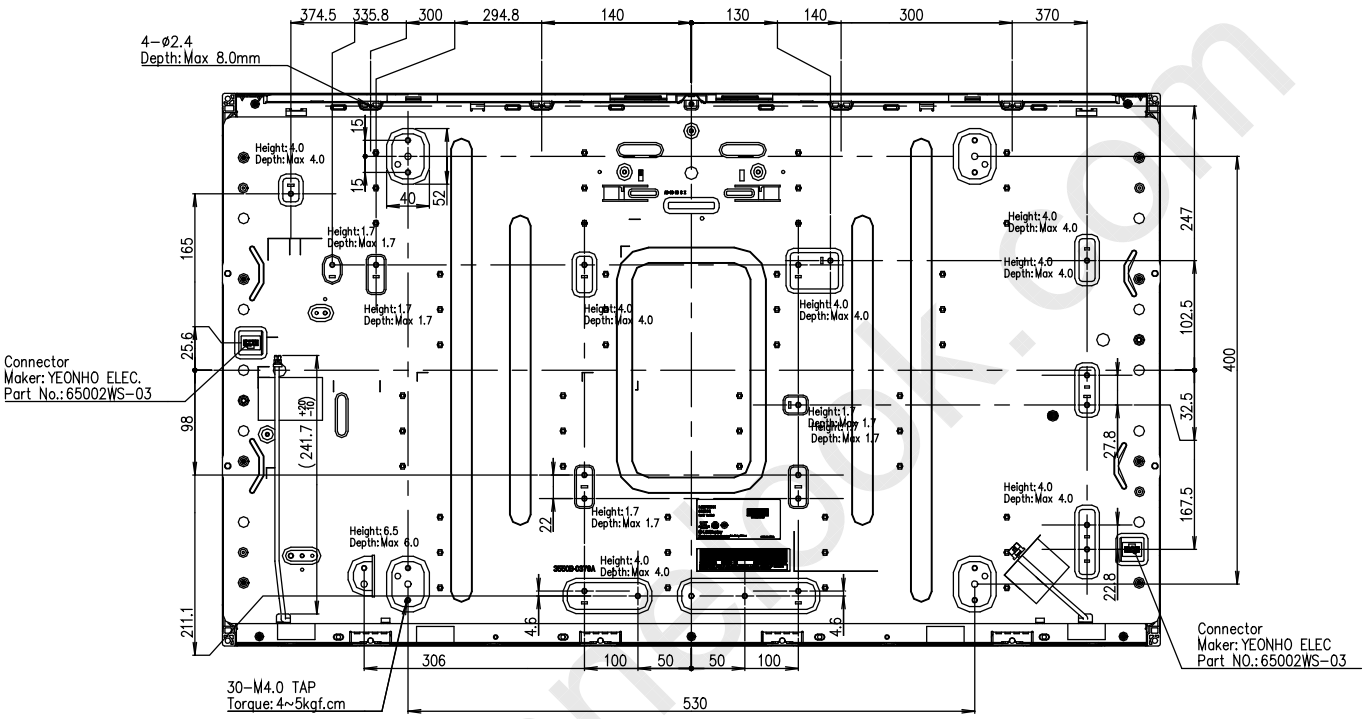
| Item | Value | |
|---|---|---|
| Outline Dimension | Horizontal | **877.0 mm** |
| | Vertical | **516.8 mm** |
| | Depth | **36.4 mm** |
| Bezel Area | Horizontal | **828.6 mm** |
| | Vertical | **469.8 mm** |
| Active Display Area | Horizontal | **819.36 mm** |
| | Vertical | **460.89 mm** |
| Weight | **7,400(Typ.)/ 7,700(Max)** | |

Note : Please refer to a mechanical drawing in terms of tolerance at the next page.

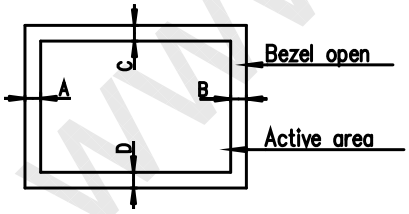
<FRONT VIEW>



<REAR VIEW>




NOTES
1. Unspecified tolerances are to be ±0.5mm.
2. This drawing is only preliminary data and can be changed without notice.
3. Tilt and partial disposition tolerance of display area is as following.
   (1) X-Direction : IA-BI ≤ 1.5mm
   (2) Y-Direction : IC-DI ≤ 1.5mm




4. IPB Wire Spec. : UL3239-HF VW-1, AWG#24(LS Cable) or compatible, Rating Voltage 6kV, UL File No. : E52853 or compatible
5. IPB Connector : UL94 V-0, BDEMR-02VS(JST) or compatible, UL File No. : E60389 or compatible
6. Shrink Tube : UL 94 V-1, NP-HF-Tube, AWG#6(N.PLASTECH) or compatible, UL File No. : E321606 or compatible

## 6. Reliability

**Table 10. ENVIRONMENT TEST CONDITION**

| No. | Test Item | Condition |
|---|---|---|
| 1 | High temperature storage test | Ta= 60°C 240h |
| 2 | Low temperature storage test | Ta= -20°C 240h |
| 3 | High temperature operation test | Ta= 50°C 50%RH 240h |
| 4 | Low temperature operation test | Ta= 0°C 240h |
| 5 | Vibration test<br>(non-operating) | Wave form : random<br>Vibration level : 1.0Grms<br>Bandwidth : 10-300Hz<br>Duration : X,Y,Z,<br>One time each direction per 10min |
| 6 | Shock test<br>(non-operating) | Shock level : 100Grms<br>Waveform : half sine wave, 2ms<br>Direction : ±X, ±Y, ±Z<br>One time each direction |
| 7 | Humidity condition Operation | Ta= 40 °C ,90%RH |
| 8 | Altitude operating<br>storage / shipment | 0 - 15,000 ft<br>0 - 40,000 ft |

Note : Before and after Reliability test, LCM should be operated with normal function.

## 7. International Standards

### 7-1. Safety

a) UL 60065, 7th Edition, dated June 30, 2003, Underwriters Laboratories, Inc., Standard for Audio, Video and Similar Electronic Apparatus.
b) CAN/CSA C22.2, No. 60065:03, Canadian Standards Association, Standard for Audio, Video and Similar Electronic Apparatus.
c) IEC60065:2001, 7th Edition CB-scheme and EN 60065:2002, Safety requirements for Audio, Video and Similar Electronic Apparatus..

### 7-2. Environment

a) RoHS, Directive 2002/95/EC of the European Parliament and of the council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment

# 8. Packing

## 8-1. Information of LCM Label

a) Lot Mark

| A | B | C | D | E | F | G | H | I | J | K | L | M |
|---|---|---|---|---|---|---|---|---|---|---|---|---|

A,B,C : SIZE(INCH)
E : MONTH

D : YEAR
F ~ M : SERIAL NO.

Note

1. YEAR

| Year | 2001 | 2002 | 2003 | 2004 | 2005 | 2006 | 2007 | 2008 | 2009 | 2010 |
|---|---|---|---|---|---|---|---|---|---|---|
| Mark | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 0 |

2. MONTH

| Month | Jan | Feb | Mar | Apr | May | Jun | Jul | Aug | Sep | Oct | Nov | Dec |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Mark | 1 | 2 | 4 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C |

b) Location of Lot Mark

Serial NO. is printed on the label. The label is attached to the backside of the LCD module.
This is subject to change without prior notice.

## 8-2. Packing Form

a) Package quantity in one box : 4 pcs

b) Box Size : 968mm X 366mm X 595mm

## 9. Precautions

Please pay attention to the followings when you use this TFT LCD module.

### 9-1. Mounting Precautions

(1) You must mount a module using specified mounting holes (Details refer to the drawings).
(2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
(4) You should adopt radiation structure to satisfy the temperature specification.
(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzine. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer. * There is no problem of Panel crack under 5kgf / φ10mm
(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(9) Do not open the case because inside circuits do not have sufficient strength.

### 9-2. Operating Precautions

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
V=±200mV(Over and under shoot voltage)
(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer
(4) Be careful for condensation at sudden temperature change.Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.
(7) Please do not give any mechanical and/or acoustical impact to LCM. Otherwise, LCM can't be operated its full characteristics perfectly.
(8) A screw which is fastened up the steels should be a machine screw.
(if not, it can causes conductive particles and deal LCM a fatal blow)
(9) Please do not set LCD on its edge.
(10) Partial darkness may happen during 3~5 minutes when LCM is operated initially in condition that luminance is under 40% at low temperature (under 5℃). This phenomenon which disappears naturally after 3~5 minutes is not a problem about reliability but LCD characteristic

## 9-3. Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

## 9-4. Precautions for Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

## 9-5. Storage

When storing modules as spares for a long time, the following precautions are necessary.

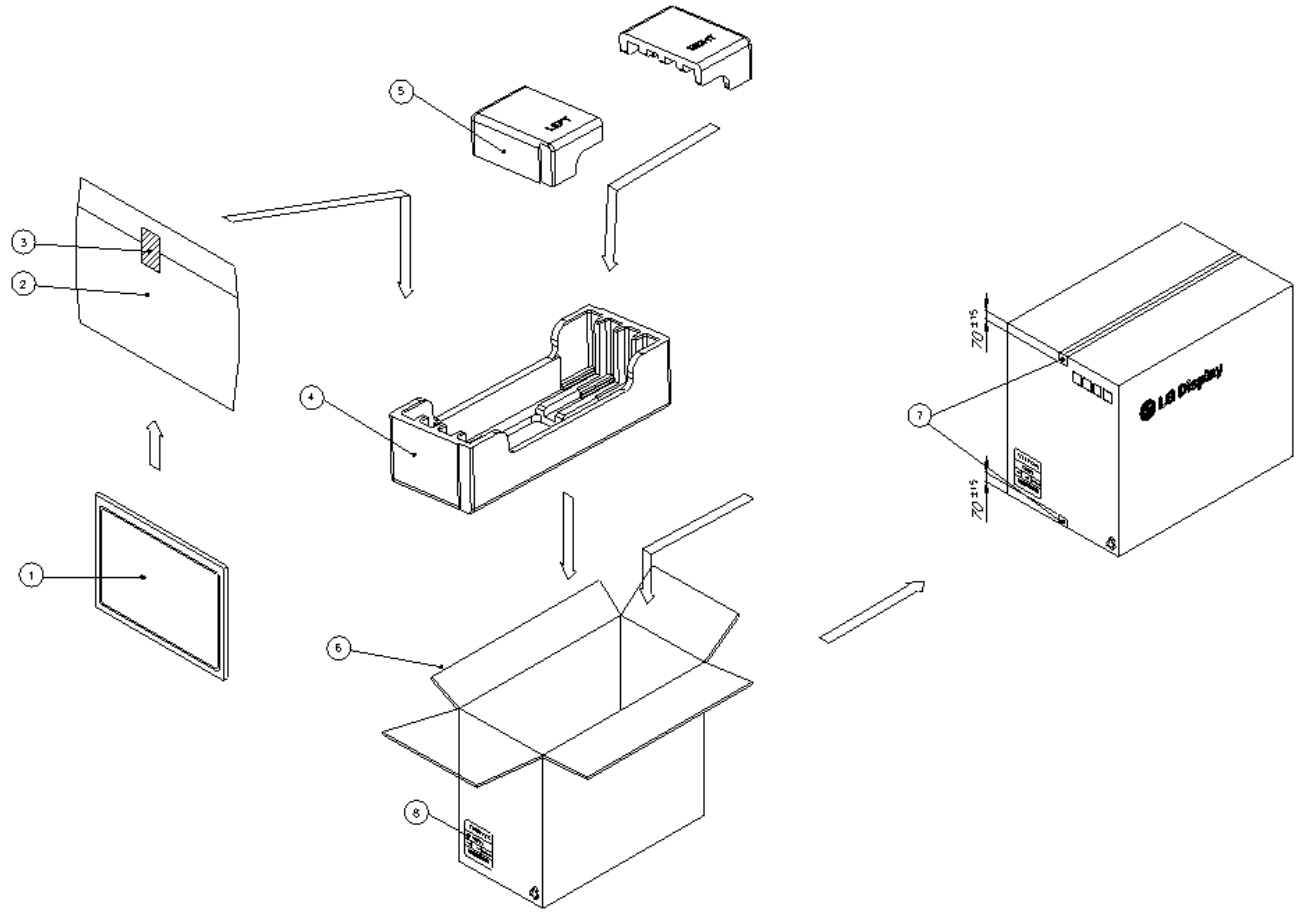
(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
(2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

## 9-6. Handling Precautions for Protection Film

(1) The protection film is attached to the bezel with a small masking tape.
When the protection film is peeled off, static electricity is generated between the film and polarizer.
This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
(2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.
(3) You can remove the glue easily. When the glue remains on the bezel surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

**# APPENDIX-I-1**

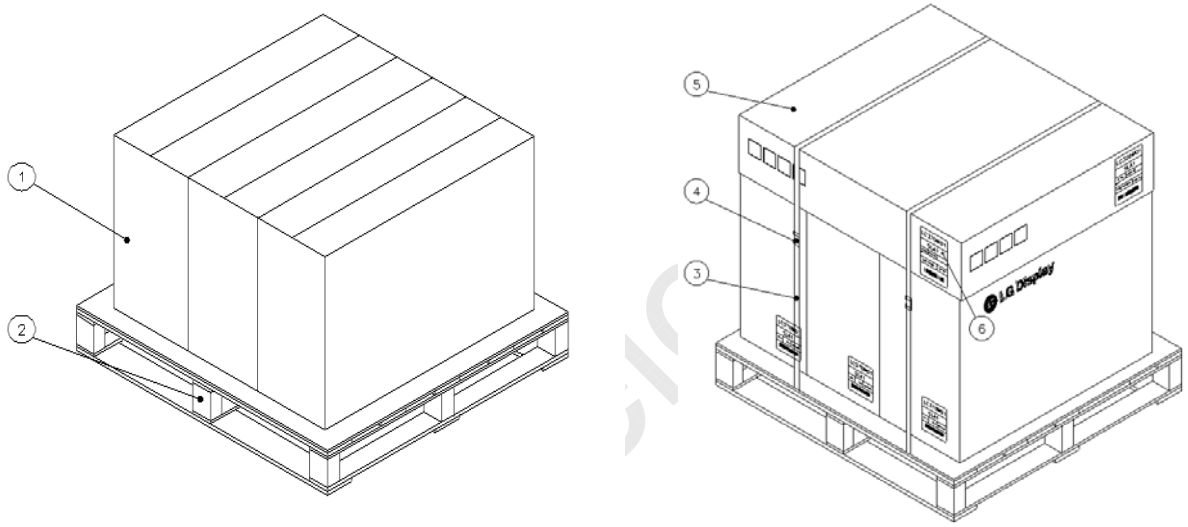
## ■ LC370WUH-SBA1 Packing Ass'y



| NO. | DESCRIPTION | MATERIAL |
|---|---|---|
| 1 | LCD MODULE | |
| 2 | BAG | AL |
| 3 | TAPE | MASKING 20MM X 50M |
| 4 | PACKING, BOTTOM | EPS |
| 5 | PACKING, TOP R_L | EPS |
| 6 | BOX | PAPER_DW3 |
| 7 | TAPE | OPP 70MMX300M |
| 8 | LABEL | YUPO PAPER 100X100 |

**# APPENDIX-I-2**

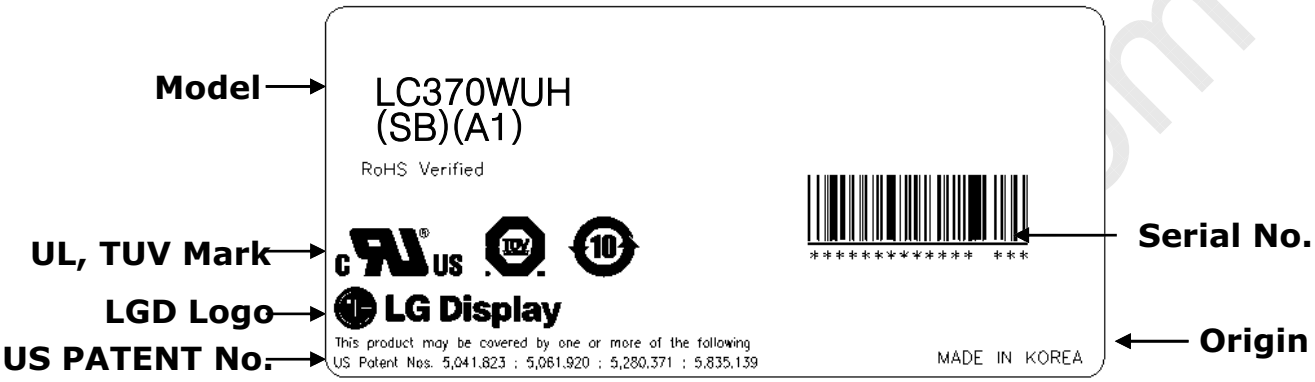
■ LC370WUH-SBA1 Pallet Ass'y




| NO. | DESCRIPTION | MATERIAL |
|---|---|---|
| 1 | PACKING ASS'Y | |
| 2 | PALLET | Plywood_1140X990X130 |
| 3 | BAND | PP |
| 4 | BAND, CLIP | CLIP 18MM |
| 5 | ANGLE, COVER | DW3 |
| 6 | LABEL | YUPO PAPER |

# APPENDIX- II

■ LCM Label



## # APPENDIX- III

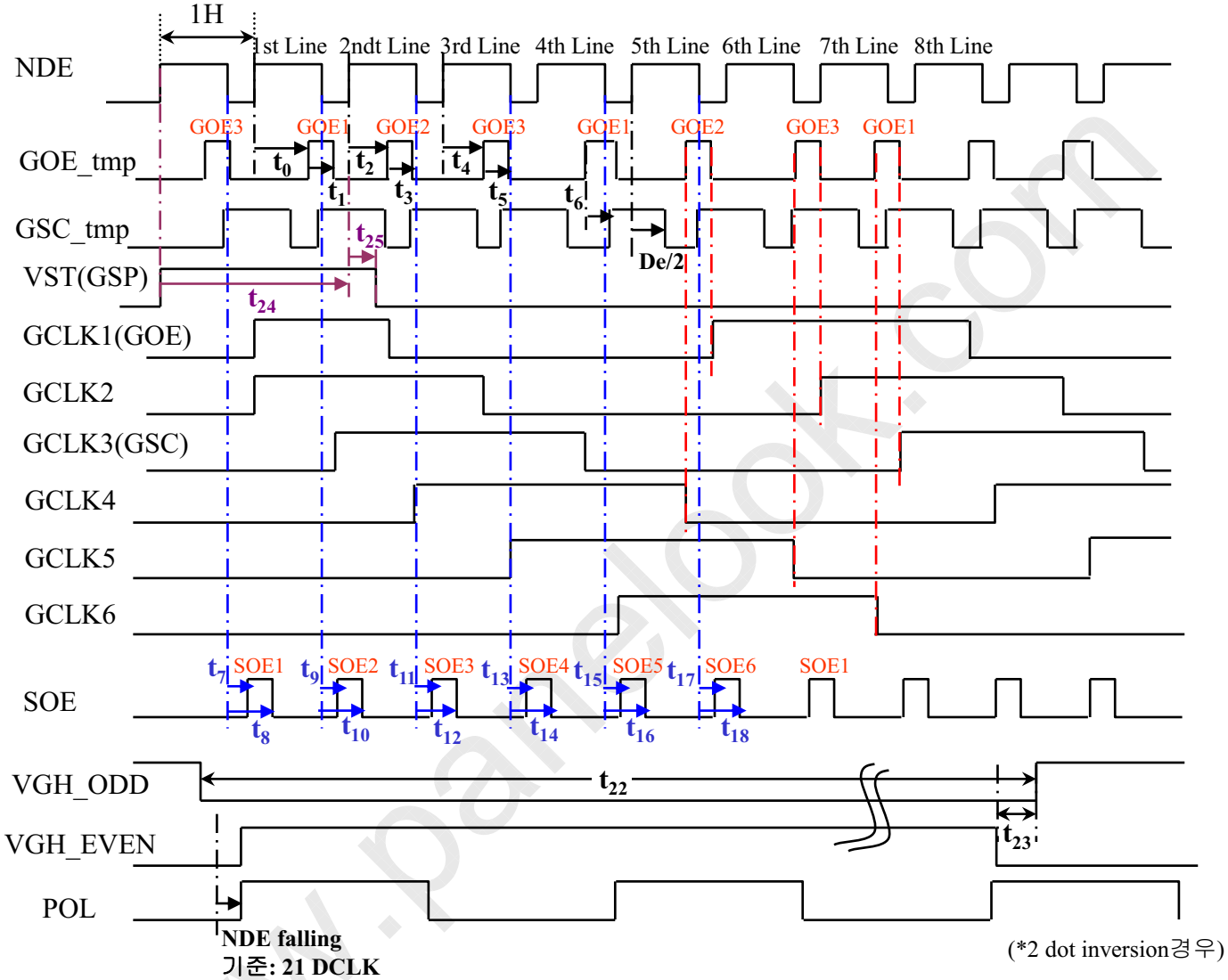
■ Box Label

| LC370WUH | | |
|---|---|---|
| SBA1 | | |
| 4 PCS | LOT/MM-DD | |
| MADE IN KOREA | | RoHS Verified |
| ********** *** | | |

■ Pallet Label

| LC370WUH | | |
|---|---|---|
| SBA1 | | |
| 12 PCS | LOT/MM-DD | |
| MADE IN KOREA | | RoHS Verified |
| ********** *** | | |

## # APPENDIX IV. Gate and Source Control Signal timing




(*2 dot inversion경우)

**Table11. Timing table**

Ta= 25±2°C, fv=120Hz, Dclk=297MHz, fH=135kHz

| Parameter | Value | | | Unit | Notes |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| t1,t3,t5 | - | 140 | - | $t_{CLK}$ | |
| t0,t2,t4 | - | 387 | - | $t_{CLK}$ | |
| t7,t9,t11 | - | 10 | - | $t_{CLK}$ | |
| t8,t10,t12 | - | 56 | - | $t_{CLK}$ | |
| t22 | - | 254 | - | frame | |
| t23 | - | 48 | - | $t_{CLK}$ | |

Note : 1. Typical value of table11 is LG Recommend timing that base model use.

## # APPENDIX- V

■ **Starting (Striking) Voltage measurement method.**

**Measure the high voltage point of Balance Ass'y after removing all lamp.**

a) CCFL Cap balance Structure

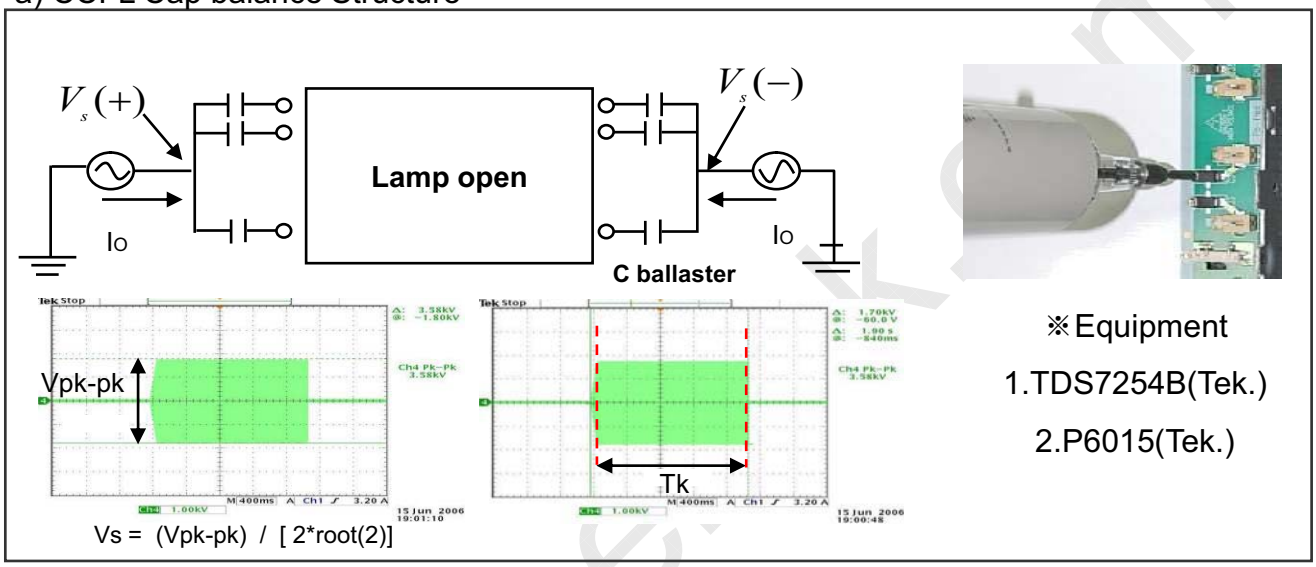



**Figure 1 . CCFL Vopen**

b) EEFL Structure

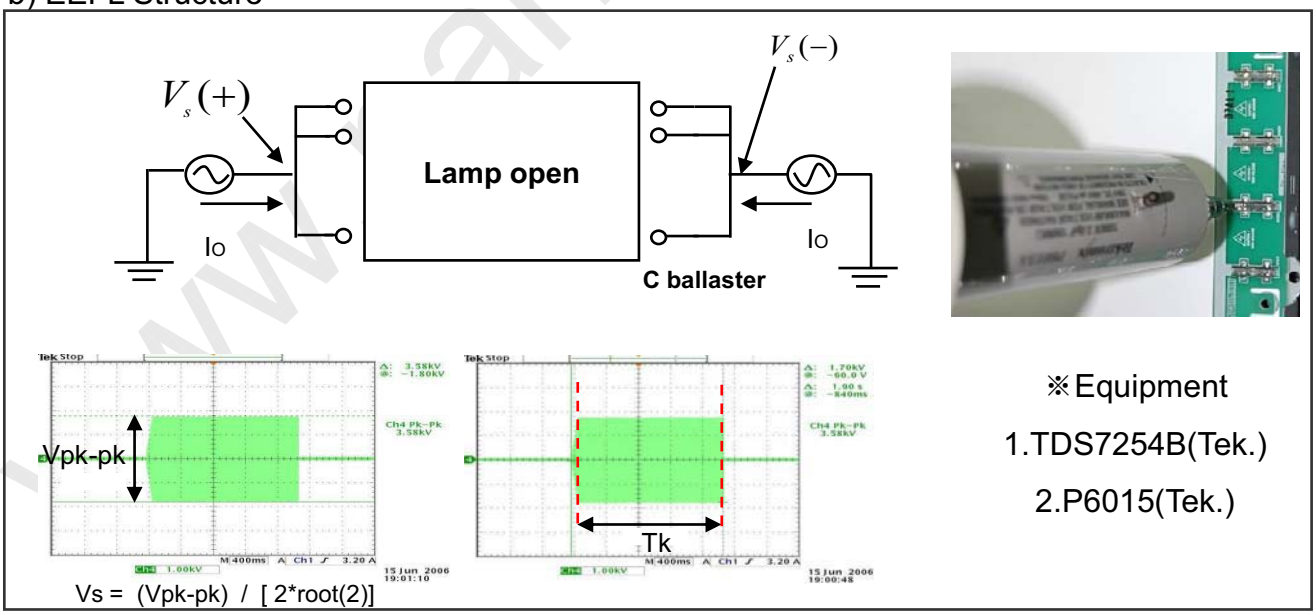



**Figure 2 . EEFL Vopen**

## # APPENDIX- VI

■ Lamp Electrical spec

| № | Item | Unit | Standards | | Notes |
|---|---|---|---|---|---|
| | | | Frequency | INV(High-High) | |
| 1 | Lamp Voltage VL | Vrms | 45kHz | 1605±7% ($I_L$=3.0mA)<br>1790±7% ($I_L$=5.0mA)<br>2075±7% ($I_L$=7.0mA)<br>2165±7% ($I_L$=7.5mA)<br>2260±7% ($I_L$=8.0mA) | Note1,3,10 |
| 2 | Starting Voltage VS | Vrms | 45kHz | Max 2240(0℃)<br>Typ 1870(0℃)<br>Max 1920(25℃)<br>Typ 1600(25℃) | Note 10,11,12 |
| 3 | Lamp Current IL | mA | | Min 3.0 mA<br>Typ 7.0 mA<br>Max 8.0 mA | Note 1,3 |
| 4 | Lamp Power IL x VL | W | 45kHz | 3.82 ($I_L$=3.0mA)<br>5.55 ($I_L$=5.0mA)<br>7.02 ($I_L$=7.0mA)<br>7.12 ($I_L$=7.5mA)<br>7.41 ($I_L$=8.0mA) | Note 1,3 |
| 5 | Average Luminance At Lamp Center L | $Cd/m^2$ | | 13500±10% ($I_L$=3.0mA,)<br>20000±10% ($I_L$=5.0mA)<br>25500±10% ($I_L$=7.0mA)<br>26500±10% ($I_L$=7.5mA,)<br>27500±10% ($I_L$=8.0mA) | Note 1,3,4 |
| 6 | Effective Light Emitting Area LE | mm | Min 792 | | Note 1,3,9 |
| 8 | Color Coordinates | x | 0.247±0.01 | | Note1,3,4 |
| | | y | 0.217±0.01 | | |

| | | | | |
|---|---|---|---|---|
| 9 | Peak spectrum (reference) | nm | Red 611<br>Green 543<br>Blue 450 | |
| 10 | Discharge Stabilization Time | min | 3 | Note 3,6 |
| 11 | Operating Frequency | kHz | 40 ~ 45(Typ) ~80 | Note 7 |
| 12 | Life Time | Hours | Min 50,000 (at 8.0mA)<br>Avg 60,000 (at 8.0mA) | **7. Life** |
| 13 | Lamp Surface Temperature | °C | Max 130( at Electrode)<br>Min 70( at Center) | Note 1,3,8 |
| 14 | Content of Mercury | mg | Min 2.0<br>Max 3.8 | |
| 15 | Solder Dipping Quantity | % | Min 95 | |
| 16 | Gas Pressure | Torr | (Typ)34±4 | Note 3 |

Note 1) Started at IL=7.5(mA) and measure 3minutes later.

2) Voltage at switch on. Inverter output voltage.

3) Ambient Temperature should be 25±1°C under no wind.

4) The center/center part of lamp shall be measured.

5) Luminance uniformity is as follows.

Luminance uniformity = Min / Max × 100 (%)

Max = max luminance which is in the area of effective lighting length.

Min = min luminance which is in the area of effective lighting length.

6) The time needed to achieve not less than 95% luminance of the center / center part of lamp.

The center / center part of lamp shall be measured. The luminance of the lamp after lighted for 3minutes is defined as 100%.

7) The frequency range can be keep within ±10% range of electrical and optical characteristics(except the chromaticity).

8) This is temperature difference between high voltage electrode and low voltage electrode(except the lamp end to 30mm).

9) The measurement Inverter is limited to the Hi-Hi.

10) The measurement NF OSS33229 Hi-Hi Voltage Type.

11) The measurement Ids 4.0 Level and Vds 10.0 Level.(NF OSS3329)

12) Be measured of ambient 0°C . Before testing the lamp is left for 24hours

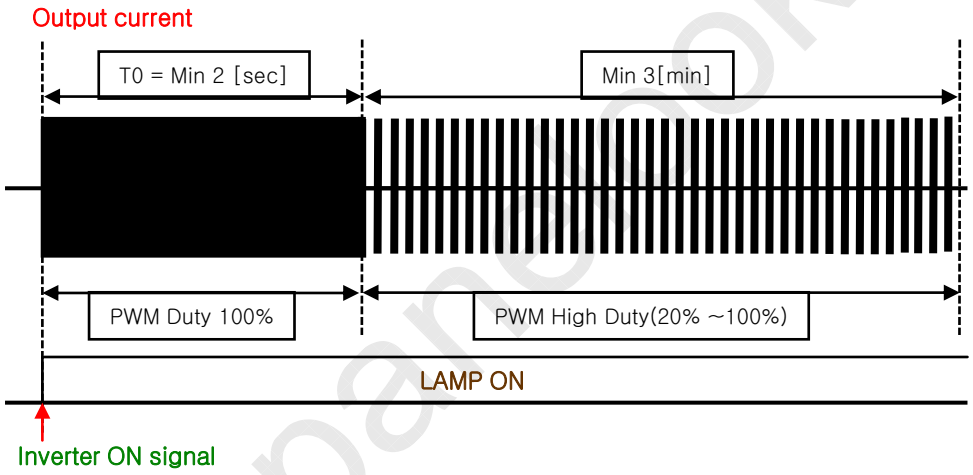
**# APPENDIX- VII-1**

# Mega DCR using condition(1)

- **After Inverter ON signal, PWM Duty 100% should be sustained during 2sec.**
- **It is recommended not to sustain more than 10 min for Deep Dimming (Low duty of the inverter output current 0%~20%).**

The deep dimming must be used very carefully due to limitation of lamp characteristics and specification.

1) For stable lamp on, its duty condition should follow below the condition.
After Inverter ON signal, T0 duration should be sustained.




2) Low duty(0%~20%) of **the inverter output current**, B/L may not satisfy some of LCM specification.

- Duration : the low duty operation(0 ~ 20%) must be limited within 10 minutes for one time operation.

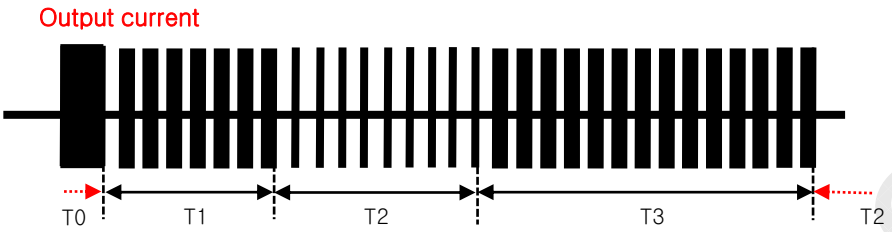
- Ratio : the period of the low duty operation must be less than 1/5 compare to that of the high duty operation(20~100%) in a certain period to prevent unwanted operation.

- FOS : partial darkness or darkness of center area during the low duty might be happened due to insufficient lamp current.

- Warm up : the low duty must be used 3 min after the lamps "ON". In case of low temperature, more warm up time may be needed.

**# APPENDIX- VII-2**

# Mega DCR using condition(2)




| Parameter | Value | | | Unit | Note |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| T1 | 3 | - | - | min | PWM High Duty[20~100%] |
| T2 | - | - | 10 | min | PWM Low Duty[0~20%] |
| T3 | T2 x 5 | - | - | min | PWM High Duty[20~100%] |

3) The output current duty may not be same as input PWM duty due to rise/fall time of output.

4) Following the recommended conditions as aforementioned, there is no difference of lamp lifetime between conventional method and new one.