Ordering number : EN*5610A

CMOS LSI

LC374500ST

Internal Synchronization Silicon Gate 4M (524288-word × 8-bit) mask ROM Pin Compatible with Flash Memory

Preliminary

Overview

The LC374500ST is a 524288-word × 8-bit (4M) mask programmable ROM that is pin compatible with flash memory. Since this product supports the wide operating voltage range of 2.6 to 5.5 V and achieves access times of 100 ns (t_{CA}) when V_{CC} is between 4.5 and 5.5 V and 200 ns when V_{CC} is between 2.6 and 5.5 V, it can be used both in high-speed 5-V systems and battery-operated 3-V systems. Since this product is pin compatible with flash memory it can replace flash memory used during prototyping and production.

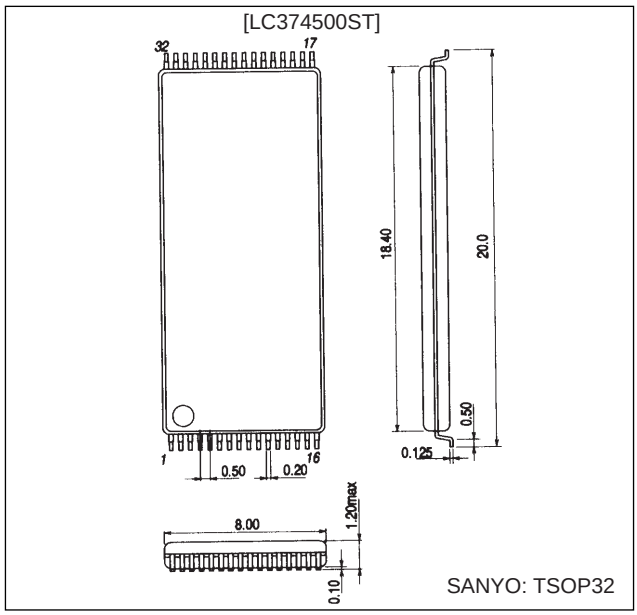
Features

- 524288-word × 8-bit organization
- Wide supply voltage range: 2.6 to 5.5 V
- Access times (t_{AA}): 120 ns (maximum) at V_{CC} = 4.5 to 5.5 V
  (t_{CA}): 100 ns (maximum) at V_{CC} = 4.5 to 5.5 V
  200 ns (maximum) at V_{CC} = 2.6 to 5.5 V
- Operating supply current: 50 mA (maximum)
- Standby mode supply current: 30 µA (maximum)
- Fully static operation (internal synchronization)
- Three-state outputs
- Pin compatible with flash memory
- Package—32-pin TSOP (8 × 20 mm) plastic package: LC374500ST

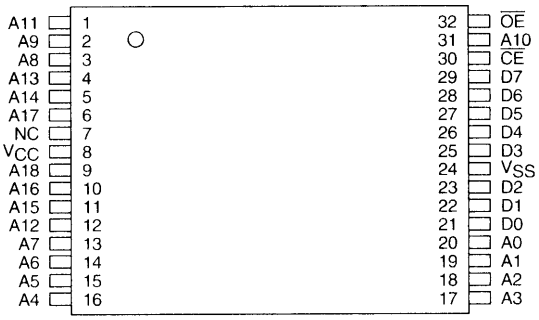
Package Dimensions

unit: mm

3224-TSOP32



Pin Assignment

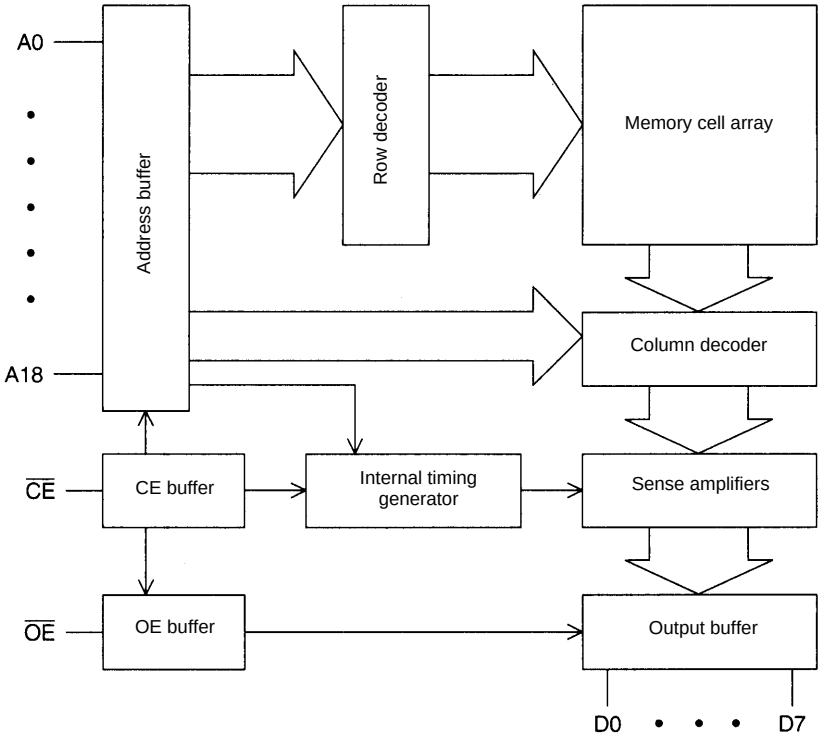


Top view

Pin Functions

A0 to A18	Address input
Do to D7	Data output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Function Logic Table

$\overline{CE}$	$\overline{OE}$	Output pin state	Supply current
H	X	High-impedance	Standby mode current
L	H	High-impedance	Operating mode current
L	L	DOUT	Operating mode current

Note: “X” indicates either a high or a low level.

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit	Note
Supply voltage	V_{CC}		–0.3 to +7.0	V	1
Input pin voltage	V_{IN}		–0.3 to V_{CC} + 0.3	V	1, 2
Output pin voltage	V_{OUT}		–0.3 to V_{CC} + 0.3	V	1
Allowable power dissipation	Pd max	Ta = 25°C, reference value for the Sanyo DIP.	1.0	W	1
Operating temperature	Topr		–10 to +70	°C	1
Storage temperature	Tstg		–55 to +125	°C	1

Note: 1. This device may be permanently damaged by stresses in excess of those listed in the maximum ratings. These are stress ratings only, and functional operation of the device at these conditions or any other conditions beyond those listed in the “DC Allowable Operating Ranges” item is not implied.
2. The minimum value is –3.0 V for pulse widths of under 30 ns.

Capacitance Characteristics at Ta = 25°C, f = 1.0 MHz

Parameter	Symbol	Conditions	Ratings			Unit	Note
			min	typ	max		
Input pin capacitance	C_{IN}	V_{IN} = 0 V, reference value for the Sanyo DIP.			8	pF	3
Output pin capacitance	C_{OUT}	V_{OUT} = 0 V, reference value for the Sanyo DIP.			10	pF	3

Note: 3. These parameters are sampled, and are not measured for every unit.

DC Allowable Operating Ranges at Ta = –10 to +70°C, V_{CC} = 2.6 to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{CC}		2.6	5.0	5.5	V
Input high-level voltage	V_{IH}		2.2		V_{CC} + 0.3	V
Input low-level voltage	V_{IL}		–0.3		+0.6	V

DC Electrical Characteristics at Ta = –10 to +70°C, V_{CC} = 2.6 to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operating current	I_{CCA1}	$\overline{CE}$ = 0.2 V, V_I = V_{CC} – 0.2 V/0.2 V			30	µA
	I_{CCA2}	$\overline{CE}$ = V_{IL}, I_O = 0 mA, V_L = V_{IH}/V_{IL}, f = 10 MHz			55	mA
Standby current	I_{CCS1}	$\overline{CE}$ = V_{CC} – 0.2 V			30 (1.0)	µA
	I_{CCS2}	$\overline{CE}$ = V_{IH}			1.0 (300)	mA (µA)
Input leakage current	I_{LI}	V_{IN} = 0 to V_{CC}			±1.0	µA
Output leakage current	I_{LO}	$\overline{CE}$ or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 to V_{CC}			±1.0	µA
Output high-level voltage	V_{OH}	I_{OH} = –0.5 mA	0.8 V_{CC}			V
Output low-level voltage	V_{OL}	I_{OL} = 0.5 mA			0.2	V

Note: Values in parentheses are guaranteed at Ta = 25°C.

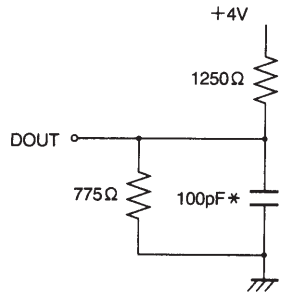
AC Characteristics at Ta = –10 to +70°C, V_{CC} = 2.6 to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Cycle time	t_{CYC}		200			ns
Address access time	t_{AA}				200 (120)	ns
$\overline{CE}$ access time	t_{CA}				200 (100)	ns
$\overline{OE}$ access time	t_{OA}				80 (40)	ns
Output hold time	t_{OH}		20			ns
Output disable time*	t_{OD}				100	ns

Note: Values in parentheses are for V_{CC} = 4.5 to 5.5 V
*: t_{OD} is defined as the time between the rise of either $\overline{CE}$ or $\overline{OE}$, whichever comes first, and the point when the output goes to the high-impedance state.
These parameters are sampled, and are not measured for every unit.

Test Conditions

Input voltage amplitude	0.4 V to 2.8 V
Rise/fall time	5 ns
Input discrimination level	1.5 V
Output discrimination level	1.5 V
Output capacitance	See figure 1



*: Includes the oscilloscope and jig capacitances.

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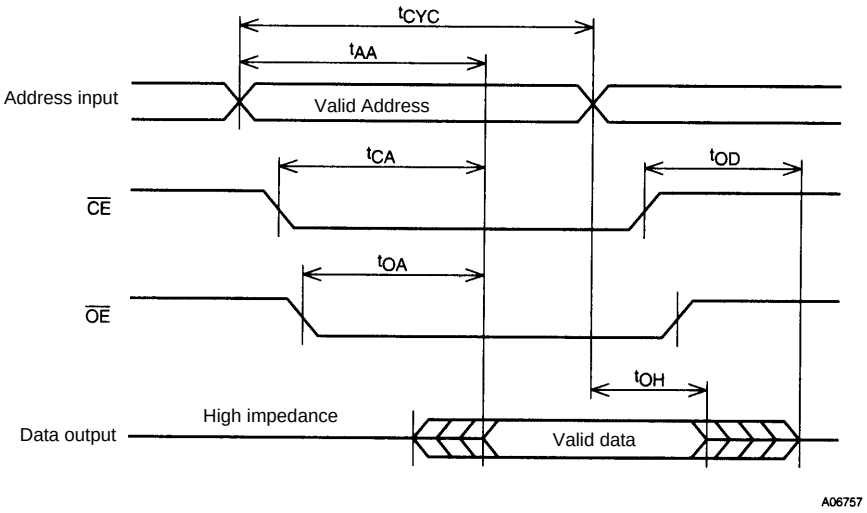
Figure 1 Output Load Circuit

Timing Waveforms



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Notes on System Design

This LSI adopts the ATD technique, in which operation starts when a change in either the $\overline{CE}$ or address inputs is detected. This means that the output data immediately after power is applied is invalid. When using this LSI as program memory for Z80 and similar microprocessors, applications must take into account the fact that valid data will not be output after power is first applied unless the value of either the $\overline{CE}$ or at least one of the address lines is changed after the power supply has stabilized.

Another point due to the use of the ATD technique is that this LSI is sensitive to input noise. Do not apply voltages outside the allowable DC input levels for extended periods and do not apply input voltages with large noise components.