SPECIFICATION
FOR
APPROVAL

( ) **Preliminary Specification**

(●) **Final Specification**

Title	42.0” WUXGA TFT LCD

BUYER	LGE
MODEL	

SUPPLIER	**RAKEN Co., Ltd.**
*MODEL	LC420EUG
SUFFIX	**RDV2**

*When you obtain standard approval,
please use the above model name without suffix

APPROVED BY	SIGNATURE DATE
/	
/	
/	

Please return 1 copy for your confirmation with your signature and comments.

APPROVED BY	SIGNATURE DATE
Charlie.Ko/ Team Leader	
REVIEWED BY	
Power.Zheng/ Engineer	
PREPARED BY	
Suxi.Jiang/ Engineer	

TV R&D LCM Qualification Dept.
RAKEN Co., Ltd.

LCM ENGINEERING SPECIFICATION

*MODEL	LC420EUG
SUFFIX	RDV2
Update	July. 05. 2011

( ) **Preliminary Specification**

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APPROVED BY	SIGNATURE	DATE
Peter. Kim / TV RD Leader		
Charlie. Ko / LCM Qualification Leader		
Herbert. Jung / EE Dept Leader		
Brainy. Jeong / ME Dept Leader		
Marco.Du / Power Dept Leader		

TV R&D Center. RAKEN Co., Ltd.

File No. :_____

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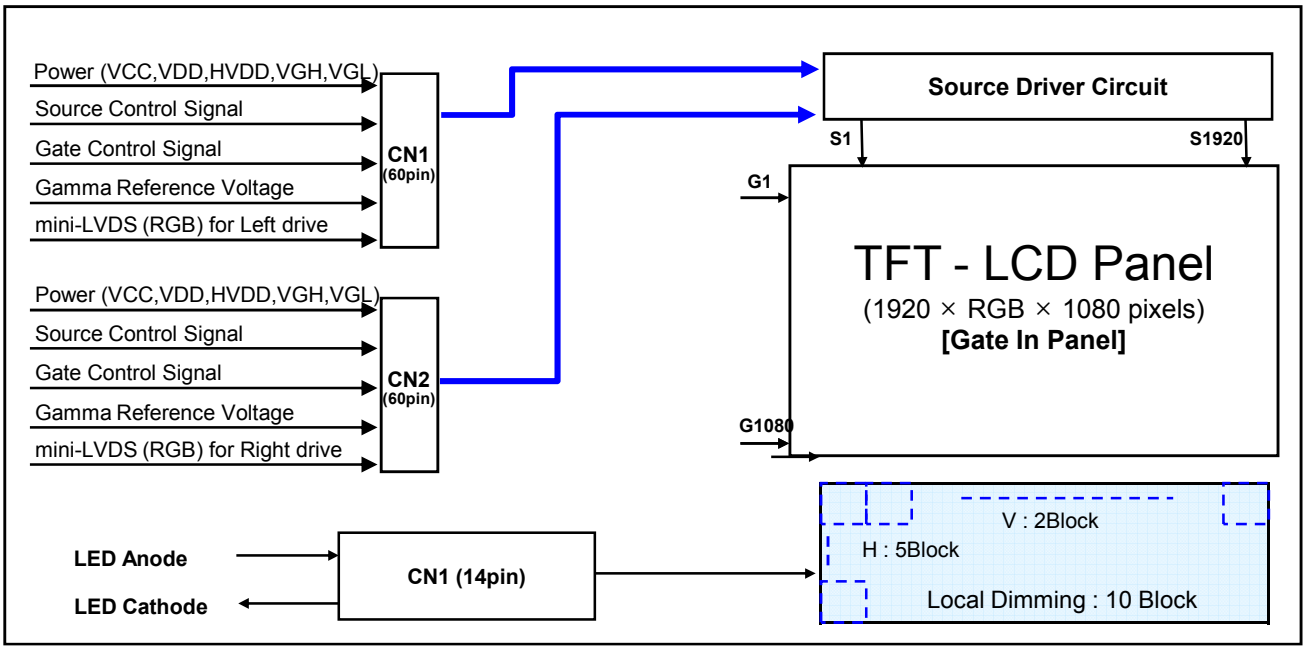
1. General Description

The LC420EUG is a Color Active Matrix Liquid Crystal Display with an integral the Source PCB and Gate implanted on Panel (GIP). The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally black mode. It has a 42.02 inch diagonally measured active display area with WUXGA resolution (1080 vertical by 1920 horizontal pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the luminance of the sub-pixel color is determined with a 8-bit gray scale signal for each dot. Therefore, it can present a palette of more than 16.7M(true) colors.
It is intended to support LCD TV, PCTV where high brightness, super wide viewing angle, high color gamut, high color depth and fast response time are important.



General Features

Active Screen Size	42.02 inches(1067.31mm) diagonal
Outline Dimension	968.4(H) × 564(V) X 10.8(B)/18.3 mm(D) (Typ.)
Pixel Pitch	0.4845 mm x 0.4845 mm
Pixel Format	1920 horiz. by 1080 vert. Pixels, RGB stripe arrangement
Color Depth	8bit, 16,7 M colors
Luminance, White	360 cd/m2 (Center 1point ,Typ.)
Viewing Angle (CR>10)	Viewing angle free (R/L 178 (Min.), U/D 178 (Min.))
Power Consumption	Total 92.9W (TBD.) [Logic= 7.3W, LED Backlight=85.6W (Ext.PWM=100%)]
Weight	8.8 Kg (Typ.)
Display Operating Mode	Transmissive mode, normally black
Surface Treatment	Hard coating(3H), Anti-glare treatment of the front polarizer (Haze 10%)

2. Absolute Maximum Ratings

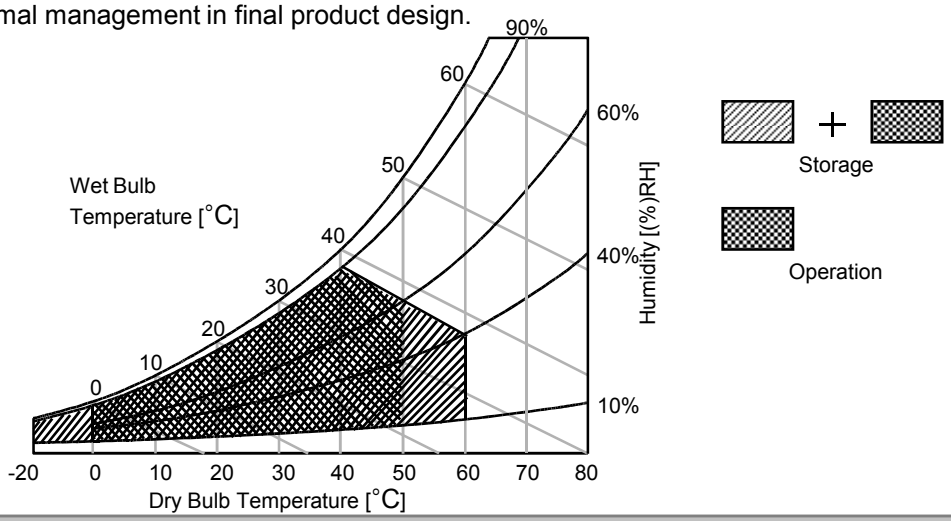
The following items are maximum values which, if exceeded, may cause faulty operation or permanent damage to the LCD module.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value		Unit	Note
		Min	Max		
Logic Power Voltage	VCC	-0.5	+4.0	VDC	1
Gate High Voltage	VGH	+18.0	+30.0	VDC	
Gate Low Voltage	VGL	-8.0	-4.0	VDC	
Source D-IC Analog Voltage	VDD	-0.3	+18.0	VDC	
Gamma Ref. Voltage (Upper)	VGMH	½VDD-0.5	VDD+0.5	VDC	
Gamma Ref. Voltage (Low)	VGML	-0.3	½ VDD+0.5	VDC	
LED Input voltage (Forward voltage)	Vf	-	+TBD	VDC	
Panel Front Temperature	TSUR	-	+68	˚C	4
Operating Temperature	TOP	0	+50	˚C	2,3
Storage Temperature	TST	-20	+60	˚C	
Operating Ambient Humidity	HOP	10	90	%RH	
Storage Humidity	HST	10	90	%RH	

Note1. Ambient temperature condition (Ta = 25 ± 2 ˚C)

2. Temperature and relative humidity range are shown in the figure below.
   Wet bulb temperature should be Max 39°C, and no condensation of water.
3. Gravity mura can be guaranteed below 40°C condition.
4. The maximum operating temperatures is based on the test condition that the surface temperature of display area is less than or equal to 68°C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 68℃. The range of operating temperature may be degraded in case of improper thermal management in final product design.



3. Electrical Specifications

3-1. Electrical Characteristics

It requires several power inputs. The VCC is the basic power of LCD Driving power sequence, Which is used to logic power voltage of Source D-IC and GIP.

Table 2. ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Note
Logic Power Voltage	VCC	-	3.0	3.3	3.6	VDC	
Logic High Level Input Voltage	VIH	-	2.7	-	VCC	VDC	
Logic Low Level Input Voltage	VIL	-	0	-	0.6	VDC	
Source D-IC Analog Voltage	VDD	-	16.5	16.7	16.9	VDC	
Half Source D-IC Analog Voltage	H_VDD	-	8.05	8.35	8.55	VDC	7
Gamma Reference Voltage	V_{GMH}	(GMA1 ~ GMA9)	8.35	-	16.5	VDC	
	V_{GML}	(GMA10 ~ GMA18)	0.2	-	8.35	VDC	
Common Voltage	Vcom	Normal	6.75	7.05	7.35	V	
		Reverse	6.75	7.05	7.35	V	
Mini-LVDS Clock frequency	CLK	3.0V≤VCC ≤3.6V		-	156	MHz	
mini-LVDS input Voltage (Center)	VIB	Mini-LVDS Clock and Data	0.7 + (VID/2)	-	(VCC-1.2) − VID / 2	V	5
mini-LVDS input Voltage Distortion (Center)	ΔVIB		-	-	0.8	V	
mini-LVDS differential Voltage range	VID		200	-	800	mV	
mini-LVDS differential Voltage range Dip	ΔVID		25	-	800	mV	
Gate High Voltage	VGH	@ 25℃	27.7	28	28.3	VDC	
		@ 0℃	28.7	29	29.3	VDC	
Gate Low Voltage	VGL	-	-5.2	-5.0	-4.8	VDC	
GIP Bi-Scan Voltage	VGI_P VGI_N	-	VGL	-	VGH	VDC	
GIP Refresh Voltage	VGH even/odd	-	VGL	-	VGH	V	
GIP Start Pulse Voltage	VST	-	VGL	-	VGH	V	
GIP Operating Clock	GCLK	-	VGL	-	VGH	V	
Total Power Current	ILCD	-		610	790	mA	1
Total Power Consumption	PLCD	-		7.32	8.05	Watt	1

Note: 1. The specified current and power consumption are under the VLCD=12V., 25 ± 2°C, f_V=60Hz condition whereas mosaic pattern(8 x 6) is displayed and f_V is the frame frequency.
2. The above spec is based on the basic model.
3. All of the typical gate voltage should be controlled within 1% voltage level
4. Ripple voltage level is recommended under 10%
5. In case of mini-LVDS signal spec, refer to Fig 2 for the more detail.
6. Logic Level Input Signal : SOE,POL,GSP
7. HVDD Voltage level is half of VDD and it should be between Gamma9 and Gamma10.

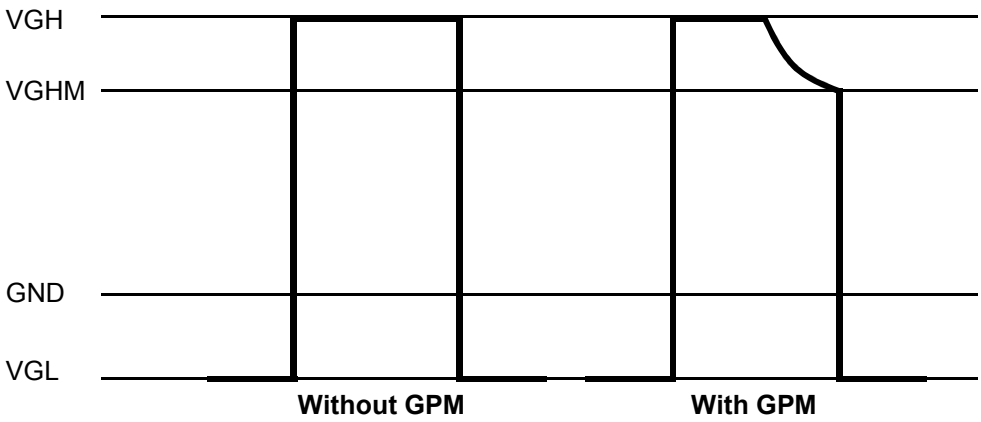


FIG. 1 Gate Output Wave form without GPM and with GPM

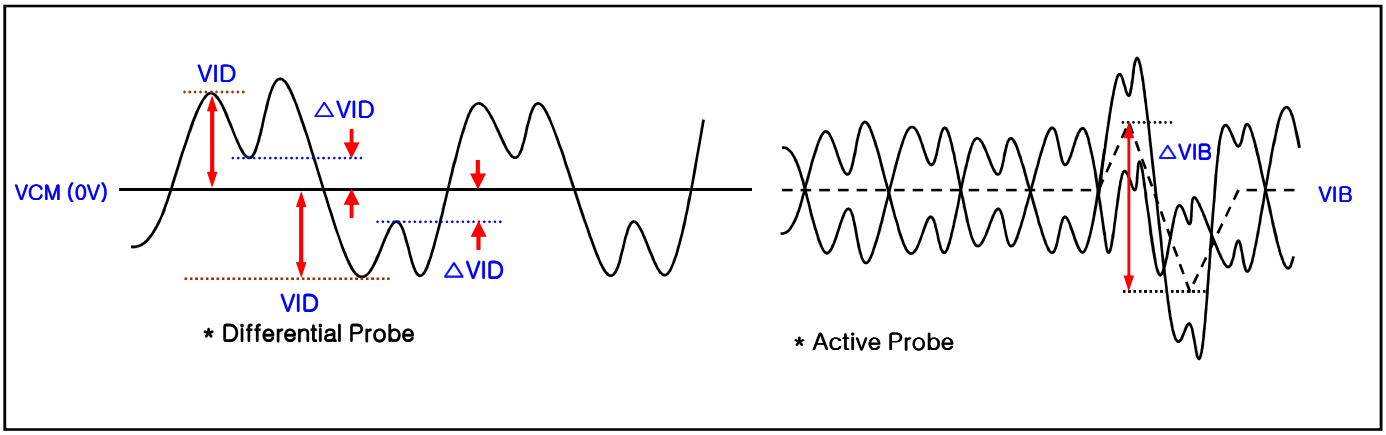


FIG. 2 Description of VID, ΔVIB, ΔVID

* Source PCB

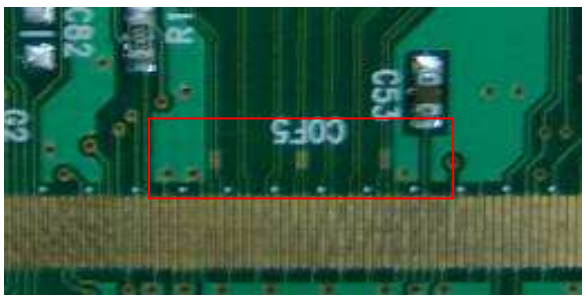


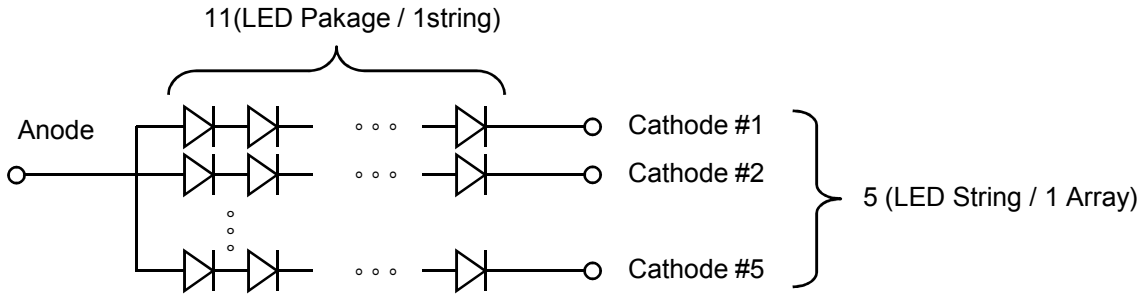
FIG. 3 Measure point

Table 3. ELECTRICAL CHARACTERISTICS (Continue)

Parameter		Symbol	Values			Unit	Note
			Min	Typ	Max		
Backlight Assembly :							
Forward Current (one array)	Anode	$I_{F\ (anode)}$		525		mAdc	±5%
	Cathode	$I_{F\ (cathode)}$	99.8	105	110.3	mAdc	2, 3
Forward Voltage		V_F	63.8	70.4	77.0	Vdc	4
Forward Voltage Variation		$\triangle V_F$			1.7	Vdc	5
Power Consumption		P_{BL}	-	85.6	95.0	W	6
Burst Dimming Duty		On duty	1		90	%	
Burst Dimming Frequency		1/T	95		182	Hz	8
LED Array : (APPENDIX-V)							
Life Time			30,000	50,000		Hrs	7

Note : The design of the LED driver must have specifications for the LED array in LCD Assembly.
The electrical characteristics of LED driver are based on Constant Current driving type.
The performance of the LED in LCM, for example life time or brightness, is extremely influenced by the characteristics of the LED Driver. So, all the parameters of an LED driver should be carefully designed.
When you design or order the LED driver, please make sure unwanted lighting caused by the mismatch of the LED and the driver (no lighting, flicker, etc) has never been occurred. When you confirm it, the LCD–Assembly should be operated in the same condition as installed in your instrument.

1. Electrical characteristics are based on LED Array specification.
2. Specified values are defined for a Backlight Assembly. (IBL : 2 LED array, 525mA/LED array)
3. Each LED array has one anode terminal and five cathode terminals.
   The forward current(I_F) of the anode terminal is 525mA and it supplies 105mA into five strings, respectively



4. The forward voltage(V_F) of LED array depends on ambient temperature (Appendix-V)
5. ΔV_F means Max V_F-Min V_F in one Backlight. So V_F variation in a Backlight isn't over Max. 1.7V
6. Maximum level of power consumption is measured at initial turn on.
   Typical level of power consumption is measured after 1hrs aging at 25 ± 2°C.
7. The life time(MTTF) is determined as the time at which brightness of the LED is 50% compared to that of initial value at the typical LED current on condition of continuous operating at 25 ± 2°C, based on duty 100%.
8. The reference method of burst dimming duty ratio.
   It is recommended to use synchronous V-sync frequency to prevent waterfall
   (Vsync x 1 =Burst Frequency)
   Though PWM frequency is over 182Hz (max252Hz), function of backlight is not affected.

3-2. Interface Connections

This LCD module employs two kinds of interface connection, two 60-pin FFC connector are used for the module electronics.

3-2-1. LCD Module

-LCD Connector (CN1): TF06L-60S-0.5SH (Manufactured by HRS)

Table 3-1. MODULE CONNECTOR(CN1) PIN CONFIGURATION

No	Symbol	Description	No	Symbol	Description
1	LTD_OUT	LTD OUTPUT	31	NC	No Connection
2	NC	No Connection	32	NC	No Connection
3	GCLK1	GIP GATE Clock 1	33	NC	No Connection
4	GCLK2	GIP GATE Clock 2	34	LCLK -	Left Mini LVDS Receiver Clock Signal(-)
5	GCLK3	GIP GATE Clock 3	35	LCLK +	Left Mini LVDS Receiver Clock Signal(+)
6	GCLK4	GIP GATE Clock 4	36	LLV2 -	Left Mini LVDS Receiver Signal(2-)
7	GCLK5	GIP GATE Clock 5	37	LLV2 +	Left Mini LVDS Receiver Signal(2+)
8	GCLK6	GIP GATE Clock 6	38	LLV1 -	Left Mini LVDS Receiver Signal(1-)
9	VGI_N	GIP Bi-Scan (Normal =VGL Rotate = VGH)	39	LLV1 +	Left Mini LVDS Receiver Signal(1+)
10	VGI_P	GIP Bi-Scan (Normal =VGH Rotate = VGL)	40	LLV0 -	Left Mini LVDS Receiver Signal(0-)
11	VGH_ODD	GIP Panel VDD for Odd GATE TFT	41	LLV0 +	Left Mini LVDS Receiver Signal(0+)
12	VGH_EVEN	GIP Panel VDD for Even GATE TFT	42	GND	Ground
13	VGL	GATE Low Voltage	43	SOE	Source Output Enable SIGNAL
14	VST	VERTICAL START PULSE	44	POL	Polarity Control Signal
15	GIP_Reset	GIP Reset	45	GSP	GATE Start Pulse
16	VCOM_L_FB	VCOM Left Feed-Back Output	46	H_CONV	"H“ H 2dot Inversion/ "L" H 1dot Inversion
17	VCOM_L	VCOM Left Input	47	OPT_N	“H” Normal Display / “L” Rotation Display
18	GND	Ground	48	GND	Ground
19	GND	Ground	49	GMA 18	GAMMA VOLTAGE 18 (Output From LCD)
20	VDD	Driver Power Supply Voltage	50	GMA 16	GAMMA VOLTAGE 16
21	VDD	Driver Power Supply Voltage	51	GMA 15	GAMMA VOLTAGE 15
22	H_VDD	Half Driver Power Supply Voltage	52	GMA 14	GAMMA VOLTAGE 14
23	H_VDD	Half Driver Power Supply Voltage	53	GMA 12	GAMMA VOLTAGE 12
24	GND	Ground	54	GMA 10	GAMMA VOLTAGE 10 (Output From LCD)
25	VCC	Logic Power Supply Voltage	55	GMA 9	GAMMA VOLTAGE 9 (Output From LCD)
26	VCC	Logic Power Supply Voltage	56	GMA 7	GAMMA VOLTAGE 7
27	GND	Ground	57	GMA 5	GAMMA VOLTAGE 5
28	NC	No Connection	58	GMA 4	GAMMA VOLTAGE 4
29	NC	No Connection	59	GMA 3	GAMMA VOLTAGE 3
30	NC	No Connection	60	GMA 1	GAMMA VOLTAGE 1(Output From LCD)

Note :

1. Please refer to application note for details.
   (**GIP & Gamma Voltage setting**)

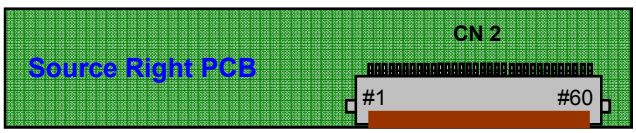
-LCD Connector (CN2): TF06L-60S-0.5SH(Manufactured by HRS)

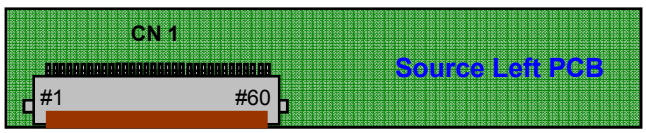
Table 3-2. MODULE CONNECTOR(CN2) PIN CONFIGURATION

No	Symbol	Description		No	Symbol	Description
1	GMA 1	GAMMA VOLTAGE 1 (Output From LCD)		31	RLV1 +	Right Mini LVDS Receiver Signal(1+)
2	GMA 3	GAMMA VOLTAGE 3		32	RLV0 -	Right Mini LVDS Receiver Signal(0-)
3	GMA 4	GAMMA VOLTAGE 4		33	RLV0 +	Right Mini LVDS Receiver Signal(0+)
4	GMA 5	GAMMA VOLTAGE 5		34	GND	Ground
5	GMA 7	GAMMA VOLTAGE 7		35	VCC	Logic Power Supply Voltage
6	GMA 9	GAMMA VOLTAGE 9 (Output From LCD)		36	VCC	Logic Power Supply Voltage
7	GMA 10	GAMMA VOLTAGE 10 (Output From LCD)		37	GND	Ground
8	GMA 12	GAMMA VOLTAGE 12		38	H_VDD	Half Driver Power Supply Voltage
9	GMA 14	GAMMA VOLTAGE 14		39	H_VDD	Half Driver Power Supply Voltage
10	GMA 15	GAMMA VOLTAGE 15		40	VDD	Driver Power Supply Voltage
11	GMA 16	GAMMA VOLTAGE 16		41	VDD	Driver Power Supply Voltage
12	GMA 18	GAMMA VOLTAGE 18 (Output From LCD)		42	GND	Ground
13	GND	Ground		43	GND	Ground
14	OPT_N	“H” Normal Display / “L” Rotation Display		44	VCOM_R	VCOM Right Input
15	H_CONV	"H“ H 2dot Inversion/ "L" H 1dot Inversion		45	VCOM_R_FB	VCOM Right Feed-Back Output
16	GSP	GATE Start Pulse		46	GIP_Reset	GIP Reset
17	POL	Polarity Control Signal		47	VST	VERTICAL START PULSE
18	SOE	Source Output Enable SIGNAL		48	VGL	GATE Low Voltage
19	GND	Ground		49	VGH_EVEN	GIP Panel VDD for Even GATE TFT
20	NC	No Connection		50	VGH_ODD	GIP Panel VDD for Odd GATE TFT
21	NC	No Connection		51	VGI_P	GIP Bi-Scan (Normal =VGH Rotate = VGL)
22	NC	No Connection		52	VGI_N	GIP Bi-Scan (Normal =VGL Rotate = VGH)
23	NC	No Connection		53	GCLK6	GIP GATE Clock 6
24	NC	No Connection		54	GCLK5	GIP GATE Clock 5
25	NC	No Connection		55	GCLK4	GIP GATE Clock 4
26	RCLK -	Right Mini LVDS Receiver Clock Signal(-)		56	GCLK3	GIP GATE Clock 3
27	RCLK +	Right Mini LVDS Receiver Clock Signal(+)		57	GCLK2	GIP GATE Clock 2
28	RLV2 -	Right Mini LVDS Receiver Signal(2-)		58	GCLK1	GIP GATE Clock 1
29	RLV2 +	Right Mini LVDS Receiver Signal(2+)		59	NC	No Connection
30	RLV1 -	Right Mini LVDS Receiver Signal(1-)		60	LTD_OUT	LTD OUTPUT

Note :

1. Please refer to application note for details (**GIP** & **Gamma Voltage setting**)





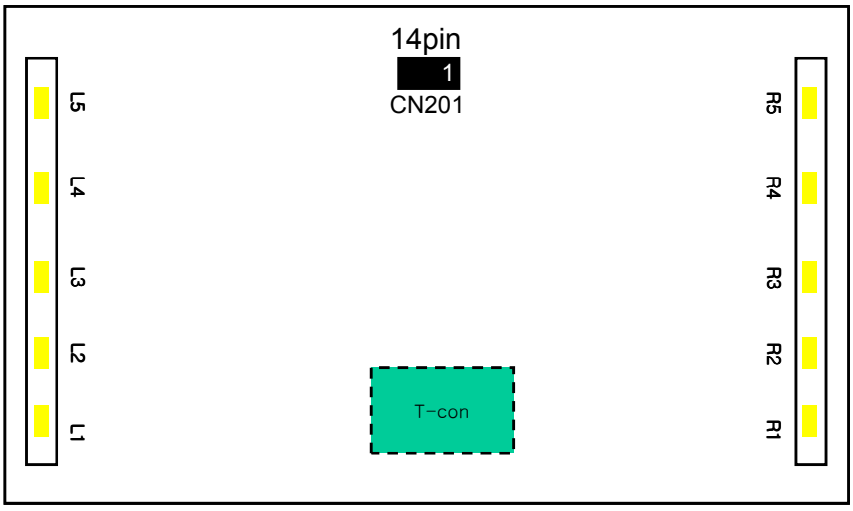
3-2-2. Backlight Module

- LED Array assy Connector(Plug) : 20022HS - 14B2 or Equivalent
- Mating Connector(Receptacle) : 20022WR - H14B1 (Yeonho) or Equivalent

Table 5. BACKLIGHT CONNECTOR PIN CONFIGURATION(CN201,CN202)

Pin No	Symbol	Description	Note
1	Anode R1~R5	LED Input Current	
2	N.C	Open	
3	R1 Cathode	LED Output Current	
4	R2 Cathode	LED Output Current	
5	R3 Cathode	LED Output Current	
6	R4 Cathode	LED Output Current	
7	R5 Cathode	LED Output Current	
8	L5 Cathode	LED Output Current	
9	L4 Cathode	LED Output Current	
10	L3 Cathode	LED Output Current	
11	L2 Cathode	LED Output Current	
12	L1 Cathode	LED Output Current	
13	N.C	Open	
14	Anode L1~L5	LED Input Current	

◆ Rear view of LCM



3-3. Signal Timing Specifications

Table 4. Timing Requirements

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Mini Clock pulse period	T_1	-	3.2	3.4	-	ns	1
Mini Clock pulse low period	T_2	-	1.6	-	-	ns	
Mini Clock pulse high period	T_3	-	1.6	-	-	ns	
Mini Data setup time	T_6	-	0.55	-	-	ns	
Mini Data hold time	T_7	-	0.55	-	-	ns	
Reset low to SOE rising time	T_8	-	0	-	-	ns	
SOE to Reset input time	T_9	-	200	-	-	ns	
Receiver off to SOE timing	T_{10}	-	10	-	-	CLK cycle	
POL signal to SOE setup time	T_{11}	-	-5	-	-	ns	
POL signal to SOE hold time	T_{12}	-	6	-	-	ns	
Reset High Period	T_{13}	-	3	-	-	CLK cycle	
SOE signal GSP setup time	T_{14}	-	100	-	-	ns	
SOE signal GSP Hold time	T_{15}	-	100	-	-	ns	
SOE signal Pulse Width	T_{16}	-	200	-	-	ns	

Note : 1. Mini-LVDS timing measure conditions
: 268MHz < Clock Frequency < 312MHz , 200mV < VID < 800mV @ 3.0<VCC<3.3
2. Setup time and hold time couldn't be satisfied at the same time

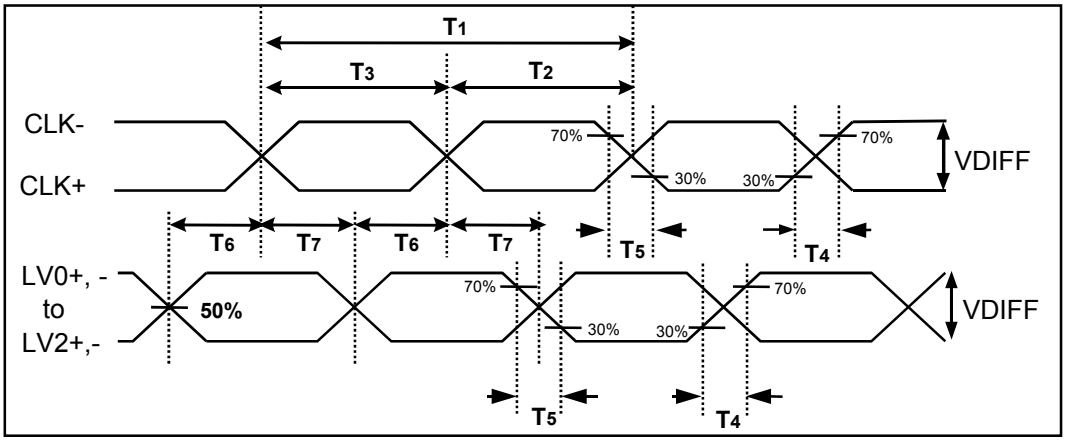


FIG 4. Source D-IC Input Data Latch Timing Waveform

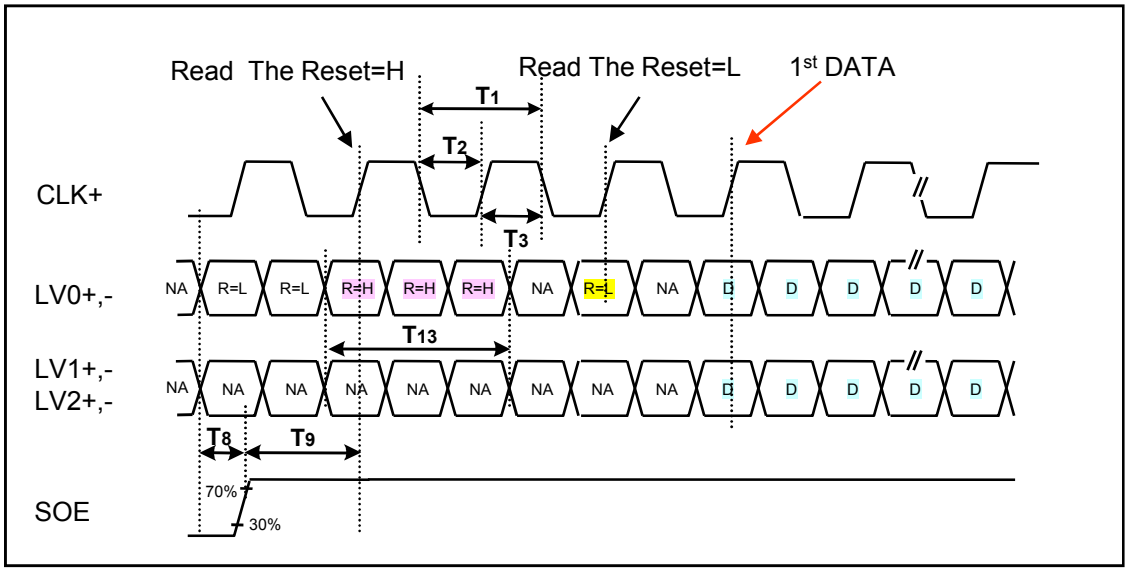


FIG 5-1. Input Data Timing for 1st Source D-IC Chip

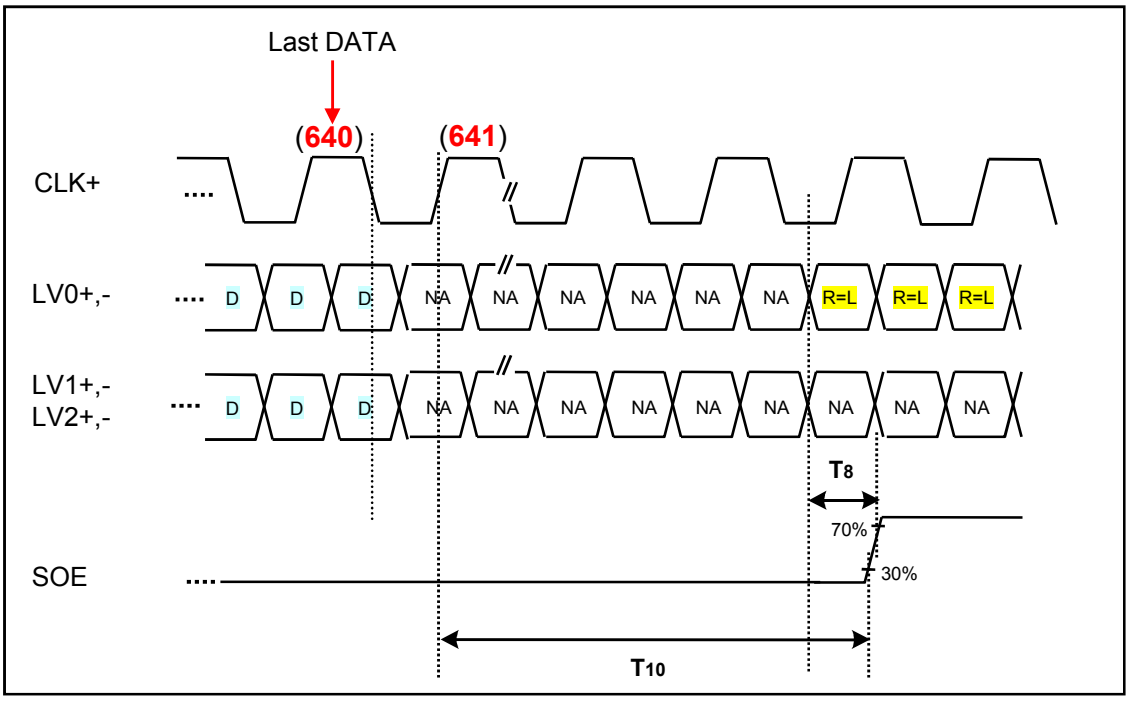


FIG 5-2. Last Data Latch to SOE Timing

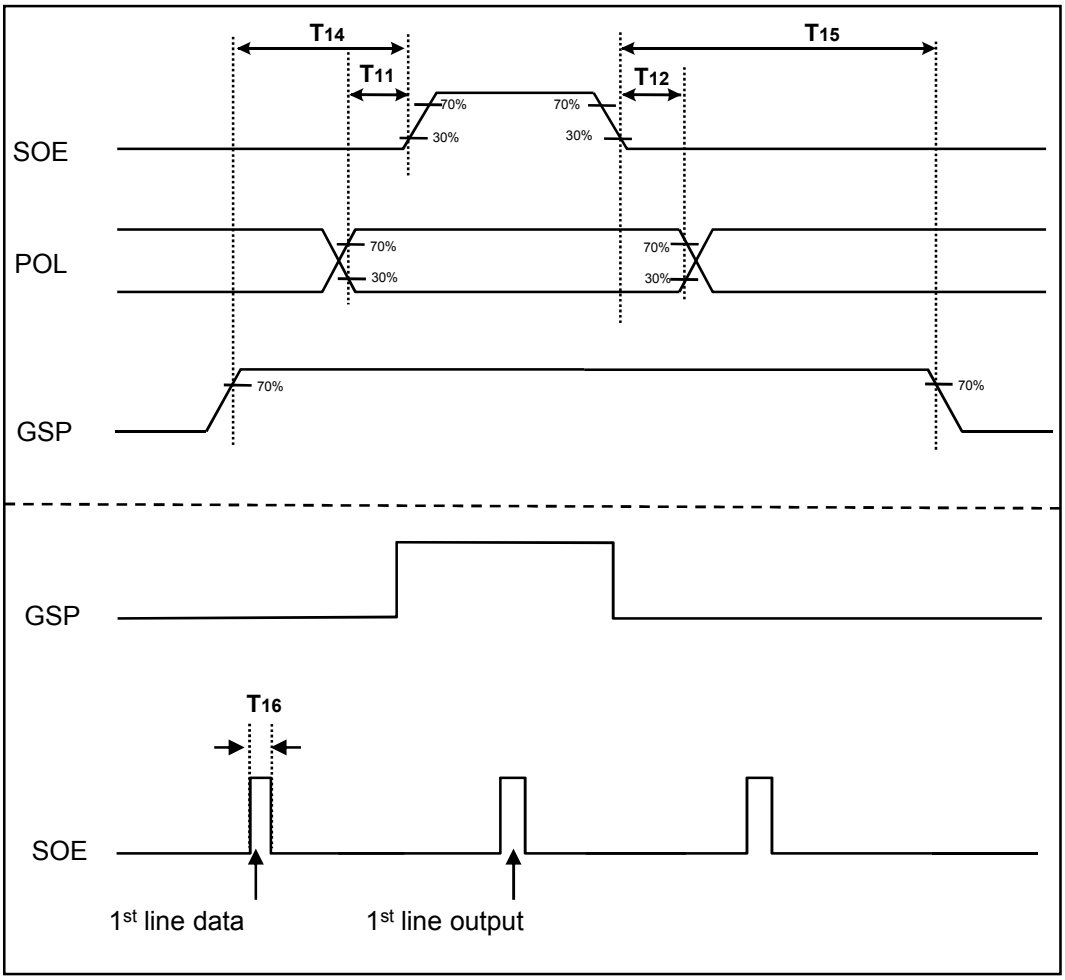
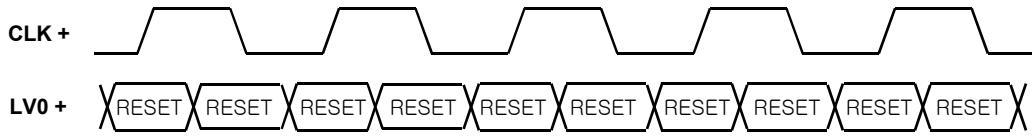


FIG 6. POL, GSP and SOE Timing Waveform

3-4. Data Mapping and Timing

Display data and control signal (RESET) are input to **LV0** to **LV2**.

3-4-1. Control signal input mode



3-4-2. Display data input mode

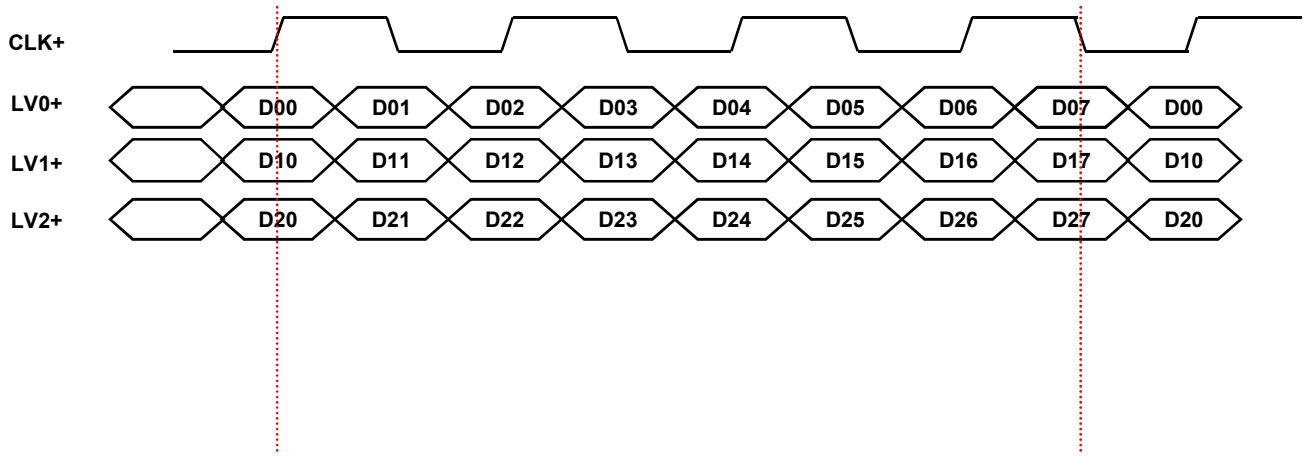


Fig. 7 Mini-LVDS Data

Note : 1. For data mapping, please refer to panel pixel structure Fig.8

3-5. Panel Pixel Structure

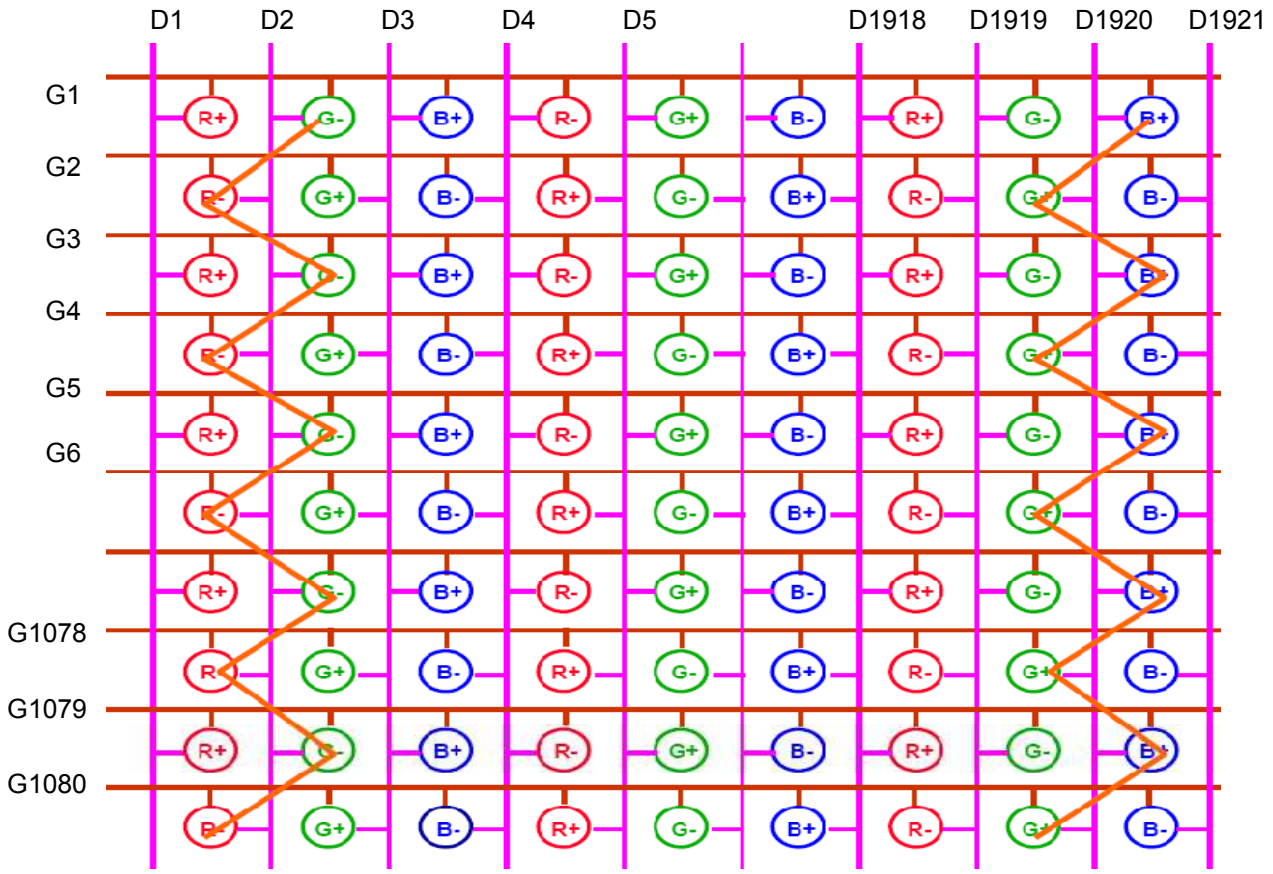


FIG. 8 Panel Pixel Structure

3-6. Power Sequence

3-6-1. LCD Driving circuit

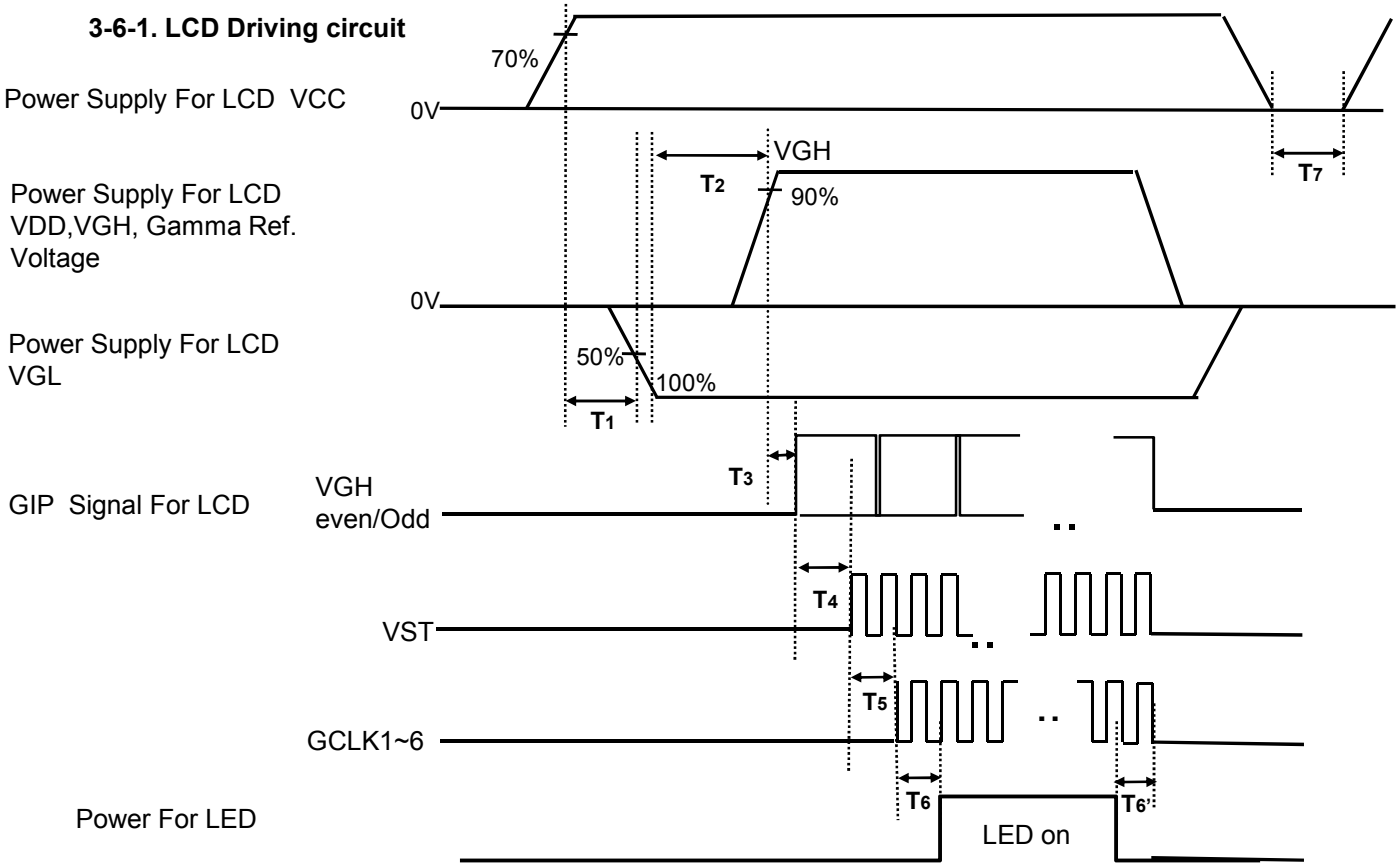


Table 3. POWER SEQUENCE

Ta= 25±2°C, fv=60Hz,

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T_1	0.5	-	-	ms	
T_2	0.5	-	-	ms	
T_3	0	-	-	ms	
T_4	10	-	-	ms	2
T_5	0	-	-	ms	
T_6 / $T_{6'}$	20	-	-	ms	6
T_7	2	-	-	s	

Note : 1. Power sequence for Source D-IC must follow the Case1 & 2.
※ Please refer to Appendix IV for more details.
2. VGH Odd signal should be started “High” status and VGH even & odd can not be “High at the same time.
3. Power Off Sequence order is reverse of Power On Condition including Source D-IC.
4. GCLK On/Off Sequence
Normal : GCLK4 → GCLK5 → GCLK6 → GCLK1 → GCLK2 → GCLK3.
Reverse :GCLK3 → GCLK2 →GCLK1 → GCLK6 → GCLK5 → GCLK4.
5. VDD_odd/even transition time should be within V_blank
6. In case of T6’, If there is no abnormal display, no problem

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable in a dark environment at 25±2°C. The values are specified at distance 50cm from the LCD surface at a viewing angle of Φ and θ equal to 0 °. FIG. 1 shows additional information concerning the measurement equipment and method.

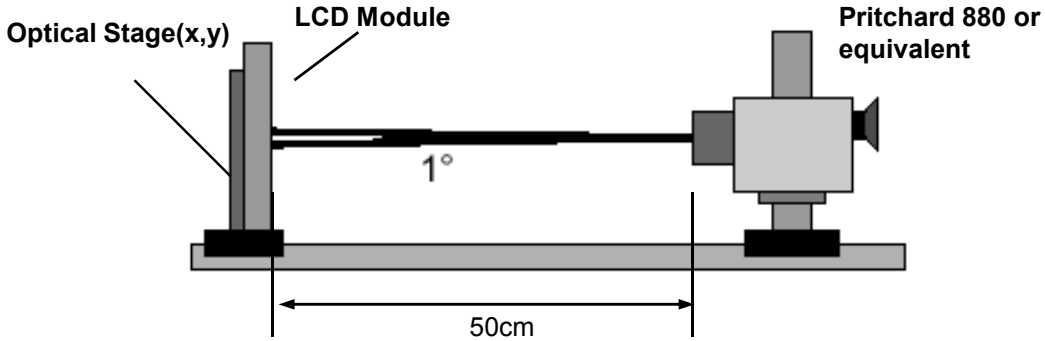


FIG. 1 Optical Characteristic Measurement Equipment and Method

Table 10. OPTICAL CHARACTERISTICS

Ta= 25±2°C, V_{LCD}=12.0V, fv=60Hz, Dclk=72.4MHz, $EXTV_{BR\_B}$=100%

Parameter		Symbol	Value			Unit	Note
			Min	Typ	Max		
Contrast Ratio		CR	1000	1400	-		1
Surface Luminance, white		L_{WH}	290	360		cd/m²	2
Luminance Variation		δ_{WHITE} 5P	-	-	1.3		3
Response Time	Variation	G to G σ		6	9	ms	5
	Gray to Gray(BW)	G to G BW		8	12	ms	4
Color Coordinates [CIE1931]	RED	Rx	Typ -0.03	0.637	Typ +0.03		
		Ry		0.341			
	GREEN	Gx		0.325			
		Gy		0.600			
	BLUE	Bx		0.152			
		By		0.051			
	WHITE	Wx		0.279			
		Wy		0.292			
Color Temperature				10,000		K	
Color Gamut				68		%	
Viewing Angle (CR>10)							
	x axis, right(ϕ=0°)	θr	89	-	-	degree	6
	x axis, left (ϕ=180°)	θl	89	-	-		
	y axis, up (ϕ=90°)	θu	89	-	-		
	y axis, down (ϕ=270°)	θd	89	-	-		
Gray Scale				-			7

Notes : 1. Contrast Ratio (CR) is defined mathematically as :

$$CR = \frac{\text{Surface Luminance at all white pixels}}{\text{Surface Luminance at all black pixels}}$$

It is measured at center 1-point.

2. Surface luminance is determined after the unit has been 'ON' and 1Hour after lighting the backlight in a dark environment at 25±2°C. Surface luminance is the luminance value at center 1-point across the LCD surface 50cm from the surface with all pixels displaying white. For more information see the FIG. 2.

3. The variation in surface luminance , δ WHITE is defined as :

δ WHITE(5P) = Maximum(L_{on1},L_{on2}, L_{on3}, L_{on4}, L_{on5}) / Minimum(L_{on1},L_{on2}, L_{on3}, L_{on4}, L_{on5})

Where L_{on1} to L_{on5} are the luminance with all pixels displaying white at 5 locations . For more information, see the FIG. 2.

4. Response time is the time required for the display to transit from any gray to white (Rise Time, Tr_R) and from any gray to black (Decay time, Tr_D). For additional information see the FIG. 3.
※ G to G_{BW} Spec stands for average value of all measured points.
Photo Detector : RD-80S / Field : 2 °

5. G to G $_\sigma$ is Variation of Gray to Gray response time composing a picture

$$G \text{ to } G\ (\sigma) = \sqrt{\frac{\Sigma(Xi - u)^2}{N}}$$

Xi = Individual Data
u = Data average
N : The number of Data

6. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD module surface. For more information, see the FIG. 4.

7. Gray scale specification
Gamma Value is approximately 2.2. For more information, see the Table 11.

Table 11. GRAY SCALE SPECIFICATION

Gray Level	Luminance [%] (Typ.)
L0	0.08
L15	0.27
L31	1.04
L47	2.49
L63	4.68
L79	7.66
L95	11.5
L111	16.1
L127	21.6
L143	28.1
L159	35.4
L175	43.7
L191	53.0
L207	63.2
L223	74.5
L239	86.7
L255	100

Measuring point for surface luminance & measuring point for luminance variation.

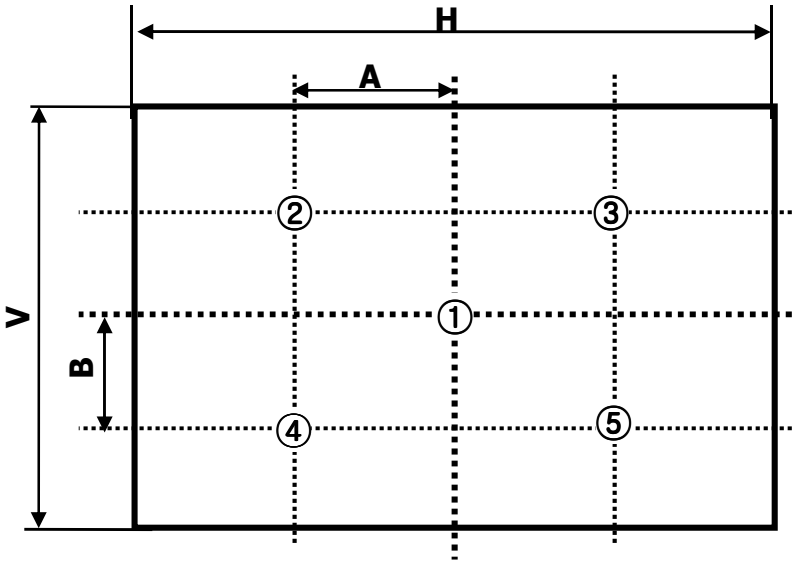


FIG. 2 5 Points for Luminance Measure

Response time is defined as the following figure and shall be measured by switching the input signal for "Gray(N)" and "Gray(M)".

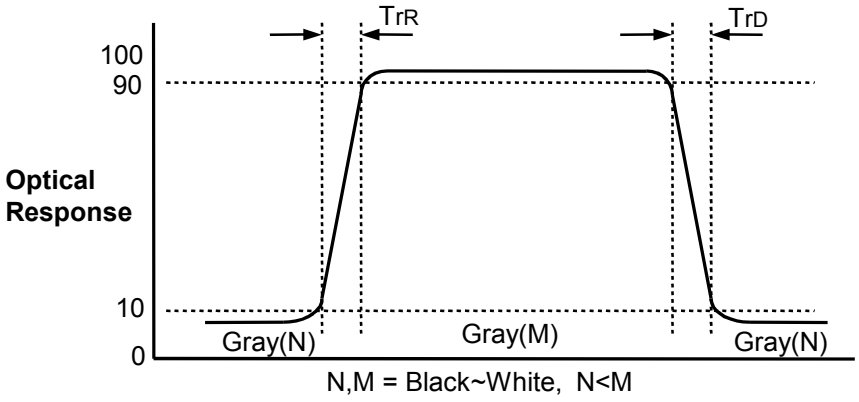


FIG. 3 Response Time

Dimension of viewing angle range

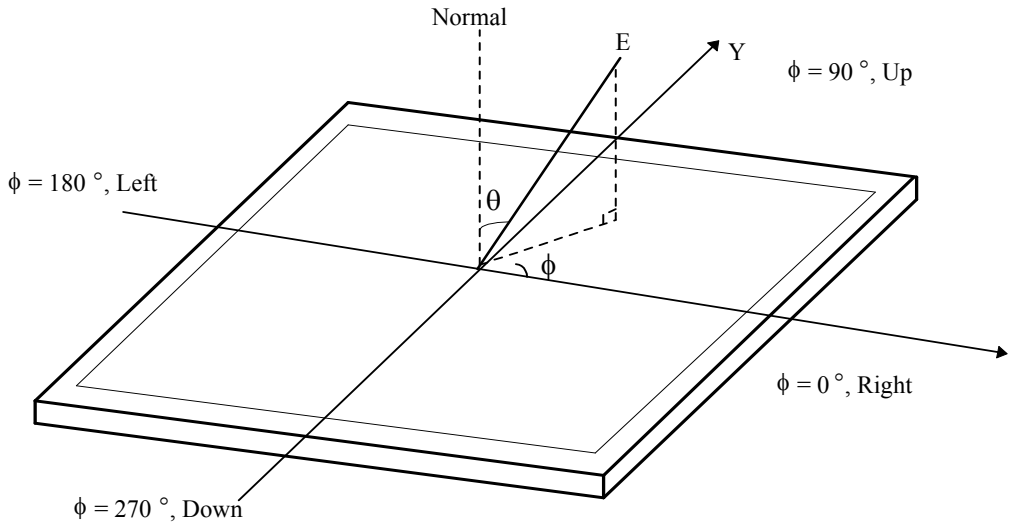


FIG. 4 Viewing Angle

FIG. 4 Viewing Angle

5. Mechanical Characteristics

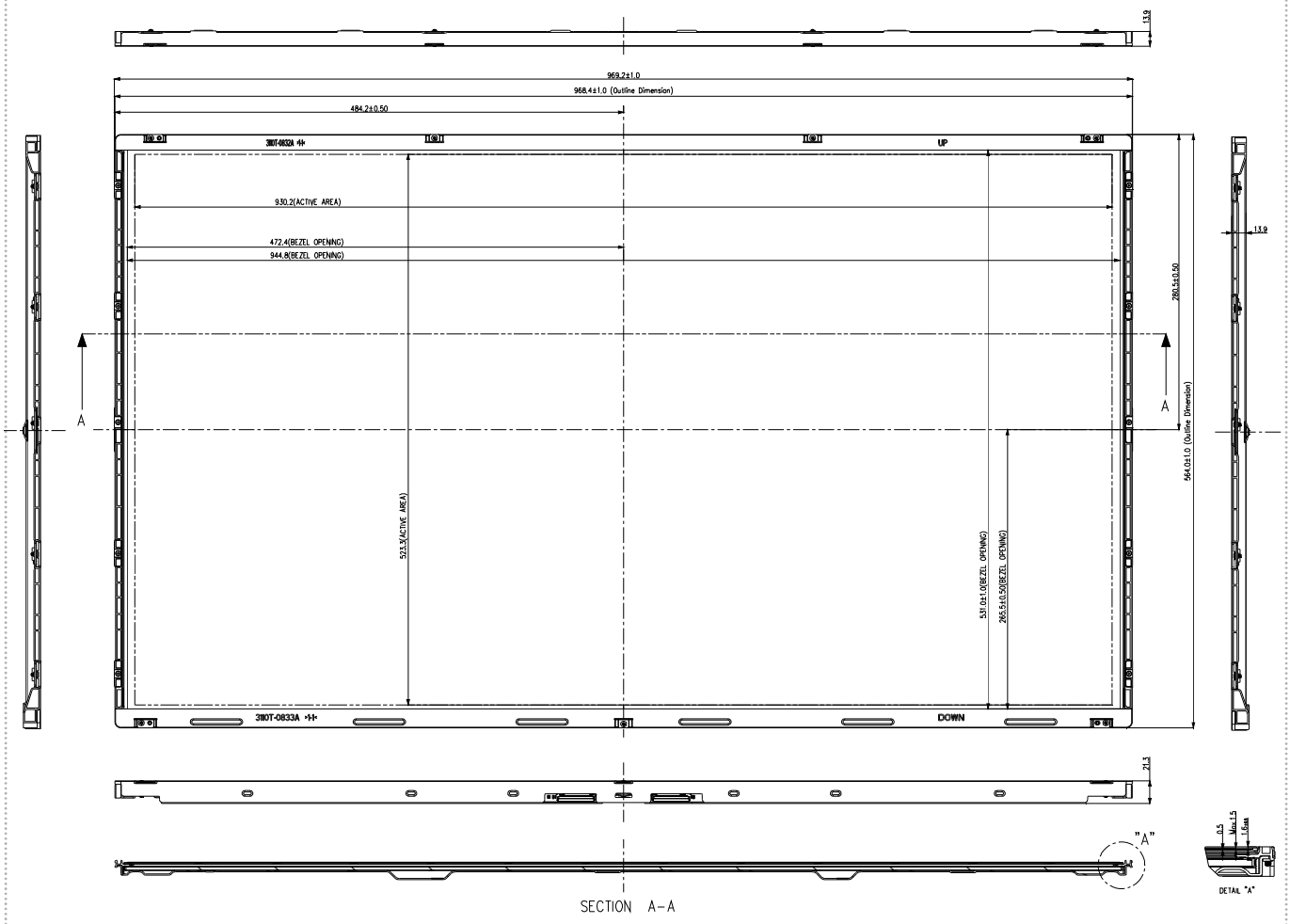
Table 12 provides general mechanical characteristics.

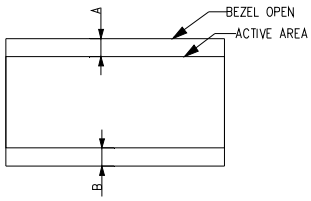
Table 12. MECHANICAL CHARACTERISTICS

Item	Value	
Outline Dimension	Horizontal	969.2 mm
	Vertical	564.0 mm
	Depth	21.3 mm
Bezel Area	Horizontal	944.8 mm (*1)
	Vertical	531.0 mm
Active Display Area	Horizontal	930.24 mm
	Vertical	523.26 mm
Weight	7.0 Kg (Typ.),7.4Kg(Max.)	

Note : Please refer to a mechanical drawing in terms of tolerance at the next page.

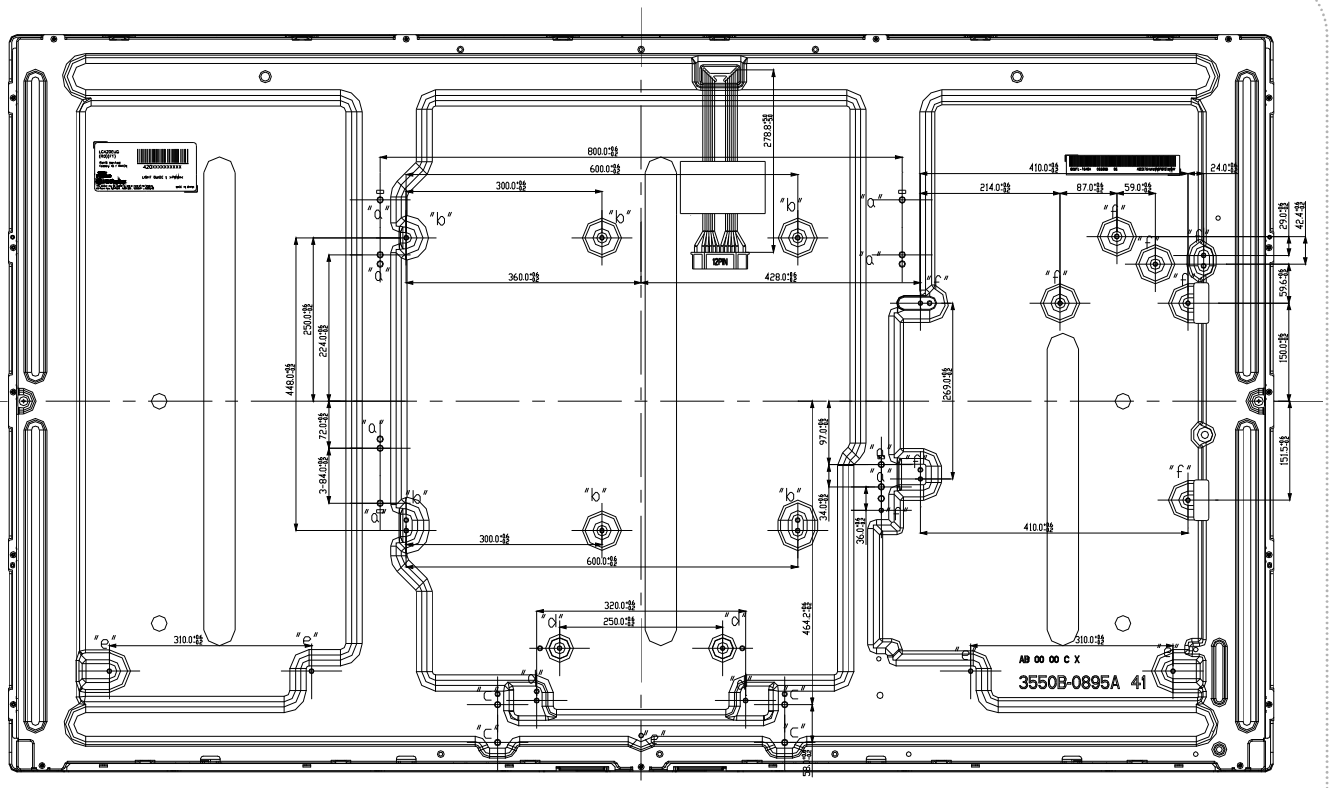
[FRONT VIEW]





NOTE
1.UNSPECIFIED TOLERANCE IS ±1.0mm
2.TILT AND PARTIAL DISPOSITION TOLERANCE OF DISPLAY AREA AS FOLLOWING.
(1) X-DIRECTION: I A-B I≤1.5
3.M3.0 TAP: Max Torque 8kgf.cm
M4.0 TAP: Max Torque 10kgf.cm

[REAR VIEW]



<TAP INFORMATION>

ITEM	TAP	MAX DEPTH(mm)	TORQUE(Kgf.cm)	NOTES
"a"	M4	7.5	Max. 8.0	-
"b"	M3	8.0	Max. 6.0	-
"c"	M4	7.5	Max. 8.0	-
"d"	M3	4.5	Max. 6.0	-
"e"	M3	7.5	Max. 6.0	-
"f"	M3	8.0	Max. 6.0	-

6. Reliability

Table 13. ENVIRONMENT TEST CONDITION

No.	Test Item	Condition
1	High temperature storage test	Ta= 60°C 240h
2	Low temperature storage test	Ta= -20°C 240h
3	High temperature operation test	Ta= 50°C 50%RH 240h
4	Low temperature operation test	Ta= 0°C 240h
5	Humidity condition Operation	Ta= 40 °C ,90%RH

Note : Before and after Reliability test, LCM should be operated with normal function.

7. International Standards

7-1. Environment

a) RoHS, Directive 2002/95/EC of the European Parliament and of the council of 27 January 2003

8. Precautions

Please pay attention to the followings when you use this TFT LCD module.

8-1. Mounting Precautions

(1) You must mount a module using specified mounting holes (Details refer to the drawings).
(2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
(4) You should adopt radiation structure to satisfy the temperature specification.
(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzine. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer
(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(9) Do not open the case because inside circuits do not have sufficient strength.

8-2. Operating Precautions

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
V=±200mV(Over and under shoot voltage)
(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer
(4) Be careful for condensation at sudden temperature change.Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.
(7) Please do not give any mechanical and/or acoustical impact to LCM. Otherwise, LCM can't be operated its full characteristics perfectly.
(8) A screw which is fastened up the steels should be a machine screw.
(if not, it can causes conductive particles and deal LCM a fatal blow)
(9) Please do not set LCD on its edge.
(10) The conductive material and signal cables are kept away from LED driver inductor to prevent abnormal display, sound noise and temperature rising.

8-3. Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

8-4. Precautions for Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

8-5. Storage

When storing modules as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
(2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.
(3) Storage condition is guaranteed under packing conditions.
(4) The phase transition of Liquid Crystal in the condition of the low or high storage temperature will be recovered when the LCD module returns to the normal condition

8-6. Handling Precautions for Protection Film

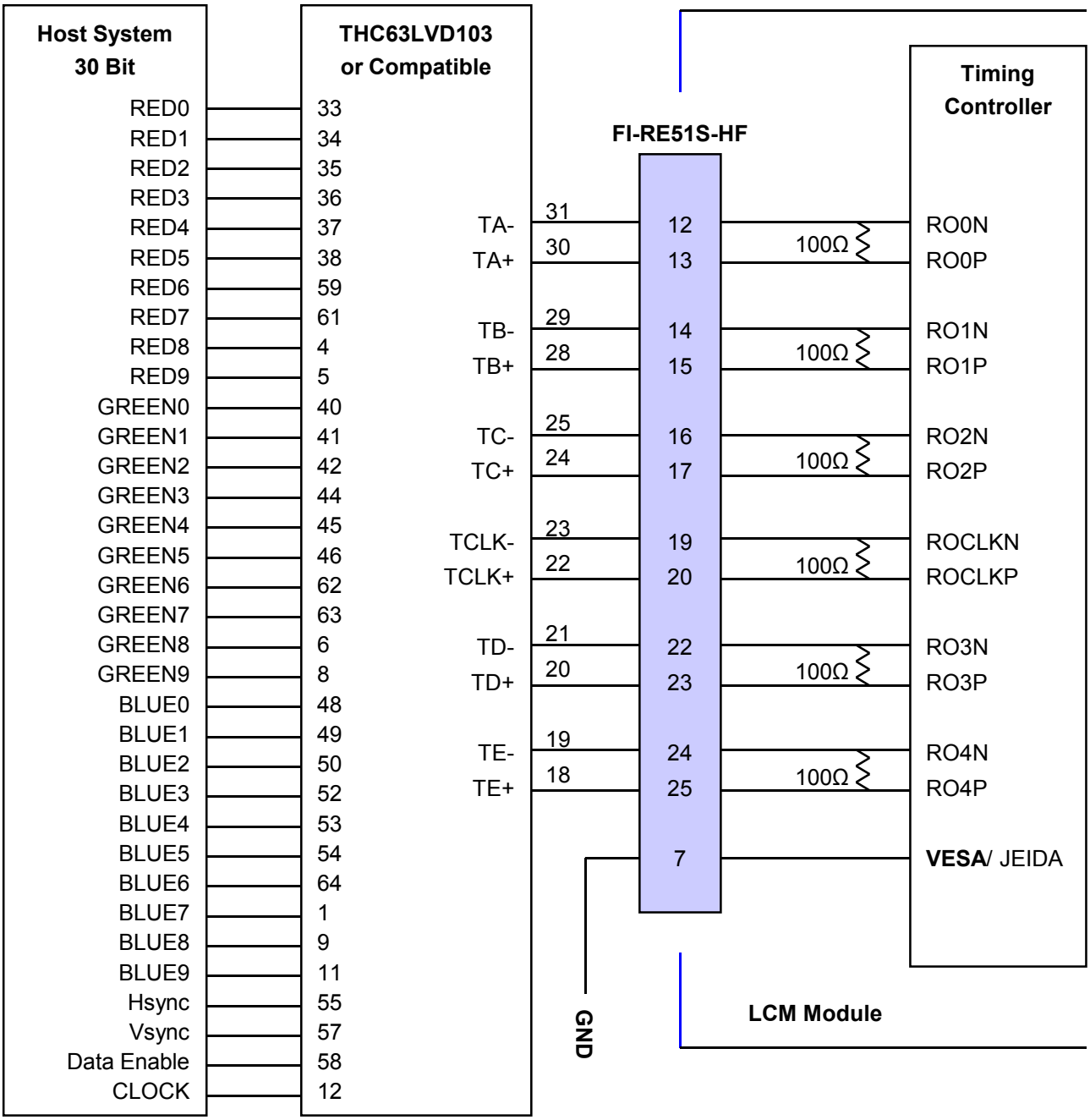
(1) The protection film is attached to the bezel with a small masking tape.
When the protection film is peeled off, static electricity is generated between the film and polarizer.
This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
(2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.
(3) You can remove the glue easily. When the glue remains on the bezel surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

 # APPENDIX- II-1

■ LCM Label

APPENDIX- II-1

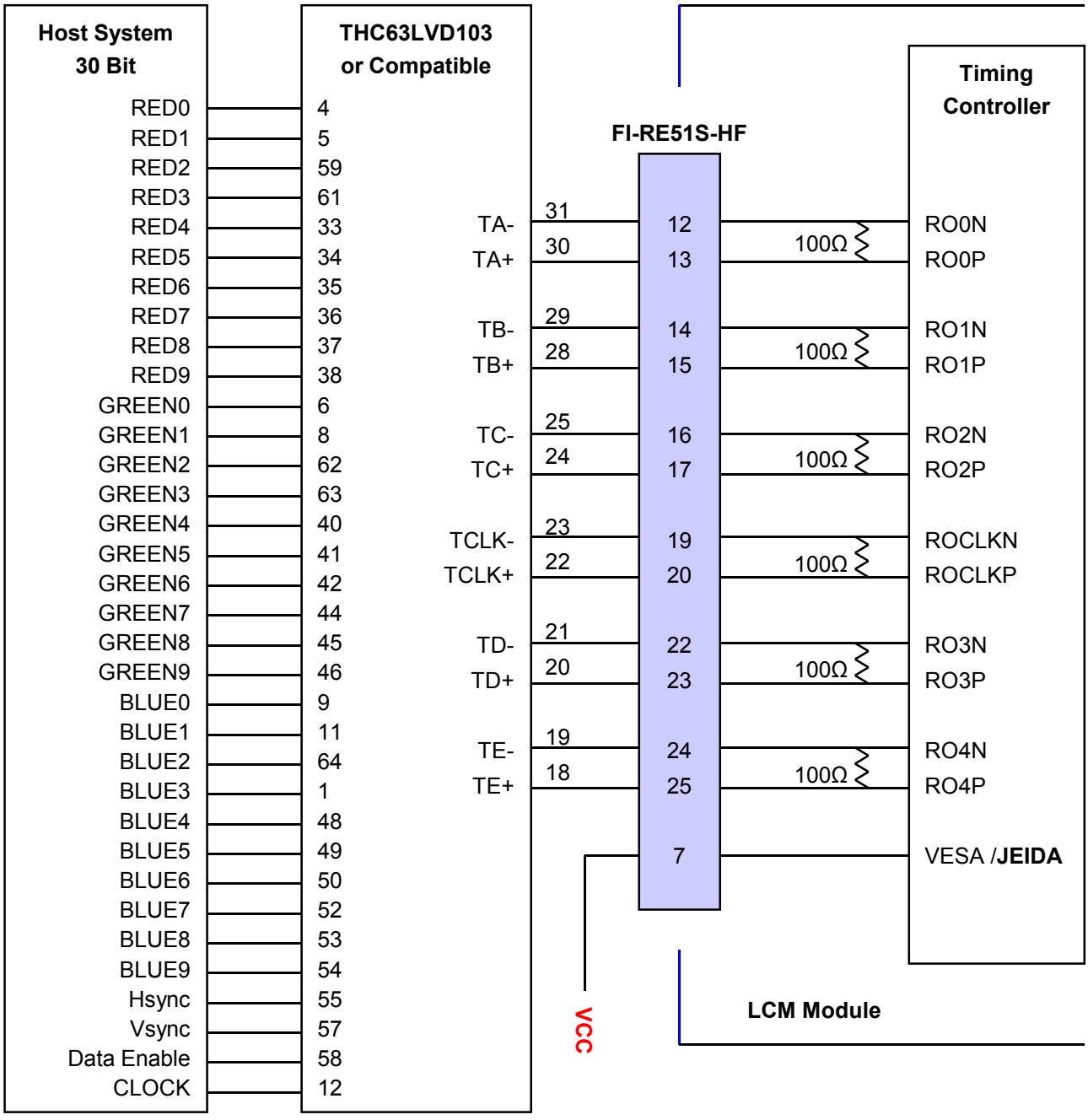
■ Required signal assignment for Flat Link (Thine : THC63LVD103) Transmitter(Pin7= **"L" or "NC**")



Note: 1. The LCD module uses a 100 Ohm[Ω] resistor between positive and negative lines of each receiver input.
2. Refer to LVDS Transmitter Data Sheet for detail descriptions. (THC63LVD103 or Compatible)
3. '9' means MSB and '0' means LSB at R,G,B pixel data.

APPENDIX- II-2

■ Required signal assignment for Flat Link (Thine : THC63LVD103) Transmitter(Pin7= **"H"**)



Note :1. The LCD module uses a 100 Ohm[Ω] resistor between positive and negative lines of each receiver input.

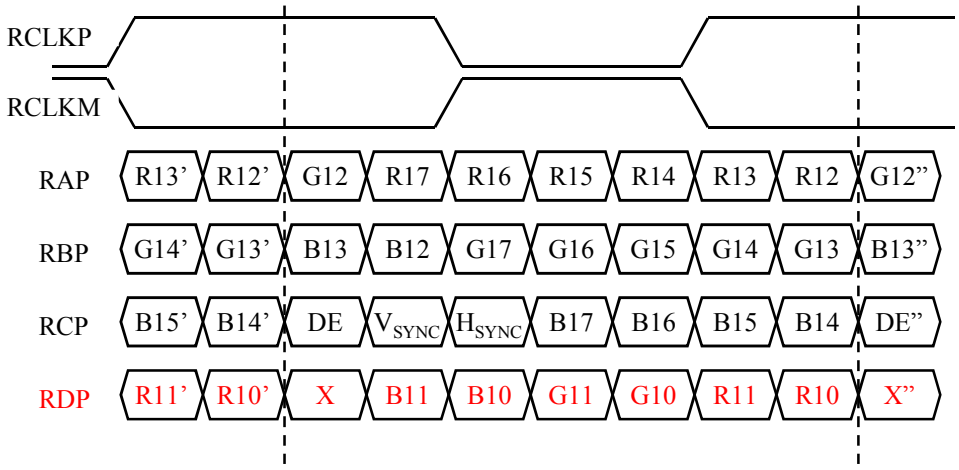
2. Refer to LVDS Transmitter Data Sheet for detail descriptions. (THC63LVD103 or Compatible)

3. '9' means MSB and '0' means LSB at R,G,B pixel data.

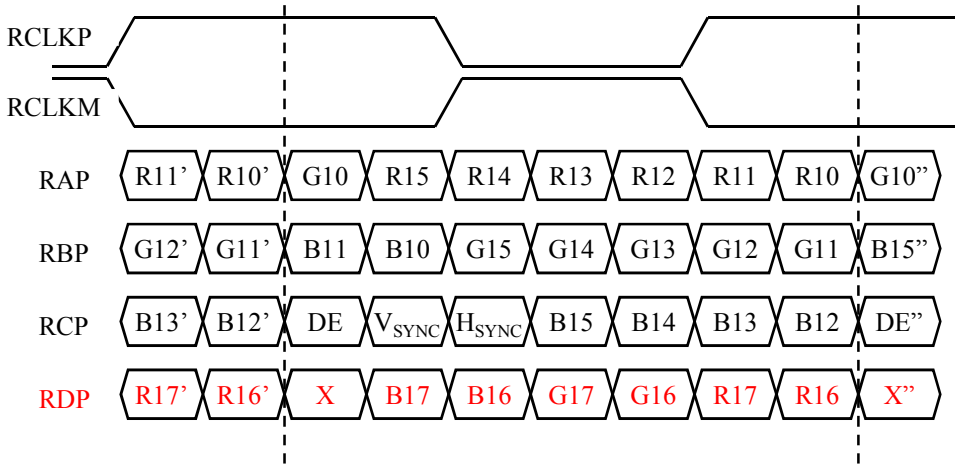
 # APPENDIX- IV

LVDS Data-Mapping info. (8bit)

■ LVDS Select : “H” Data-Mapping (JEIDA format)



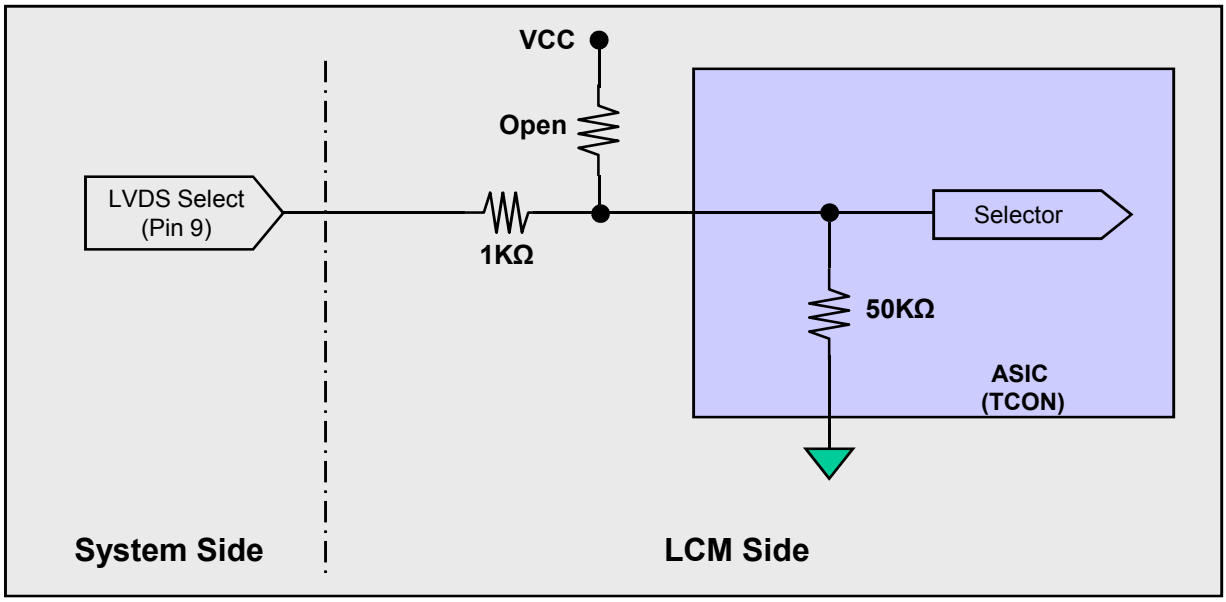
■ LVDS Select : “L” Data-Mapping (VESA format)



 # APPENDIX- V

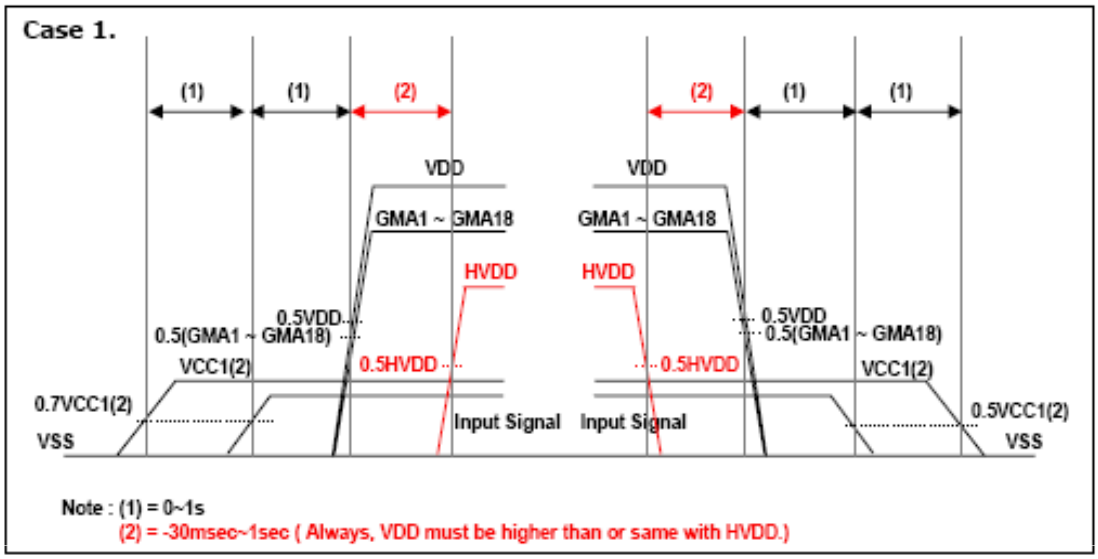
Option Pin Circuit Block Diagram

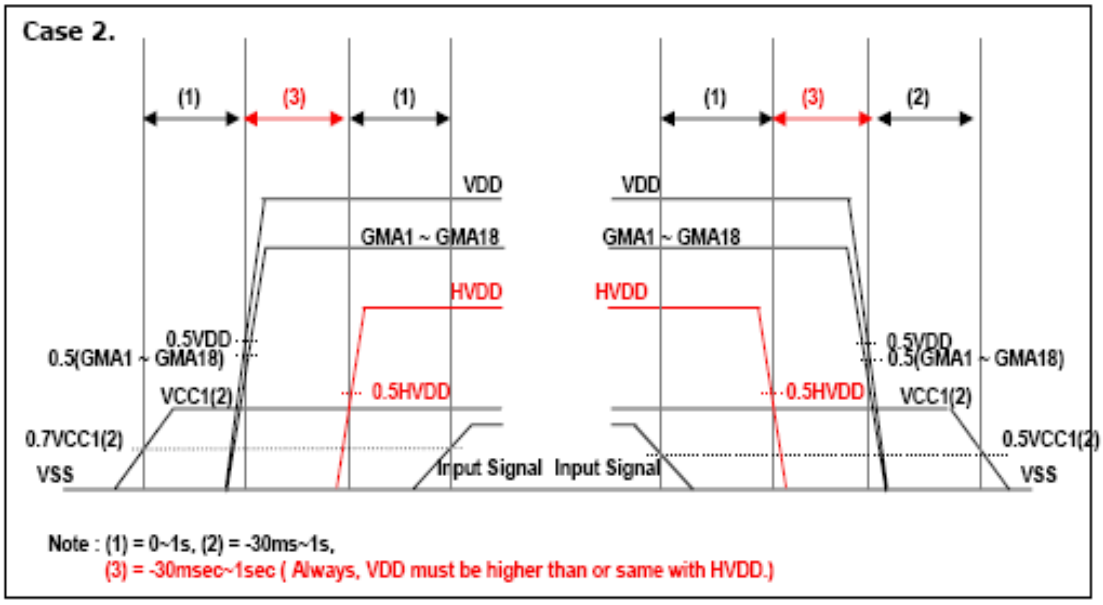
Circuit Block Diagram of LVDS Format Selection pin



APPENDIX- IV

■ Source D-IC Power Sequence





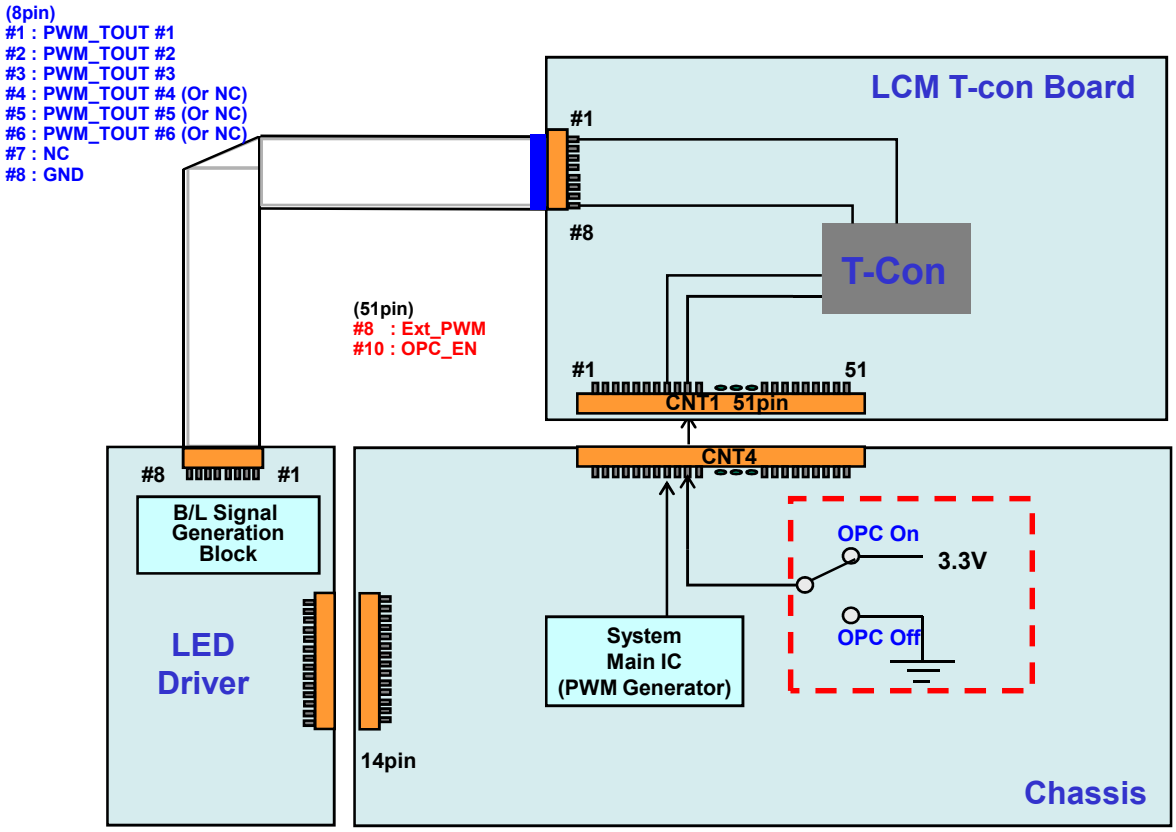
- Input Signal : SOE,POL,GSP,H_CONV,OPT_N, mini-LVDS

APPENDIX- VI

■ Scanning and OPC Design Guide

◇ When OPC Enable is “L", OPC Output = System Dimming.

OPC Output(PWM Signal) is synchronized with V-Sync Freq. of System in T-Con Board.



<With Driver Model>

◇ PWM Specification (VDD = 3.3V) @ OPC

1. PWM High Voltage Range : 2.5V~3.6V
2. PWM Low Voltage Range : 0.0V~0.8V

EXTVBR-B Frequency	50 Hz for PAL 60 Hz for NTSC
Rising Time	MAX 10.0 μs
Falling Time	MAX 10.0 μs