



LC420EUG

Product Specification

SPECIFICATION FOR APPROVAL

- () Preliminary Specification
 (●) Final Specification

Title	42.0" WUXGA TFT LCD
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BUYER	LGE
MODEL	

SUPPLIER	LG.Display Co., Ltd.
*MODEL	LC420EUG
SUFFIX	SCA1 (RoHS Verified)

*When you obtain standard approval,
please use the above model name without suffix

APPROVED BY	SIGNATURE DATE
/	_____
/	_____
/	_____

Please return 1 copy for your confirmation with your signature and comments.

APPROVED BY	SIGNATURE DATE
P.Y. Kim / Team Leader	_____
REVIEWED BY	
S.J. Cho / Project Leader	_____
PREPARED BY	
J.H. Oh / Engineer	_____

**TV Products Development Dept.
LG. Display LCD Co., Ltd**

LC420EUG

Product Specification

CONTENTS

Number	ITEM	Page
	COVER	0
	CONTENTS	1
	RECORD OF REVISIONS	2
1	GENERAL DESCRIPTION	3
2	ABSOLUTE MAXIMUM RATINGS	4
3	ELECTRICAL SPECIFICATIONS	5
3-1	ELECTRICAL CHARACTERISTICS	5
3-2	INTERFACE CONNECTIONS	8
3-3	SIGNAL TIMING SPECIFICATIONS	11
3-4	DATA MAPPING AND TIMING	14
3-5	PANEL PIXEL STRUCTURE	15
3-6	POWER SEQUENCE	16
4	OPTICAL SPECIFICATIONS	17
5	MECHANICAL CHARACTERISTICS	21
6	RELIABILITY	24
7	INTERNATIONAL STANDARDS	25
7-1	SAFETY	25
7-2	Environment	25
8	PACKING	26
8-1	DESIGNATION OF LOT MARK	26
8-2	PACKING FORM	26
9	PRECAUTIONS	27
9-1	MOUNTING PRECAUTIONS	27
9-2	OPERATING PRECAUTIONS	27
9-3	ELECTROSTATIC DISCHARGE CONTROL	28
9-4	PRECAUTIONS FOR STRONG LIGHT EXPOSURE	28
9-5	STORAGE	28
9-6	HANDLING PRECAUTIONS FOR PROTECTION FILM	28

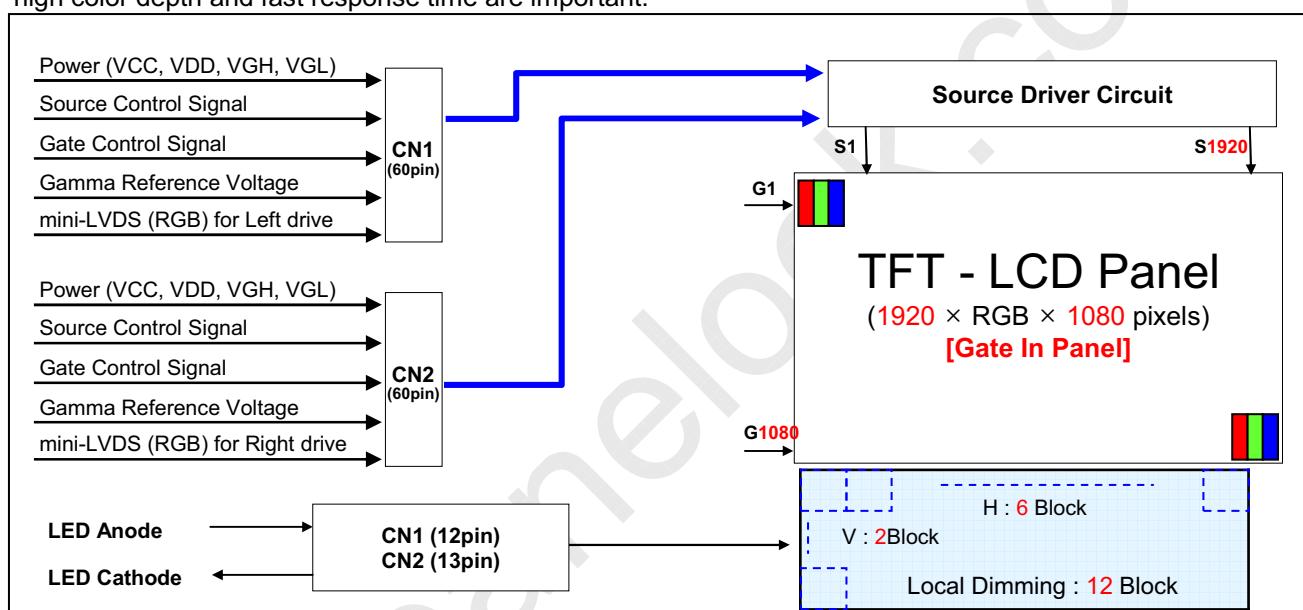
LC420EUG

Product Specification

1. General Description

The LC420EUG is a Color Active Matrix Liquid Crystal Display with an integral Light Emitting Diode (LED) backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally black mode. It has a 42.02 inch diagonally measured active display area with WUXGA resolution (1080 vertical by 1920 horizontal pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the luminance of the sub-pixel color is determined with a 8-bit gray scale signal for each dot. Therefore, it can present a palette of more than 16.7M(true) colors.

It is intended to support LCD TV, PCTV where high brightness, super wide viewing angle, high color gamut, high color depth and fast response time are important.



General Features

Active Screen Size	42.02 inches(1067.31mm) diagonal
Outline Dimension	973.2(H) x 566.2 (V) x 10.8 mm(B)/25.3(D) (Typ.)
Pixel Pitch	0.4845 mm x 0.4845 mm
Pixel Format	1920 horiz. by 1080 vert. Pixels, RGB stripe arrangement
Color Depth	8-bit, 16.7 M colors (* 1.06B colors @ 10 bit (D) System Output)
Drive IC Data Interface	Source D-IC : 8-bit mini-LVDS, gamma reference voltage, and control signals Gate D-IC : Gate In Panel
Luminance, White	450 cd/m ² (Center 1point ,Typ.)
Viewing Angle (CR>10)	Viewing angle free (R/L 178 (Min.), U/D 178 (Min.))
Power Consumption	Total 95.8 W (Typ.) (Logic=7.8 W with T-CON, LED Backlight =88W @ with Driver)
Weight	11.1Kg (Typ.)
Display Mode	Transmissive mode, Normally black
Surface Treatment	Hard coating (3H), Anti-glare treatment of the front polarizer (Haze 10%)

LC420EUG

Product Specification

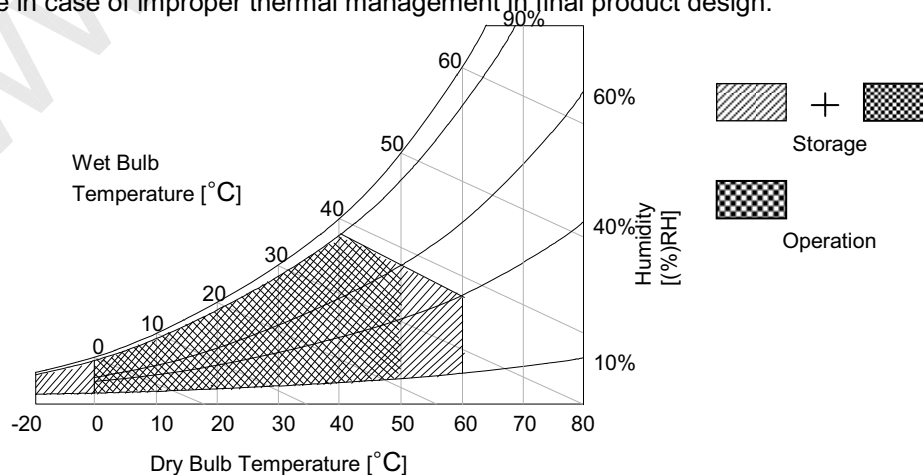
2. Absolute Maximum Ratings

The following items are maximum values which, if exceeded, may cause faulty operation or damage to the LCD module.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value		Unit	Note
		Min	Max		
Logic Power Voltage	VCC	-0.5	+4.0	V _{DC}	1
Gate High Voltage	VGH	+18.0	+30.0	V _{DC}	
Gate Low Voltage	VGL	-8.0	-4.0	V _{DC}	
Source D-IC Analog Voltage	VDD	-0.3	+18.0	V _{DC}	
Gamma Ref. Voltage (Upper)	VGMH	½VDD-0.5	VDD+0.5	V _{DC}	
Gamma Ref. Voltage (Low)	VGML	-0.3	½ VDD+0.5	V _{DC}	
LED Input Voltage	Vf	-	+180.0	V _{DC}	4
Panel Front Temperature	TSUR	-	+68	°C	
Operating Temperature	TOP	0	+50	°C	2,3
Storage Temperature	TST	-20	+60	°C	
Operating Ambient Humidity	HO _P	10	90	%RH	
Storage Humidity	HST	10	90	%RH	

- Note:
1. Ambient temperature condition ($T_a = 25 \pm 2 \text{ }^\circ\text{C}$)
 2. Temperature and relative humidity range are shown in the figure below. Wet bulb temperature should be Max 39 °C and no condensation of water.
 3. Gravity mura can be guaranteed below 40 °C condition.
 4. The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 68 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 68 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.



Product Specification

3. Electrical Specifications

3-1. Electrical Characteristics

It requires several power inputs. The VCC is the basic power of LCD Driving power sequence, Which is used to logic power voltage of Source D-IC and GIP.

Table 2. ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Note
Logic Power Voltage	VCC	-	3.0	3.3	3.6	VDC	
Logic High Level Input Voltage	V _{IH}		2.7		VCC	VDC	
Logic Low Level Input Voltage	V _{IL}		0		0.6	VDC	
Source D-IC Analog Voltage	VDD	-	16.05	16.25	16.45	VDC	
Half Source D-IC Analog Voltage	H_VDD	-	7.89	8.0	8.31	VDC	
Gamma Reference Voltage	V _{GMH}	(GMA1 ~ GMA9)	½*VDD		VDD-0.2		
	V _{GML}	(GMA10 ~ GMA18)	0.2		½*VDD		
Common Voltage	V _{com}	Normal	6.71	7.01	7.31	V	
		Reverse	6.71	7.01	7.31	V	
Mini-LVDS Clock frequency	CLK	3.0V≤VCC≤3.6V			156	MHz	
mini-LVDS input Voltage (Center)	V _{IB}	Mini-LVDS Clock and Data	0.7 + (VID/2)		(VCC-1.2) - VID / 2	V	5
mini-LVDS input Voltage Distortion (Center)	ΔV _{IB}				0.8	V	
mini-LVDS differential Voltage range	V _{ID}		150		800	mV	
mini-LVDS differential Voltage range Dip	ΔV _{ID}		25		800	mV	
Gate High Voltage	V _{GH}		@ 25°C	27.39	27.69	27.99	
		@ 0°C	28.85	29.15	29.45	VDC	
Gate Low Voltage	V _{GL}		-5.5	-5.3	-5.1	VDC	
GIP Bi-Scan Voltage	V _{GI_P} V _{GI_N}	-	V _{GL}	-	V _{GH}	VDC	
GIP Refresh Voltage	V _{GH} even/odd	-	V _{GL}	-	V _{GH}	V	
GIP Start Pulse Voltage	V _{ST}	-	V _{GL}	-	V _{GH}	V	
GIP Operating Clock	GCLK	-	V _{GL}	-	V _{GH}	V	
Total Power Current	I _{LCD}	-		815	938	mA	2
Total Power Consumption	P _{LCD}	-		9.78	11.25	Watt	2

- Note: 1. The specified current and power consumption are under the V_{LCD}=12V., 25 ± 2°C, f_v=120Hz condition whereas mosaic pattern(8 x 6) is displayed and f_v is the frame frequency.
2. The above spec is based on the basic model.
3. All of the typical gate voltage should be controlled within 1% voltage level
4. Ripple voltage level is recommended under 10%
5. In case of mini-LVDS signal spec, refer to Fig 2 for the more detail.
6. Logic Level Input Signal : SOE,POL,GSP,H_CONV,OPT_N
7. HVDD Voltage level is half of VDD and it should be between Gamma9 and Gamma10.

LC420EUG

Product Specification

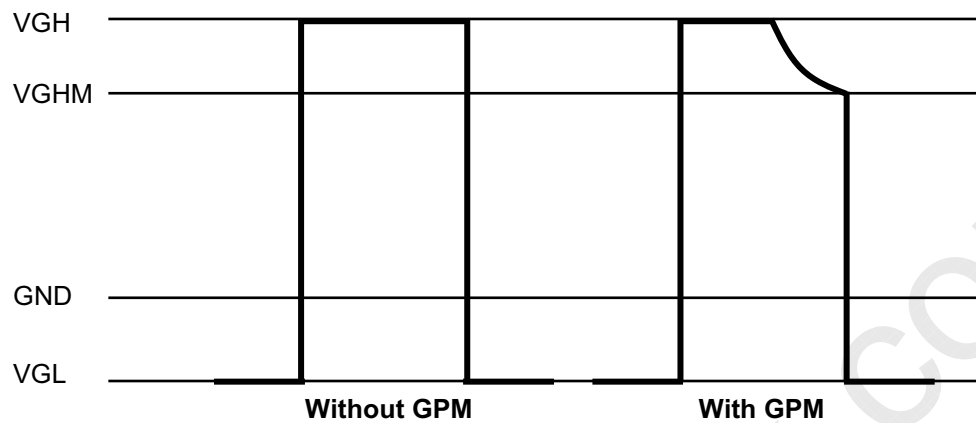
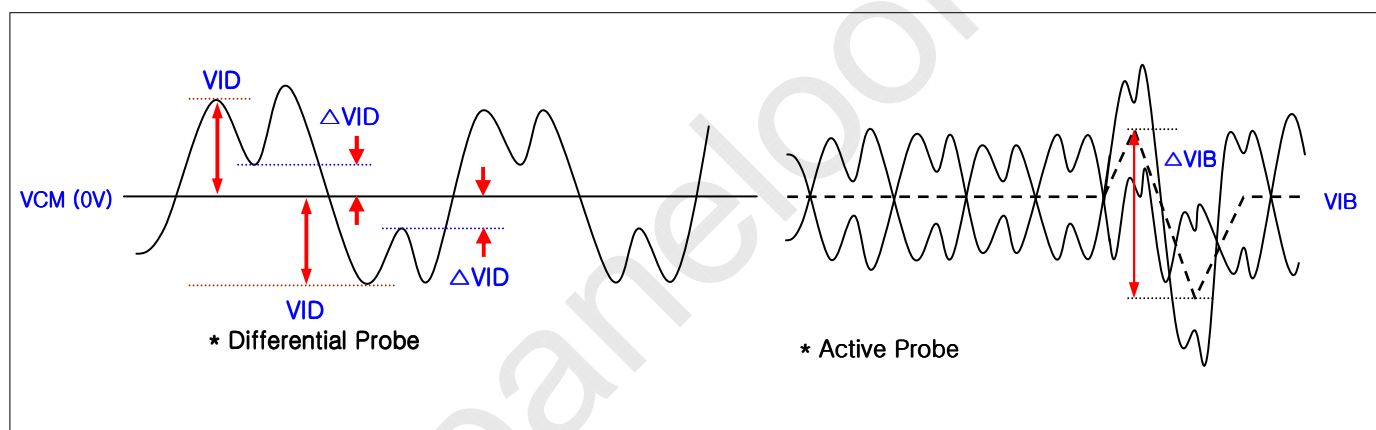


FIG. 1 Gate Output Wave form without GPM and with GPM

FIG. 2 Description of VID, Δ VIB, Δ VID

* Source PCB

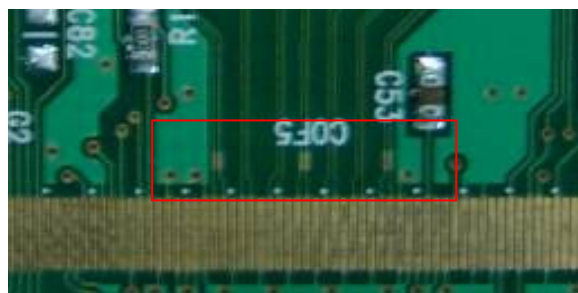


FIG. 3 Measure point

Product Specification

Table 3. ELECTRICAL CHARACTERISTICS (Continue)

Parameter	Symbol	Values			Unit	Note	
		Min	Typ	Max			
Backlight Assembly :							
Forward Current (one array)	Anode	$I_{F (anode)}$		165		mAdc	±5%
	Cathode	$I_{F (cathode)}$	52.25	55	57.75	mAdc	2, 3
Forward Voltage		V_F	110.2	117.8	125.4	Vdc	4
Forward Voltage Variation		ΔV_F			1.7	Vdc	5
Power Consumption		P_{BL}	72.7	77.8	82.7	W	6
Burst Dimming Duty		On duty	1		100	%	
Burst Dimming Frequency		1/T	95		182	Hz	8
LED Array : (APPENDIX-III)							
Life Time			30,000	50,000		Hrs	7

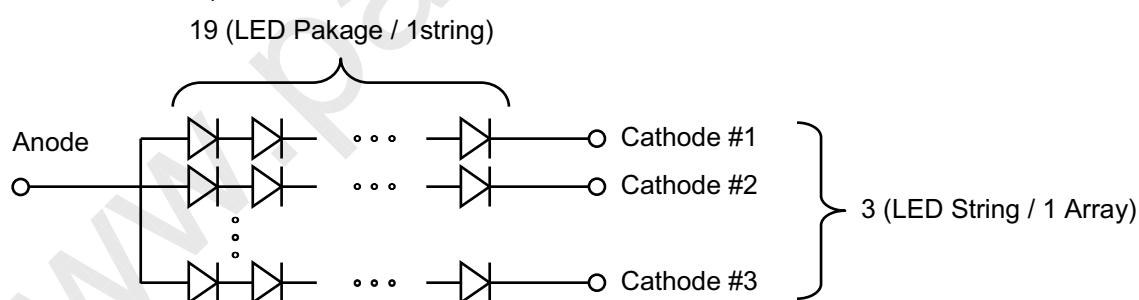
Notes :The design of the LED driver must have specifications for the LED array in LCD Assembly.

The electrical characteristics of LED driver are based on Constant Current driving type.

The performance of the LED in LCM, for example life time or brightness, is extremely influenced by the characteristics of the LED Driver. So, all the parameters of an LED driver should be carefully designed.

When you design or order the LED driver, please make sure unwanted lighting caused by the mismatch of the LED and the driver (no lighting, flicker, etc) has never been occurred. When you confirm it, the LCD-Assembly should be operated in the same condition as installed in your instrument.

1. Electrical characteristics are based on LED Array specification.
2. Specified values are defined for a Backlight Assembly. (IBL : 4 LED array, 165mA/LED array)
3. Each LED array has one anode terminal and three cathode terminals.
The forward current(I_F) of the anode terminal is 165mA and it supplies 55mA into three strings, respectively



4. The forward voltage(V_F) of LED array depends on ambient temperature (Appendix-III)
5. ΔV_F means Max V_F -Min V_F in one Backlight. So V_F variation in a Backlight isn't over Max. 1.7V
6. Maximum level of power consumption is measured at initial turn on.
Typical level of power consumption is measured after 1hrs aging at $25 \pm 2^\circ\text{C}$.
7. The life time(MTTF) is determined as the time at which brightness of the LED is 50% compared to that of initial value at the typical LED current on condition of continuous operating at $25 \pm 2^\circ\text{C}$, based on duty 100%.
8. The reference method of burst dimming duty ratio.
It is recommended to use synchronous V-sync frequency to prevent waterfall
(Vsync x 1 =Burst Frequency)
Though PWM frequency is over 182Hz (max252Hz), function of backlight is not affected.

LC420EUG

Product Specification

3-2. Interface Connections

This LCD module employs two kinds of interface connection, two 60-pin FFC connector are used for the module electronics and 12-pin,13-pin connectors are used for the integral backlight system.

3-2-1. LCD Module

-LCD Connector (CN1): **TF06L-60S-0.5SF** (Manufactured by **HRS**) or Equivalent

Table 4-1. MODULE CONNECTOR(CN1) PIN CONFIGURATION

No	Symbol	Description	No	Symbol	Description
1	GND	Ground	31	LLV3 -	Left Mini LVDS Receiver Signal(3-)
2	LTD_OUT	LTD OUTPUT	32	LLV3 +	Left Mini LVDS Receiver Signal(3+)
3	GCLK1	GIP GATE Clock 1	33	LCLK -	Left Mini LVDS Receiver Clock Signal(-)
4	GCLK2	GIP GATE Clock 2	34	LCLK +	Left Mini LVDS Receiver Clock Signal(+)
5	GCLK3	GIP GATE Clock 3	35	LLV2 -	Left Mini LVDS Receiver Signal(2-)
6	GCLK4	GIP GATE Clock 4	36	LLV2 +	Left Mini LVDS Receiver Signal(2+)
7	GCLK5	GIP GATE Clock 5	37	LLV1 -	Left Mini LVDS Receiver Signal(1-)
8	GCLK6	GIP GATE Clock 6	38	LLV1 +	Left Mini LVDS Receiver Signal(1+)
9	VGI_N	GIP Bi-Scan (Normal =VGL Rotate = VGH)	39	LLV0 -	Left Mini LVDS Receiver Signal(0-)
10	VGI_P	GIP Bi-Scan (Normal =VGH Rotate = VGL)	40	LLV0 +	Left Mini LVDS Receiver Signal(0+)
11	VGH_ODD	GIP Panel VDD for Odd GATE TFT	41	GND	Ground
12	VGH_EVEN	GIP Panel VDD for Even GATE TFT	42	SOE	Source Output Enable SIGNAL
13	VGL	GATE Low Voltage	43	POL	Polarity Control Signal
14	VST	VERTICAL START PULSE	44	GSP	GATE Start Pulse
15	GND	Ground	45	H_CONV	"H" H 2dot Inversion/ "L" H 1dot Inversion
16	VCOM_L_FB	VCOM Left Feed-Back Output	46	OPT_N	"H" Normal Display / "L" Rotation Display
17	VCOM_L	VCOM Left Input	47	GND	Ground
18	GND	Ground	48	GMA 18	GAMMA VOLTAGE 18 (Output From LCD)
19	VDD	Driver Power Supply Voltage	49	GMA 16	GAMMA VOLTAGE 16
20	VDD	Driver Power Supply Voltage	50	GMA 15	GAMMA VOLTAGE 15
21	H_VDD	Half Driver Power Supply Voltage	51	GMA 14	GAMMA VOLTAGE 14
22	H_VDD	Half Driver Power Supply Voltage	52	GMA 12	GAMMA VOLTAGE 12
23	GND	Ground	53	GMA 10	GAMMA VOLTAGE 10 (Output From LCD)
24	VCC	Logic Power Supply Voltage	54	GMA 9	GAMMA VOLTAGE 9 (Output From LCD)
25	VCC	Logic Power Supply Voltage	55	GMA 7	GAMMA VOLTAGE 7
26	GND	Ground	56	GMA 5	GAMMA VOLTAGE 5
27	LLV5 -	Left Mini LVDS Receiver Signal(5-)	57	GMA 4	GAMMA VOLTAGE 4
28	LLV5 +	Left Mini LVDS Receiver Signal(5+)	58	GMA 3	GAMMA VOLTAGE 3
29	LLV4 -	Left Mini LVDS Receiver Signal(4-)	59	GMA 1	GAMMA VOLTAGE 1(Output From LCD)
30	LLV4 +	Left Mini LVDS Receiver Signal(4+)	60	GND	Ground

- Note :
1. Please refer to application note for details.
(GIP & Half VDD & Gamma Voltage & H_CONV setting)
 2. These 'input signal' (OPT_N,H_CONV) should be connected

LC420EUG

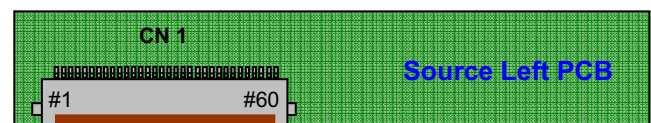
Product Specification

-LCD Connector (CN2): **TF06L-60S-0.5SF**(Manufactured by **HRS**) or Equivalent

Table 4-2. MODULE CONNECTOR(CN2) PIN CONFIGURATION

No	Symbol	Description	No	Symbol	Description
1	GND	Ground	31	RLV1 -	Right Mini LVDS Receiver Signal(1-)
2	GMA 1	GAMMA VOLTAGE 1 (Output From LCD)	32	RLV1 +	Right Mini LVDS Receiver Signal(1+)
3	GMA 3	GAMMA VOLTAGE 3	33	RLV0 -	Right Mini LVDS Receiver Signal(0-)
4	GMA 4	GAMMA VOLTAGE 4	34	RLV0 +	Right Mini LVDS Receiver Signal(0+)
5	GMA 5	GAMMA VOLTAGE 5	35	GND	Ground
6	GMA 7	GAMMA VOLTAGE 7	36	VCC	Logic Power Supply Voltage
7	GMA 9	GAMMA VOLTAGE 9 (Output From LCD)	37	VCC	Logic Power Supply Voltage
8	GMA 10	GAMMA VOLTAGE 10 (Output From LCD)	38	GND	Ground
9	GMA 12	GAMMA VOLTAGE 12	39	H_VDD	Half Driver Power Supply Voltage
10	GMA 14	GAMMA VOLTAGE 14	40	H_VDD	Half Driver Power Supply Voltage
11	GMA 15	GAMMA VOLTAGE 15	41	VDD	Driver Power Supply Voltage
12	GMA 16	GAMMA VOLTAGE 16	42	VDD	Driver Power Supply Voltage
13	GMA 18	GAMMA VOLTAGE 18 (Output From LCD)	43	GND	Ground
14	GND	Ground	44	VCOM_R	VCOM Right Input
15	OPT_N	"H" Normal Display / "L" Rotation Display	45	VCOM_R_FB	VCOM Right Feed-Back Output
16	H_CONV	"H" H 2dot Inversion/ "L" H 1dot Inversion	46	GND	Ground
17	GSP	GATE Start Pulse	47	VST	VERTICAL START PULSE
18	POL	Polarity Control Signal	48	VGL	GATE Low Voltage
19	SOE	Source Output Enable SIGNAL	49	VGH_EVEN	GIP Panel VDD for Even GATE TFT
20	GND	Ground	50	VGH_ODD	GIP Panel VDD for Odd GATE TFT
21	RLV5 -	Right Mini LVDS Receiver Signal(5-)	51	VGI_P	GIP Bi-Scan (Normal =VGH Rotate = VGL)
22	RLV5 +	Right Mini LVDS Receiver Signal(5+)	52	VGI_N	GIP Bi-Scan (Normal =VGL Rotate = VGH)
23	RLV4 -	Right Mini LVDS Receiver Signal(4-)	53	GCLK6	GIP GATE Clock 6
24	RLV4 +	Right Mini LVDS Receiver Signal(4+)	54	GCLK5	GIP GATE Clock 5
25	RLV3 -	Right Mini LVDS Receiver Signal(3-)	55	GCLK4	GIP GATE Clock 4
26	RLV3 +	Right Mini LVDS Receiver Signal(3+)	56	GCLK3	GIP GATE Clock 3
27	RCLK -	Right Mini LVDS Receiver Clock Signal(-)	57	GCLK2	GIP GATE Clock 2
28	RCLK +	Right Mini LVDS Receiver Clock Signal(+)	58	GCLK1	GIP GATE Clock 1
29	RLV2 -	Right Mini LVDS Receiver Signal(2-)	59	LTD_OUT	LTD OUTPUT
30	RLV2 +	Right Mini LVDS Receiver Signal(2+)	60	GND	Ground

- Note :
1. Please refer to application note for details
(**GIP & Half VDD & Gamma Voltage & H_CONV setting**)
 2. These 'input signal' (OPT_N,H_CONV) should be connected



LC420EUG

Product Specification

3-2-2. Backlight Module

[CN1]

1) LED Array assy Connector (Plug)

: 20010HS-12 (manufactured by Yeonho) or equivalent

2) Mating Connector (Receptacle)

: 20010WR-12B1 (manufactured by Yeonho) or equivalent

[CN2]

1) LED Array assy Connector (Plug)

: 20010HS-13 (manufactured by Yeonho) or equivalent

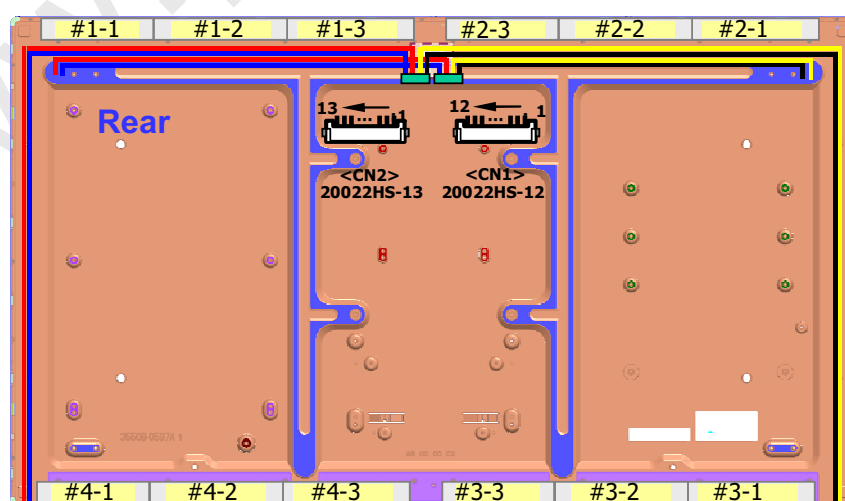
2) Mating Connector (Receptacle)

: 20010WR-13B1 (manufactured by Yeonho) or equivalent

Table 5. BACKLIGHT CONNECTOR PIN CONFIGURATION(CN1,CN2)

No	Symbol	Description	Note	No	Symbol	Description	Note
1	#1 Anode	LED Input Current		1	#3 Anode	LED Input Current	
2	N.C	Open		2	N.C	Open	
3	#1-1 Cathode	LED Output Current		3	#3-1 Cathode	LED Output Current	
4	#1-2 Cathode	LED Output Current		4	#3-2 Cathode	LED Output Current	
5	#1-3 Cathode	LED Output Current		5	#3-3 Cathode	LED Output Current	
6	N.C	Open		6	N.C	Open	
7	N.C	Open		7	N.C	Open	
8	#2-3Cathode	LED Output Current		8	N.C	Open	
9	#2-2 Cathode	LED Output Current		9	#4-3Cathode	LED Output Current	
10	#2-1 Cathode	LED Output Current		10	#4-2 Cathode	LED Output Current	
11	N.C	Open		11	#4-1 Cathode	LED Output Current	
12	#2 Anode	LED Input Current		12	N.C	Open	
				13	#4 Anode	LED Input Current	

◆ Rear view of LCM



Product Specification

3-3. Signal Timing Specifications

Table 6. Timing Requirements

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Mini Clock pulse period	T1		6.4	6.7		ns	1
Mini Clock pulse low period	T2		3.2	-	-	ns	
Mini Clock pulse high period	T3		3.2	-	-	ns	
Mini Data setup time	T6		1.2	-	-	ns	
Mini Data hold time	T7		1.2	-	-	ns	
Reset low to SOE rising time	T8		0	-	-	ns	
SOE to Reset input time	T9		200	-	-	ns	
Receiver off to SOE timing	T10		10	-	-	CLK cycle	
POL signal to SOE setup time	T11		-5	-	-	ns	
POL signal to SOE hold time	T12		6	-	-	ns	
Reset High Period	T13		3			CLK cycle	
SOE signal GSP setup time	T14		100			ns	
SOE signal GSP Hold time	T15		100			ns	
SOE signal Pulse Width	T16		200			ns	

- Note :
1. Mini-LVDS timing measure conditions
: 126MHz < Clock Frequency < 156MHz , 150mV < VID < 800mV @ 3.0<VCC<3.3
 2. Setup time and hold time Should be satisfied at the same time

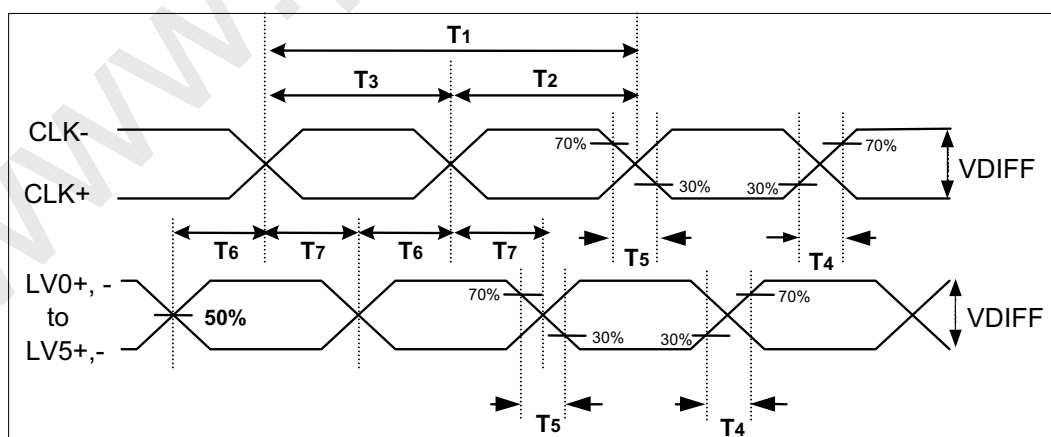


FIG 4. Source D-IC Input Data Latch Timing Waveform

Product Specification

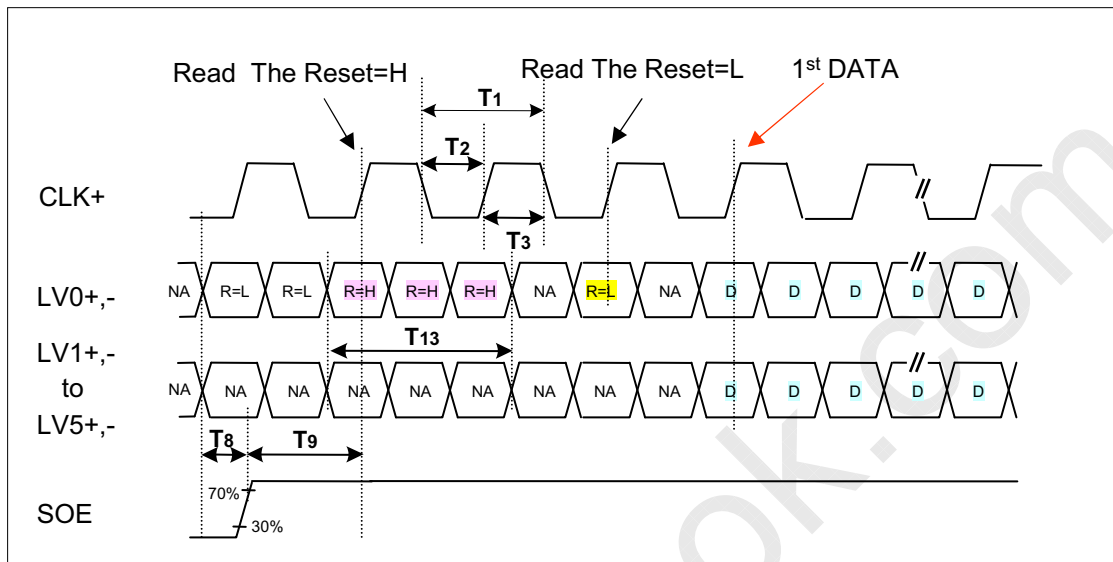


FIG 5-1. Input Data Timing for 1st Source D-IC Chip

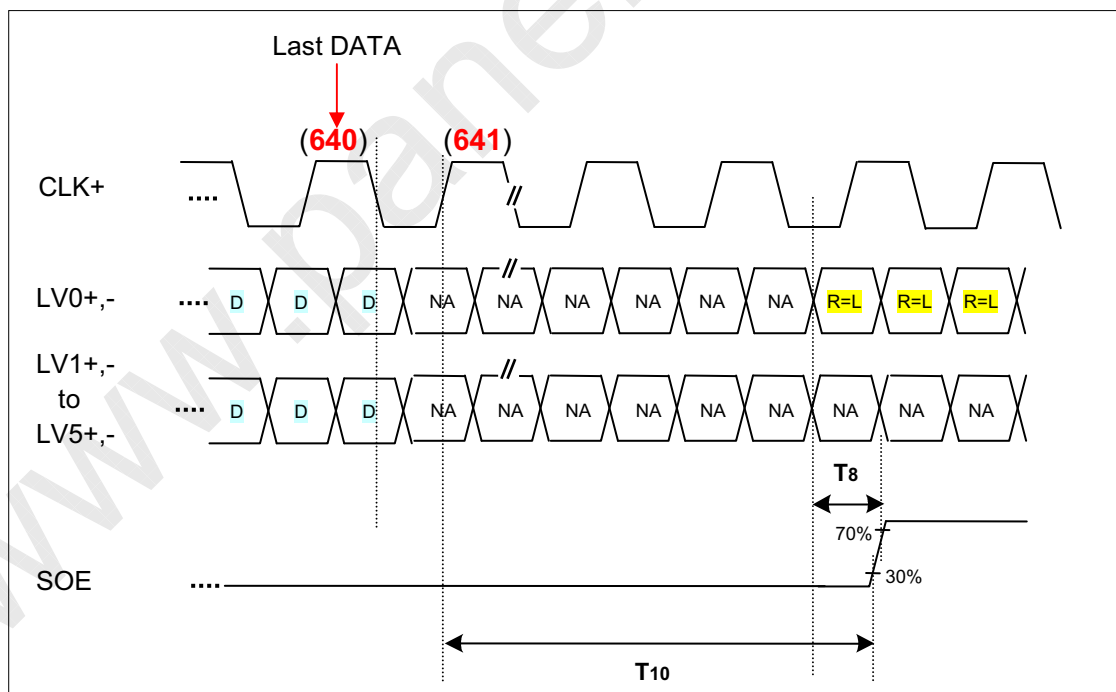


FIG 5-2. Last Data Latch to SOE Timing

Product Specification

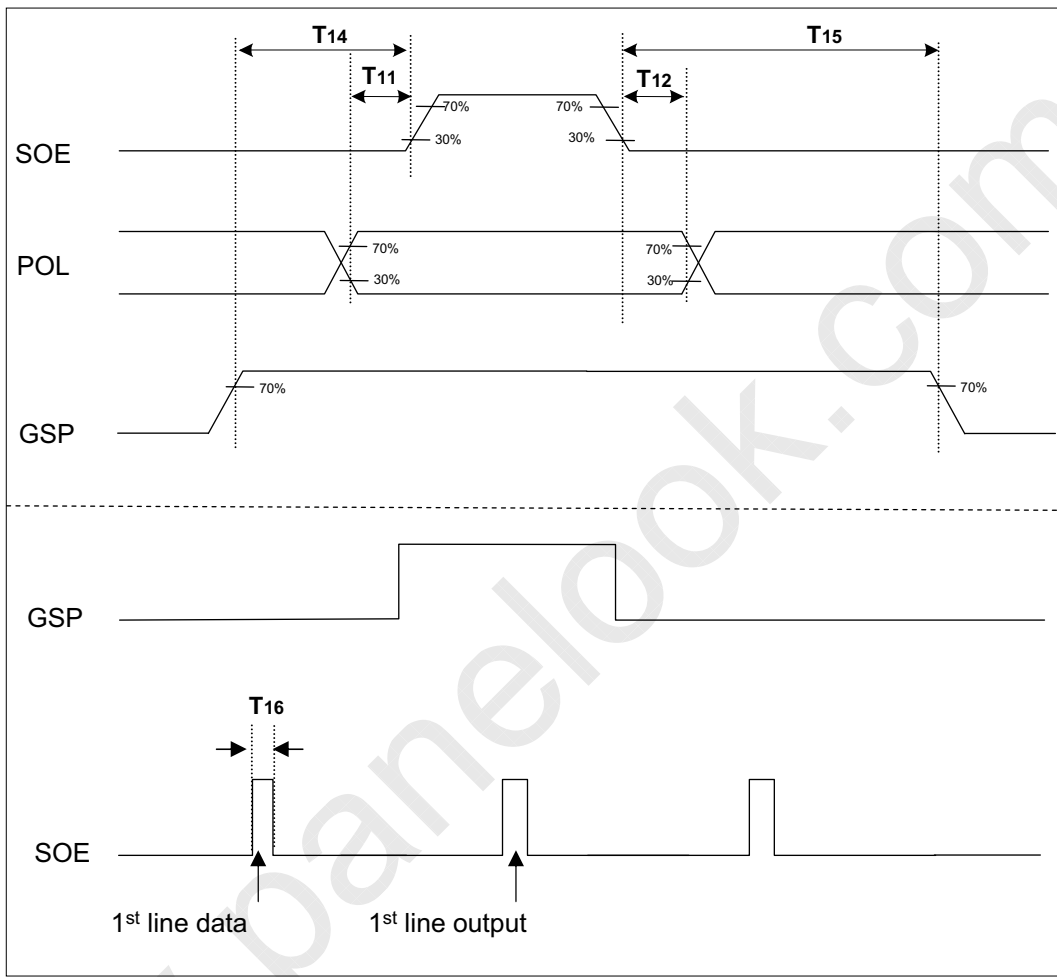
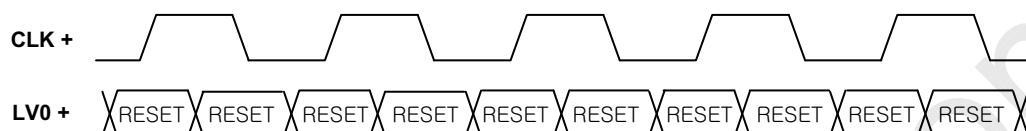
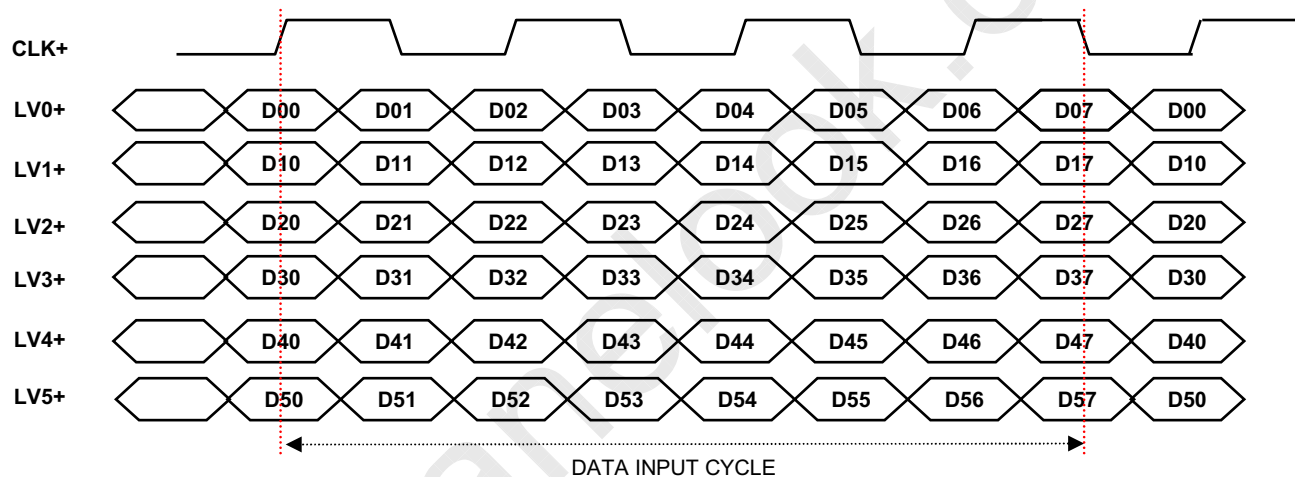


FIG 6. POL, GSP and SOE Timing Waveform

Product Specification

3-4. Data Mapping and Timing

Display data and control signal (RESET) are input to **LV0** to **LV5**.

3-4-1. Control signal input mode**3-4-2. Display data input mode****Fig. 7 Mini-LVDS Data**

Note : 1. For data mapping, please refer to panel pixel structure Fig.8

LC420EUG

Product Specification

3-5. Panel Pixel Structure

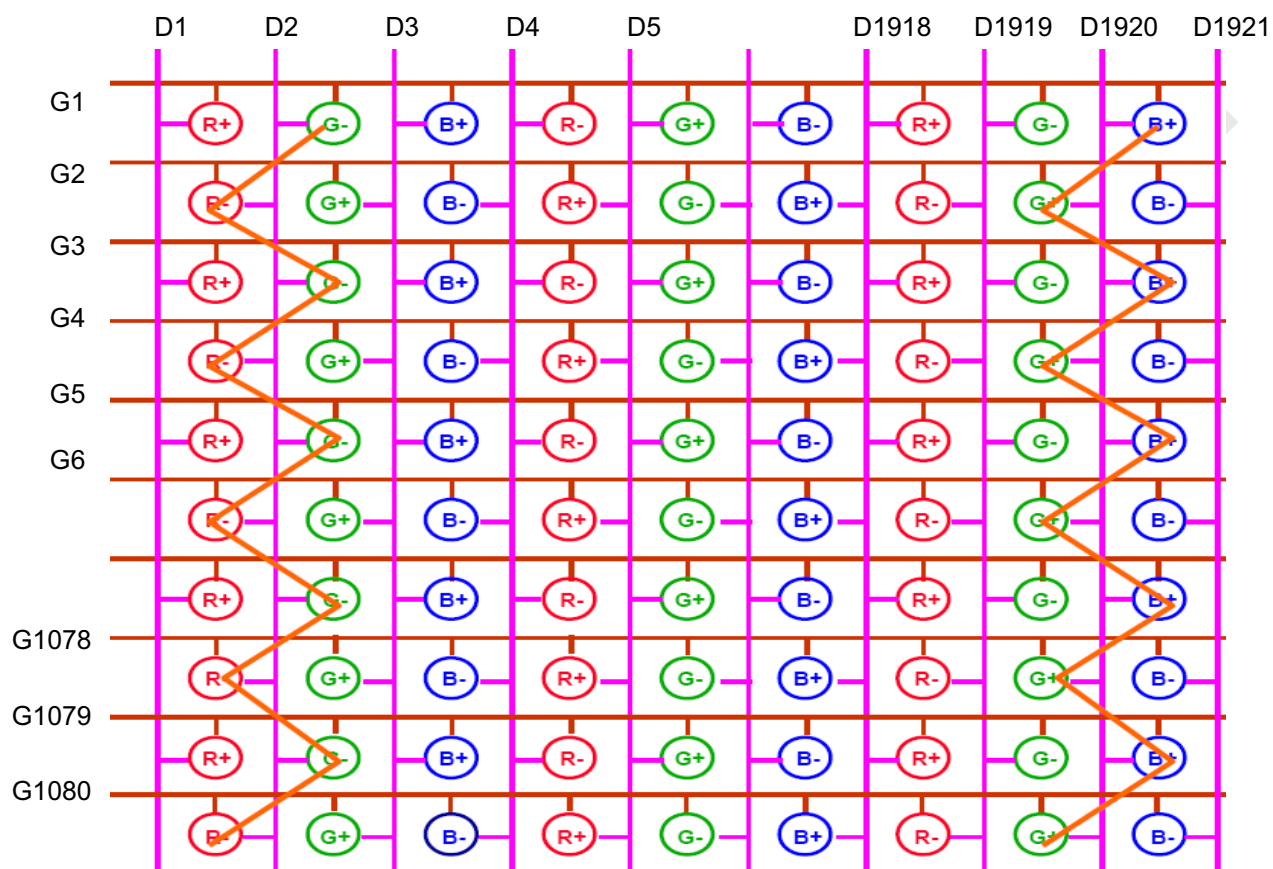


FIG. 8 Panel Pixel Structure

LC420EUG

Product Specification

3-6. Power Sequence

3-6-1. LCD Driving circuit

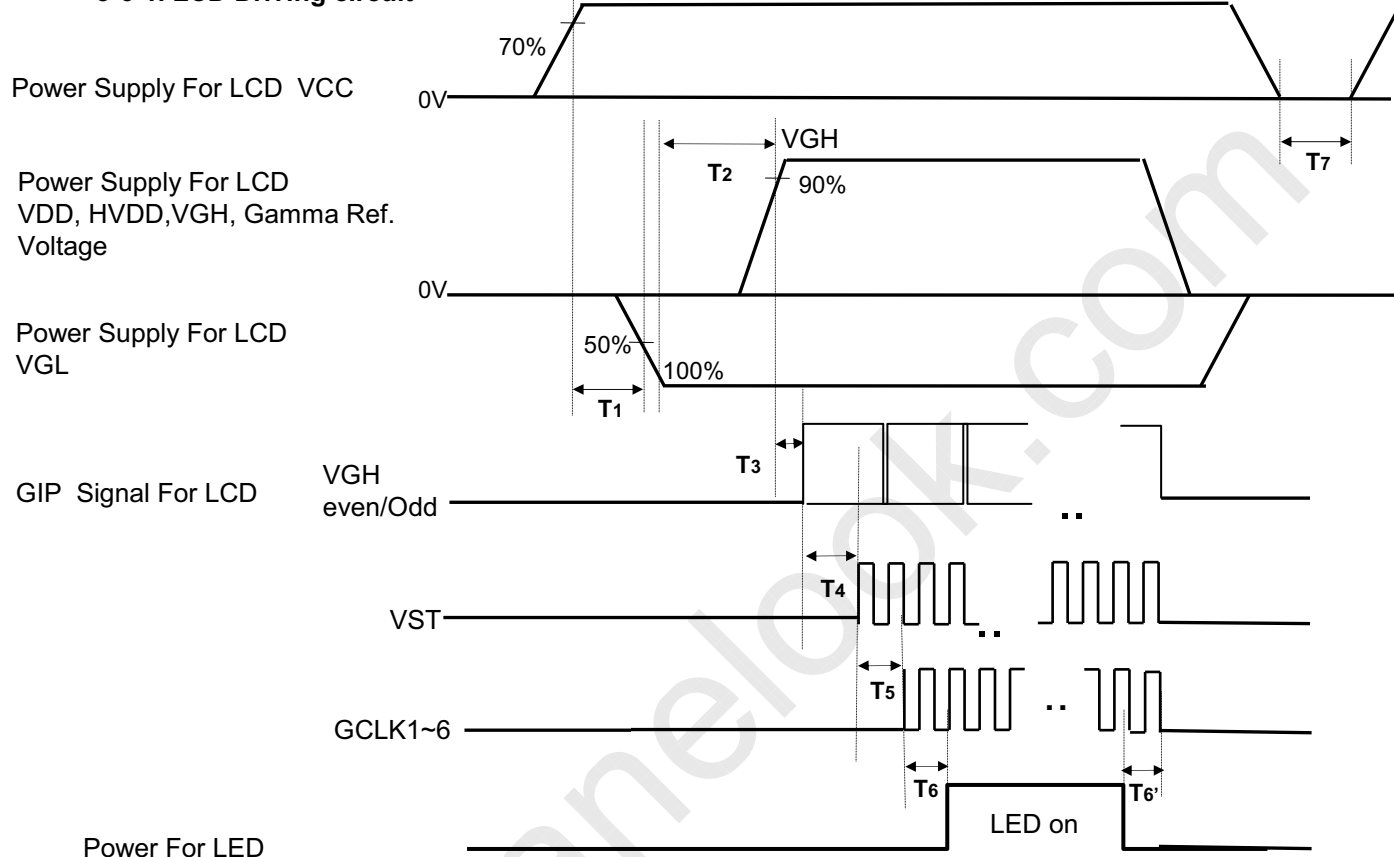


Table 7. POWER SEQUENCE

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	0.5		-	ms	
T2	0.5		-	ms	
T3	0		-	ms	
T4	10		-	ms	2
T5	0		-	ms	
T6 / T6'	20		-	ms	
T7	2		-	sec	

Note : 1. Power sequence for Source D-IC must follow the Case1 & 2.

※ Please refer to Appendix V for more details.

2. VGH Odd signal should be started "High" status and VGH even & odd can not be "High at the same time.
3. Power Off Sequence order is reverse of Power On Condition including Source D-IC.
4. GCLK On/Off Sequence
Normal : GCLK4 → GCLK5 → GCLK6 → GCLK1 → GCLK2 → GCLK3.
Reverse : GCLK3 → GCLK2 → GCLK1 → GCLK6 → GCLK5 → GCLK4.
5. VDD_odd/even transition time should be within V_blank

Product Specification

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable in a dark environment at $25\pm 2^{\circ}\text{C}$. The values are specified at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and θ equal to 0° .

It is presented additional information concerning the measurement equipment and method in FIG. 9.

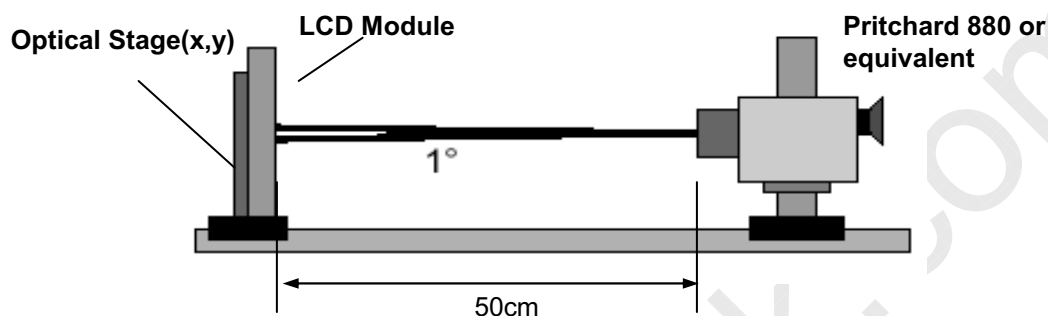


FIG. 9 Optical Characteristic Measurement Equipment and Method

$T_a = 25\pm 2^{\circ}\text{C}$, $V_{DD}, H_V_{DD}, V_{GH}, V_{GL} = \text{typ}$,
 $f_v = 60\text{Hz}$, $\text{Clk} = 148.5\text{MHz}$, $I_f = 165\text{mA}$ (Typ)

Table 8. OPTICAL CHARACTERISTICS

Parameter	Symbol	Value			Unit	Note	
		Min	Typ	Max			
Contrast Ratio	CR	1000	1400	-		1	
Surface Luminance, white	L_{WH}	360	450	-	cd/m ²	2	
Luminance Variation	δ_{WHITE} 5P	-	-	1.3		3	
Response Time	Rising	T_r	-	8	12	ms	4
	Falling	T_f	-	10	14		
Color Coordinates [CIE1931]	RED	R_x	Typ -0.03	0.647	Typ +0.03		
		R_y		0.332			
	GREEN	G_x		0.309			
		G_y		0.601			
	BLUE	B_x		0.149			
		B_y		0.059			
	WHITE	W_x		0.279			
W_y		0.292					
Color Temperature			10,000		K		
Color Gamut			72		%		
Viewing Angle (CR>10)							
	x axis, right($\phi=0^{\circ}$)	θ_r	89	-	-	degree	5
	x axis, left ($\phi=180^{\circ}$)	θ_l	89	-	-		
	y axis, up ($\phi=90^{\circ}$)	θ_u	89	-	-		
	y axis, down ($\phi=270^{\circ}$)	θ_d	89	-	-		
Gray Scale			-	-	-		6

LC420EUG

Product Specification

Note : 1. Contrast Ratio(CR) is defined mathematically as :

$$CR = \frac{\text{Surface Luminance at all white pixels}}{\text{Surface Luminance at all black pixels}}$$

It is measured at center 1-point.

2. Surface luminance is determined after the unit has been 'ON' and 1Hour after lighting the backlight in a dark environment at $25 \pm 2^\circ\text{C}$. Surface luminance is the luminance value at center 1-point across the LCD surface 50cm from the surface with all pixels displaying white. For more information see the FIG. 10.

3. The variation in surface luminance, δ WHITE is defined as :

$$\delta \text{ WHITE}(5P) = \text{Maximum}(L_{on1}, L_{on2}, L_{on3}, L_{on4}, L_{on5}) / \text{Minimum}(L_{on1}, L_{on2}, L_{on3}, L_{on4}, L_{on5})$$

Where L_{on1} to L_{on5} are the luminance with all pixels displaying white at 5 locations .

For more information, see the FIG. 10.

4. Response time is the time required for the display to transit from G(255) to G(0) (Rise Time, Tr_R) and from G(0) to G(255) (Decay Time, Tr_D).

5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD module surface. For more information, see the FIG. 12.

6. Gray scale specification

Gamma Value is approximately 2.2. For more information, see the Table 9.

Table 9. GRAY SCALE SPECIFICATION

Gray Level	Luminance [%] (Typ)
L0	0.07
L15	0.27
L31	1.04
L47	2.49
L63	4.68
L79	7.66
L95	11.5
L111	16.1
L127	21.6
L143	28.1
L159	35.4
L175	43.7
L191	53.0
L207	63.2
L223	74.5
L239	86.7
L255	100

	Gray Level	Gamma Ref.
Positive Voltage	L0	Gamma9
	L1	Gamma8
	L31	Gamma7
	L63	Gamma6
	L127	Gamma5
	L191	Gamma4
	L223	Gamma3
	L255	Gamma1
	Negative Voltage	L255
L223		Gamma16
L191		Gamma15
L127		Gamma14
L63		Gamma13
L31		Gamma12
L1		Gamma11
L0		Gamma10

LC420EUG

Product Specification

Measuring point for surface luminance & luminance variation

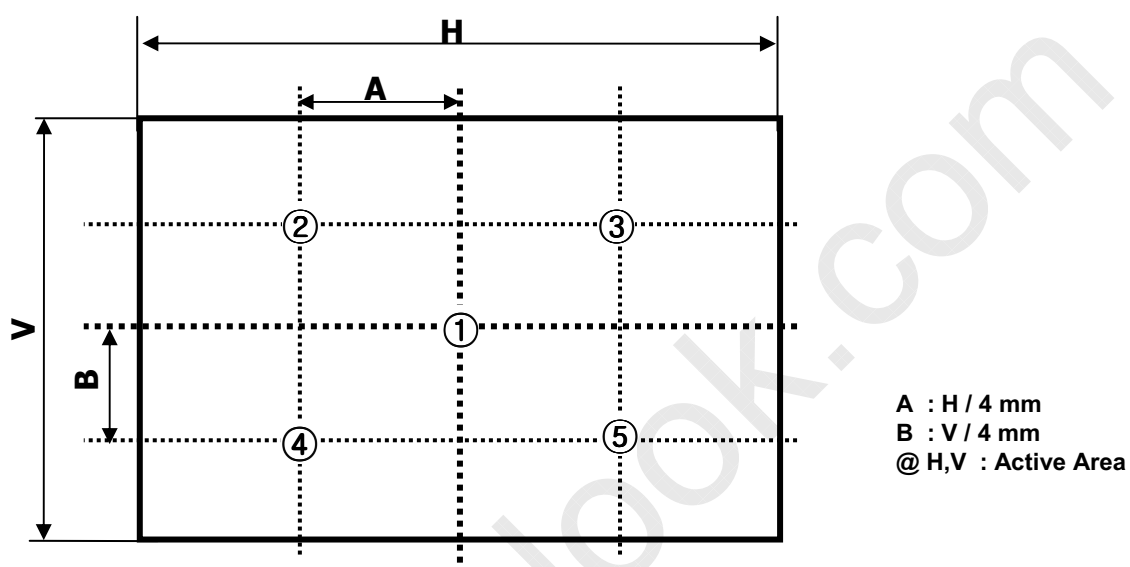


FIG. 10 5 Points for Luminance Measure

Response time is defined as the following figure and shall be measured by switching the input signal for "Gray(N)" and "Gray(M)".

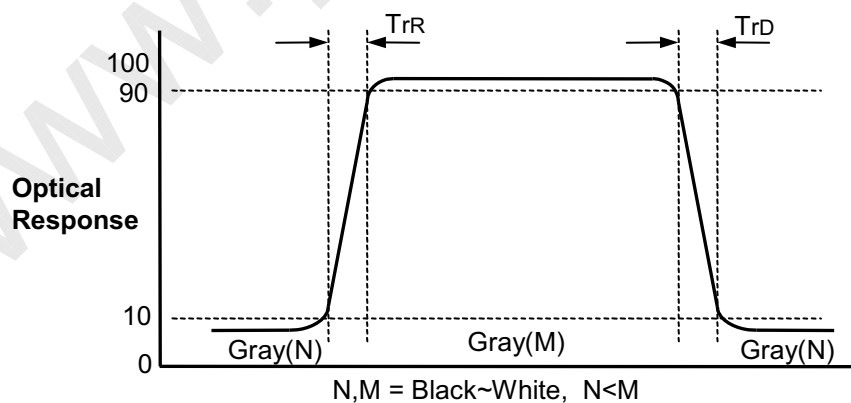


FIG. 11 Response Time

LC420EUG

Product Specification

Dimension of viewing angle range

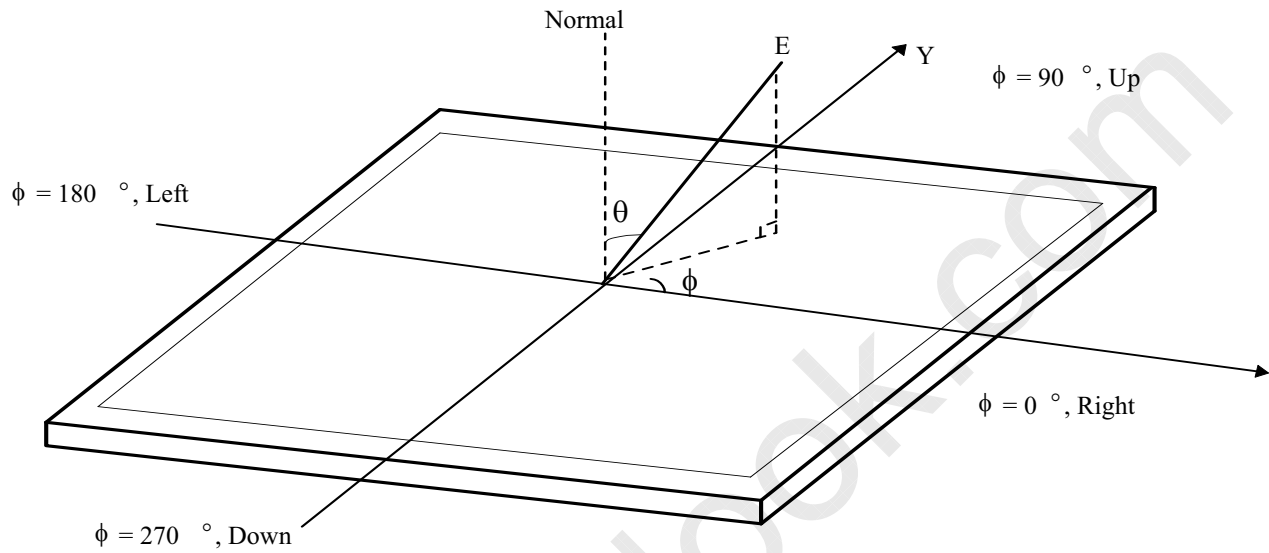


FIG.12 Viewing Angle

LC420EUG

Product Specification

5. Mechanical Characteristics

Table 10 provides general mechanical characteristics.

Table 10. MECHANICAL CHARACTERISTICS

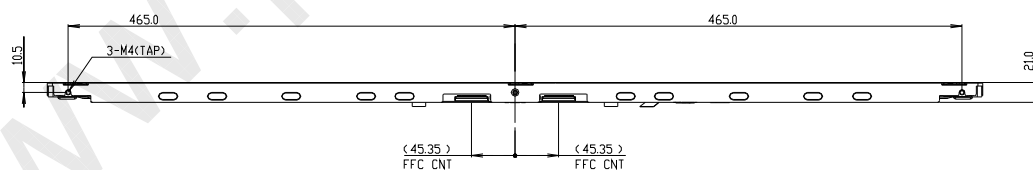
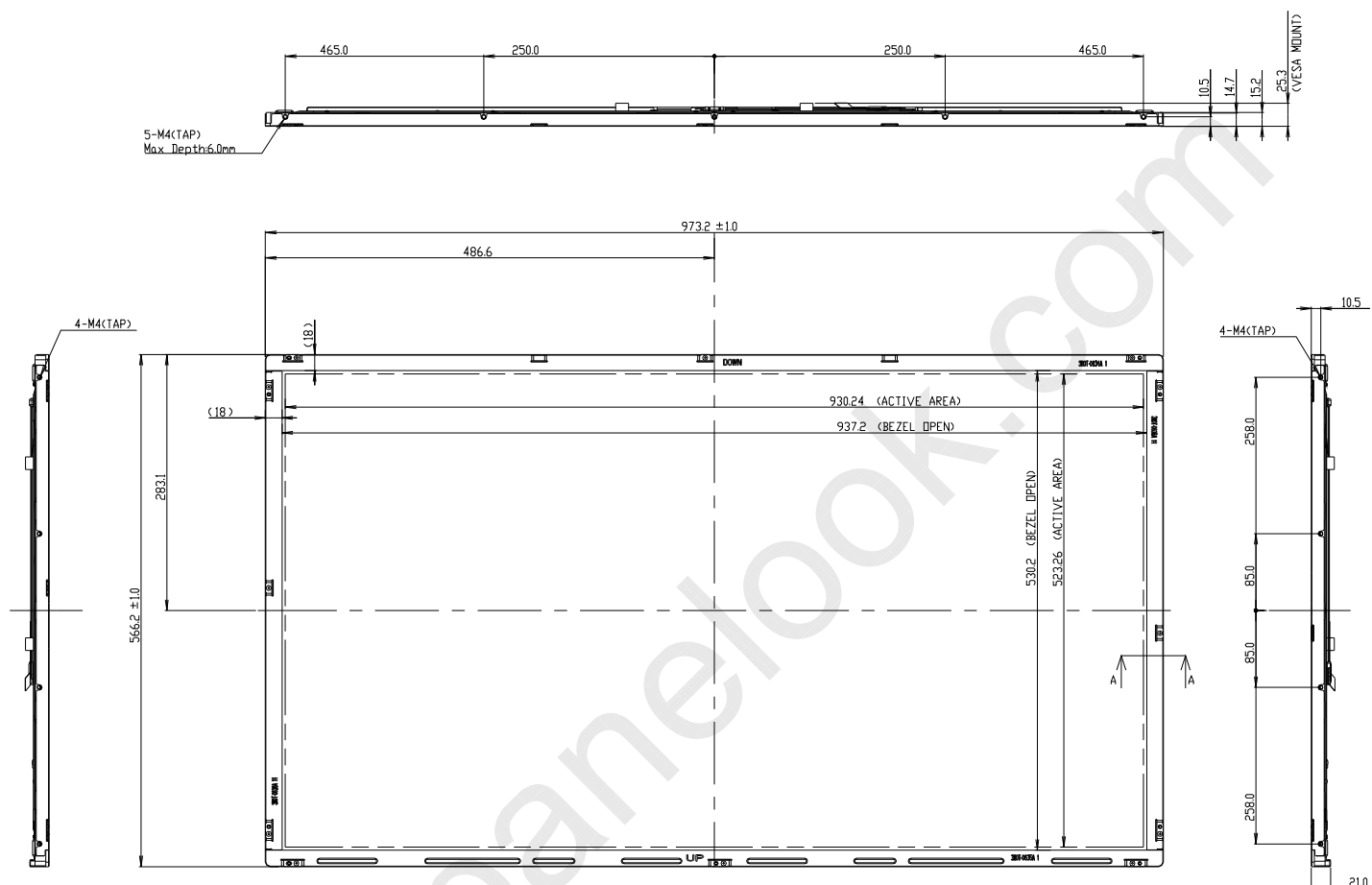
Item	Value	
Outline Dimension	Horizontal	973.2 mm
	Vertical	566.2 mm
	Depth	10.8 mm
Bezel Area	Horizontal	937.2 mm
	Vertical	530.2 mm
Active Display Area	Horizontal	930.24 mm
	Vertical	523.26 mm
Weight	11.1 Kg	

Note : Please refer to a mechanical drawing in terms of tolerance at the next page.

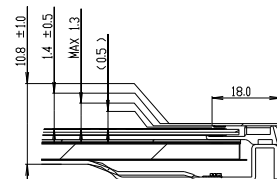
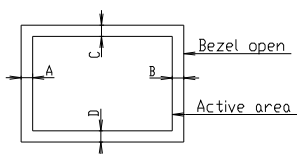
LC420EUG

Product Specification

[FRONT VIEW]



NOTES:
 1. UNSPECIFIED TOLERANCE IS ±1.0MM
 2. TILT AND PARTIAL DISPOSITION TOLERANCE OF DISPLAY AREA AS FOLLOWING.
 (1) Y-DIRECTION: I A-B I ≤ 1.5
 (2) X-DIRECTION: I C-D I ≤ 1.5
 3. M3.0, M4.0 TAP: Max Torque 6kgf.cm

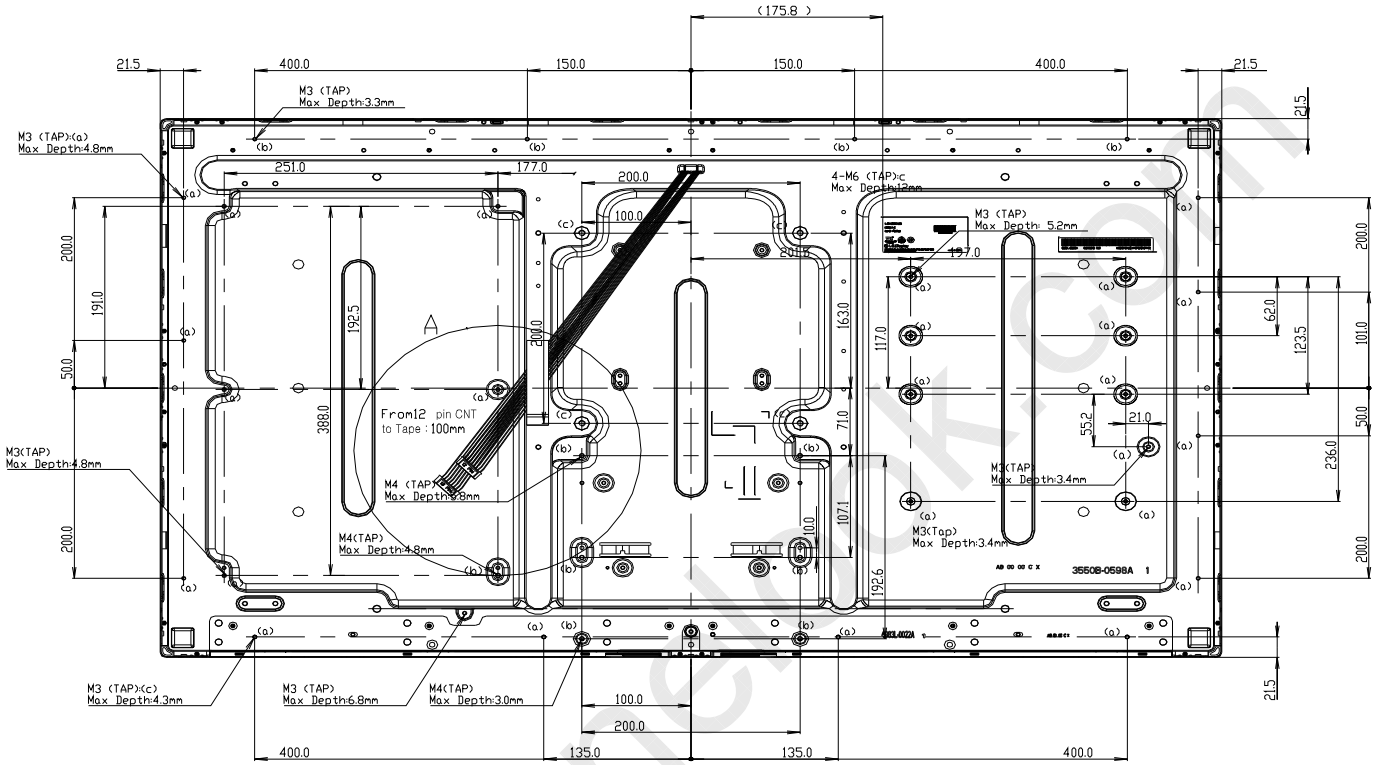


SECTION A-A
SCALE 1/1

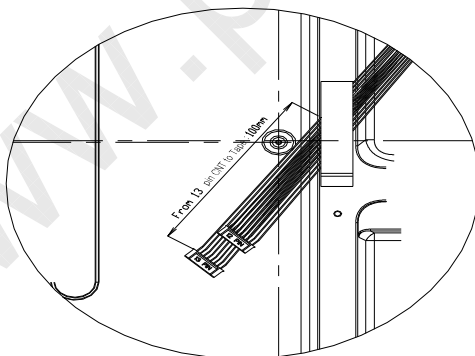
LC420EUG

Product Specification

[REAR VIEW]



Screw (a), M3 Max Torque 6kgf
Screw (b), M4 Max Torque 8kgf



Detail A
Scale 1:1.5

LC420EUG

Product Specification

6. Reliability

Table 11. ENVIRONMENT TEST CONDITION

No.	Test Item	Condition
1	High temperature storage test	Ta= 60°C 240h
2	Low temperature storage test	Ta= -20°C 240h
3	High temperature operation test	Ta= 50°C 50%RH 240h
4	Low temperature operation test	Ta= 0°C 240h
5	Vibration test (non-operating)	Wave form : random Vibration level : 1.0Grms Bandwidth : 10-300Hz Duration : X,Y,Z, 30 min Each direction per 10 min
6	Shock test (non-operating)	Shock level : 50Grms Waveform : half sine wave, 11ms Direction : ±X, ±Y, ±Z One time each direction
7	Humidity condition Operation	Ta= 40 °C ,90%RH
8	Altitude operating storage / shipment	0 - 15,000 ft 0 - 40,000 ft

Note : Before and after Reliability test, LCM should be operated with normal function.

Product Specification

7. International Standards

7-1. Safety

- a) UL 60065, Seventh Edition, Underwriters Laboratories Inc.
Audio, Video and Similar Electronic Apparatus - Safety Requirements.
- b) CAN/CSA C22.2 No.60065:03, Canadian Standards Association.
Audio, Video and Similar Electronic Apparatus - Safety Requirements.
- c) EN 60065:2002 + A11:2008, European Committee for Electrotechnical Standardization (CENELEC).
Audio, Video and Similar Electronic Apparatus - Safety Requirements.
- d) IEC 60065:2005 + A1:2005, The International Electrotechnical Commission (IEC).
Audio, Video and Similar Electronic Apparatus - Safety Requirements.
(Including report of IEC60825-1:2001 clause 8 and clause 9)

Notes

1. Laser (LED Backlight) Information

Class 1 LED Product IEC60825-1 : 2001 Embedded LED Power (Class 1)
--

2. Caution

- : LED inside.
- Class XX laser (LEDs) radiation when open.
- Do not open while operating.

7-2. Environment

- a) RoHS, Directive 2002/95/EC of the European Parliament and of the council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment

LC420EUG

Product Specification

8. Packing**8-1. Information of LCM Label**

a) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M
---	---	---	---	---	---	---	---	---	---	---	---	---

A,B,C : SIZE(INCH)
E : MONTH

D : YEAR
F ~ M : SERIAL NO.

Note

1. YEAR

Year	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
Mark	1	2	3	4	5	6	7	8	9	0

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	4	4	5	6	7	8	9	A	B	C

b) Location of Lot Mark

Serial NO. is printed on the label. The label is attached to the backside of the LCD module.
This is subject to change without prior notice.

8-2. Packing Form

a) Package quantity in one pallet : 15 ea

b) Pallet Size : 1140 mm X 990 mm X 125.5mm

Product Specification

9. Precautions

Please pay attention to the followings when you use this TFT LCD module.

9-1. Mounting Precautions

- (1) You must mount a module using specified mounting holes (Details refer to the drawings).
- (2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
- (3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
- (4) You should adopt radiation structure to satisfy the temperature specification.
- (5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
- (6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
- (7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzine. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
- (8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
- (9) Do not open the case because inside circuits do not have sufficient strength.

9-2. Operating Precautions

- (1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
 $V = \pm 200\text{mV}$ (Over and under shoot voltage)
- (2) Response time depends on the temperature. (In lower temperature, it becomes longer.)
- (3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time (required time that brightness is stable after turned on) becomes longer
- (4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
- (5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
- (6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.
- (7) Please do not give any mechanical and/or acoustical impact to LCM. Otherwise, LCM can't be operated its full characteristics perfectly.
- (8) A screw which is fastened up the steels should be a machine screw.
(if not, it can causes conductive particles and deal LCM a fatal blow)
- (9) Please do not set LCD on its edge.
- (10) The conductive material and signal cables are kept away from LED driver inductor to prevent abnormal display, sound noise and temperature rising.

Product Specification

9-3. Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9-4. Precautions for Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

9-5. Storage

When storing modules as spares for a long time, the following precautions are necessary.

- (1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
- (2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

9-6. Handling Precautions for Protection Film

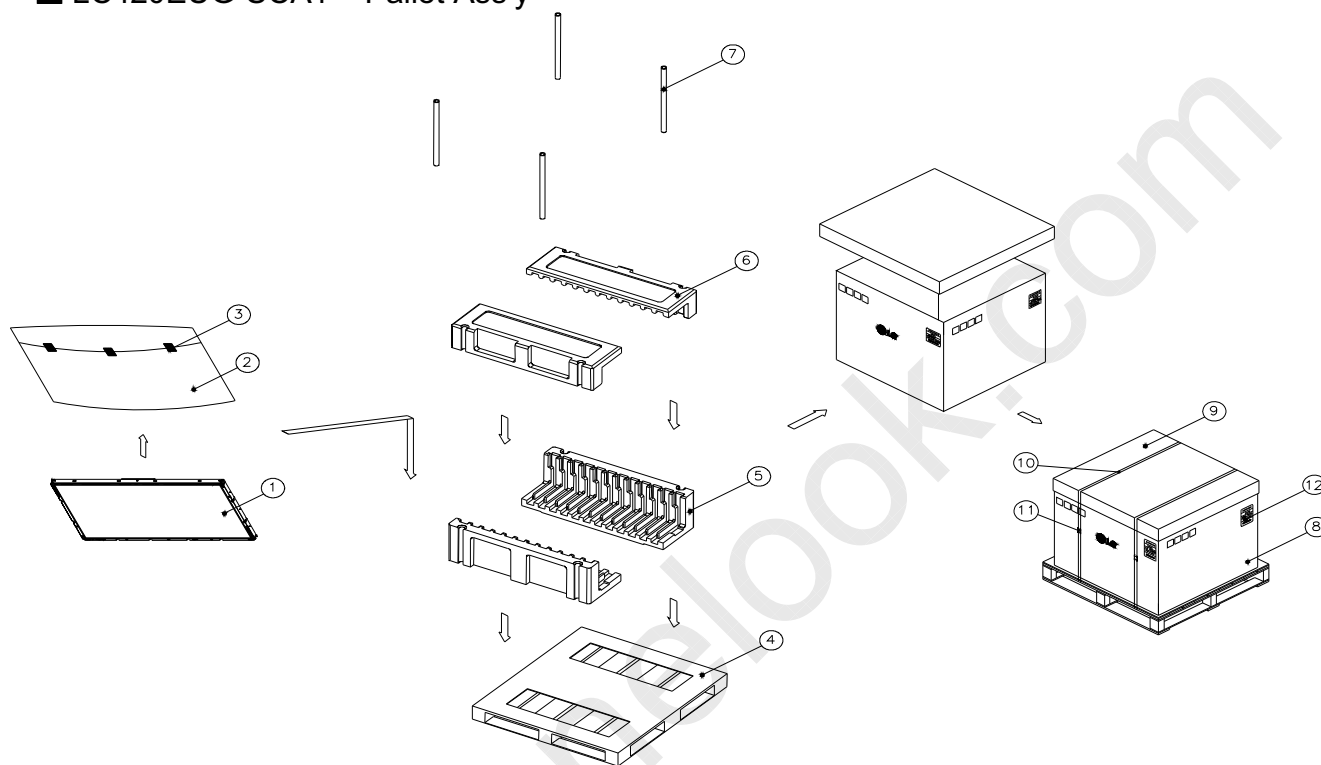
- (1) The protection film is attached to the bezel with a small masking tape.
When the protection film is peeled off, static electricity is generated between the film and polarizer.
This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
- (2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.
- (3) You can remove the glue easily. When the glue remains on the bezel surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

LC420EUG

Product Specification

APPENDIX-I

■ LC420EUG-SCA1 – Pallet Ass'y

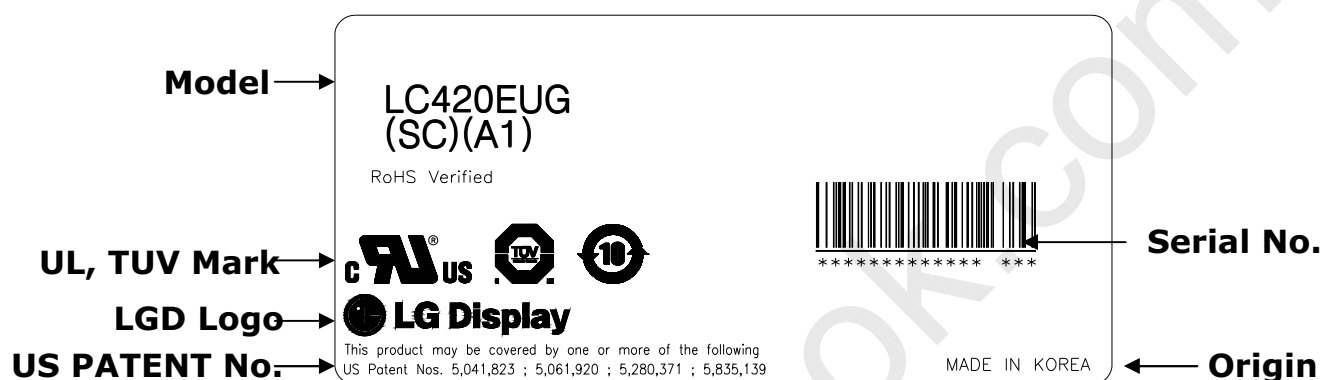


NO.	DESCRIPTION	MATERIAL
1	LCD Module	
2	BAG	42INCH
3	TAPE	MASKING 20MMX50M
4	PALLET	Plywood 1140X990X125.5mm
5	PACKING,BOTTOM	EPS
6	PACKING, TOP	EPS
7	ANGLE,POST	PAPER
8	ANGLE,PACKING	PAPER
9	ANGLE.COVER	PAPER
10	BAND,CLIP	STEEL or PP
11	BAND	PP
12	LABEL	YUPO 80G 100X70

LC420EUG

APPENDIX- II-1

■ LC420EUG-SCA1-LCM Label



■ Production site

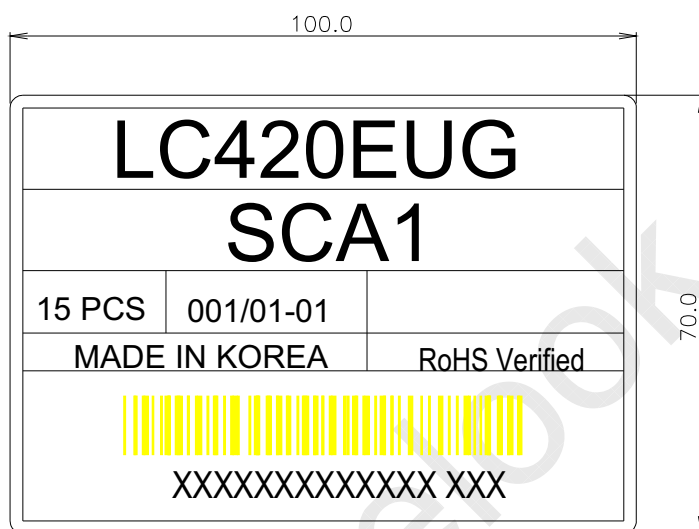
- LG Display (Paju) Co., LTD
- LG Display (Guangzhou) Co., LTD

Note 1.The origin of LCM Label will be changed according to the production site.

LC420EUG

APPENDIX- II-2

■ LC420EUG-SCA1-Pallet Label



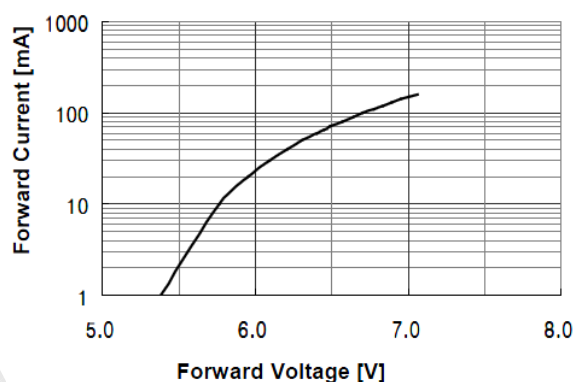
Product Specification

APPENDIX-III

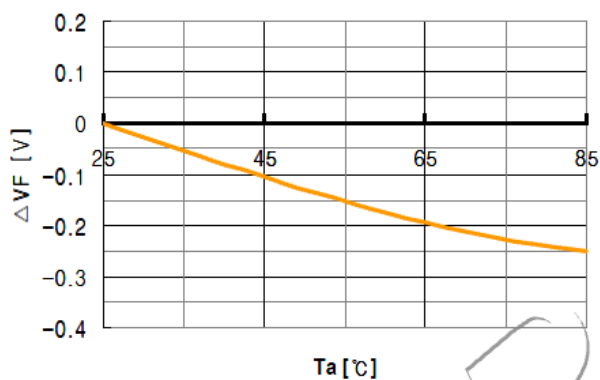
■ LED Array Electrical Spec

Items	Symbol	Condition	Min	Typ	Max	Unit
Array Operating Voltage	V_F	$I_{FM}=165mA$	110.2	117.8	125.4	V
	$\Delta V_{op}^{*2)}$	$I_{FM}=165mA$	-	-	1.7	V
Luminous of White	I_v	$I_{FM}=165mA$	11,020	11,600	-	nit
Color Chromaticity	C_x	$I_{FM}=165mA$	0.250	0.258	0.266	
	C_y	$I_{FM}=165mA$	0.200	0.208	0.216	
Bright Uniformity ^{*3)}	Bu	$I_{FM}=165mA$	90	-	-	%
Color Uniformity ^{*4)}	$\Delta u'v'$	$I_{FM}=165mA$	-	-	0.007	
Life time		$T_J \leq 70^\circ C$	30,000	50,000	-	hrs

■ Forward Current vs. Forward Voltage



■ Ambient Temperature vs. Forward Voltage



LC420EUG

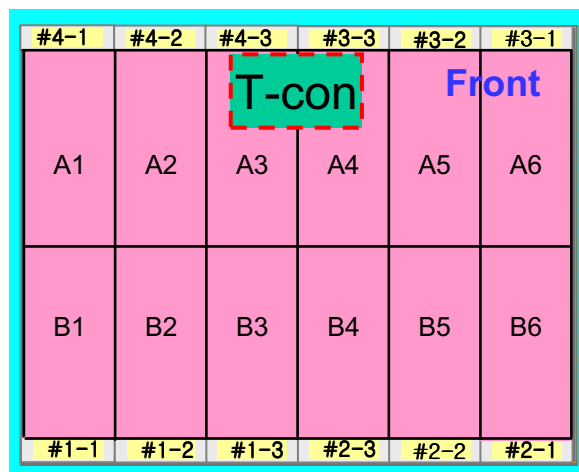
Product Specification

APPENDIX-IV

■ Local Dimming Block Pin Matching

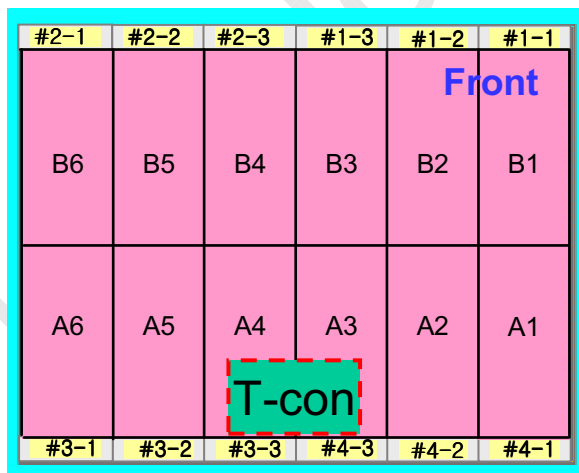
[CN2]

Pin No	Block
1	Vo_2
2	N.C
3	A6
4	A5
5	A4
6	N.C
7	N.C
8	N.C
9	A3
10	A2
11	A1
12	N.C
13	Vo_2



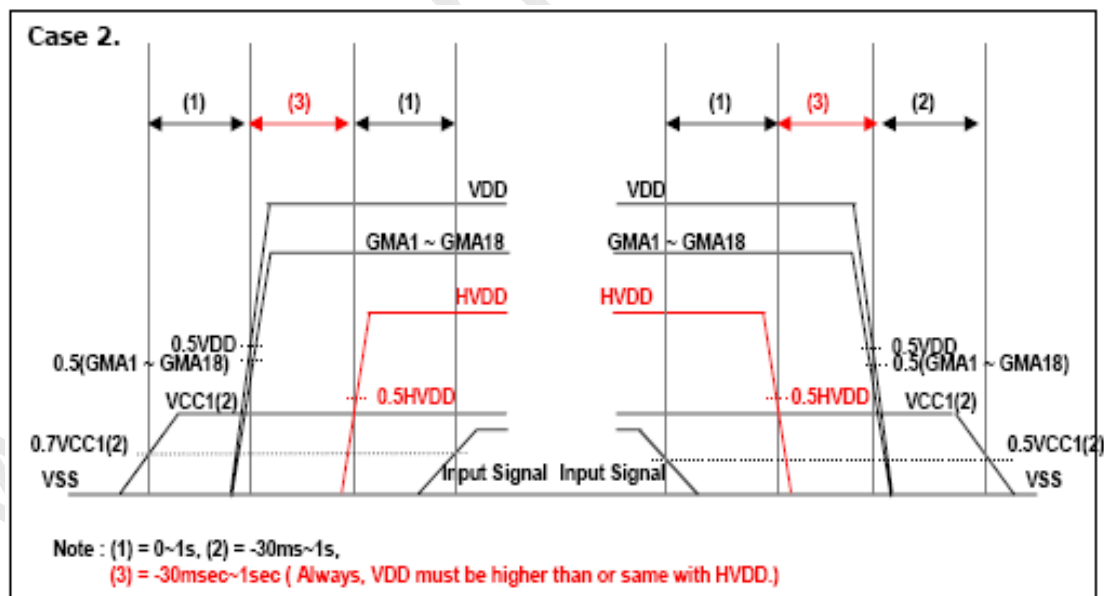
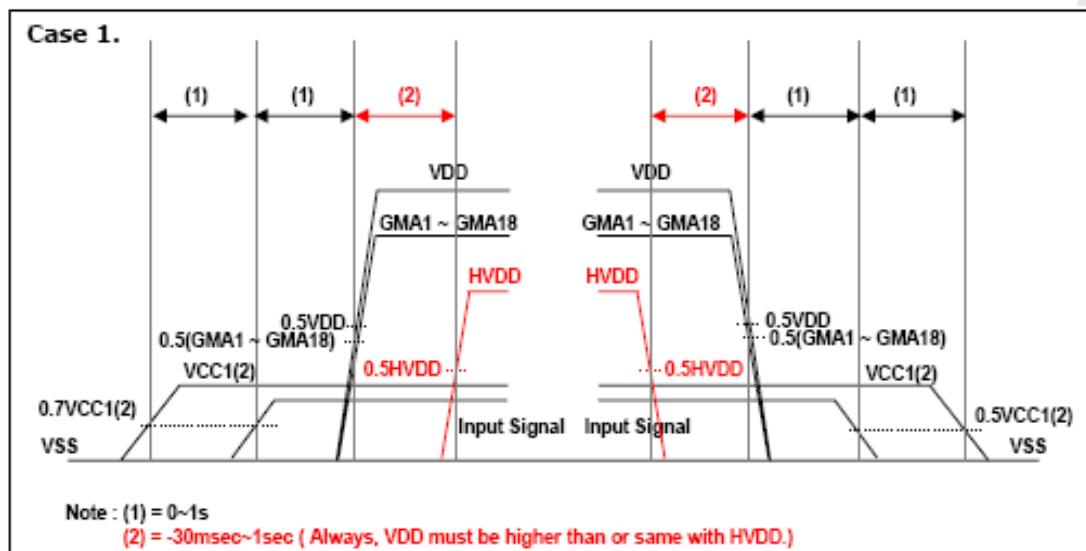
[CN1]

Pin No	Block
1	Vo_1
2	N.C
3	B1
4	B2
5	B3
6	N.C
7	N.C
8	B4
9	B5
10	B6
11	N.C
12	Vo_1



APPENDIX- V

■ LC420EUG-SCA1-Source D-IC Power Sequence



- Input Signal : SOE,POL,GSP,H_CONV,OPT_N