SPECIFICATION
FOR
APPROVAL

( ) Preliminary Specification
(●) Final Specification

Title	42.0” WUXGA TFT LCD

BUYER	General
MODEL	

SUPPLIER	LG Display Co., Ltd.
*MODEL	LC420WUH
SUFFIX	SCM1

*When you obtain standard approval,
please use the above model name without suffix

APPROVED BY	SIGNATURE / DATE
/	
/	
/	

Please return 1 copy for your confirmation with your signature and comments.

APPROVED BY	SIGNATURE / DATE
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TV Products Development Dept.
LG Display LCD Co., Ltd

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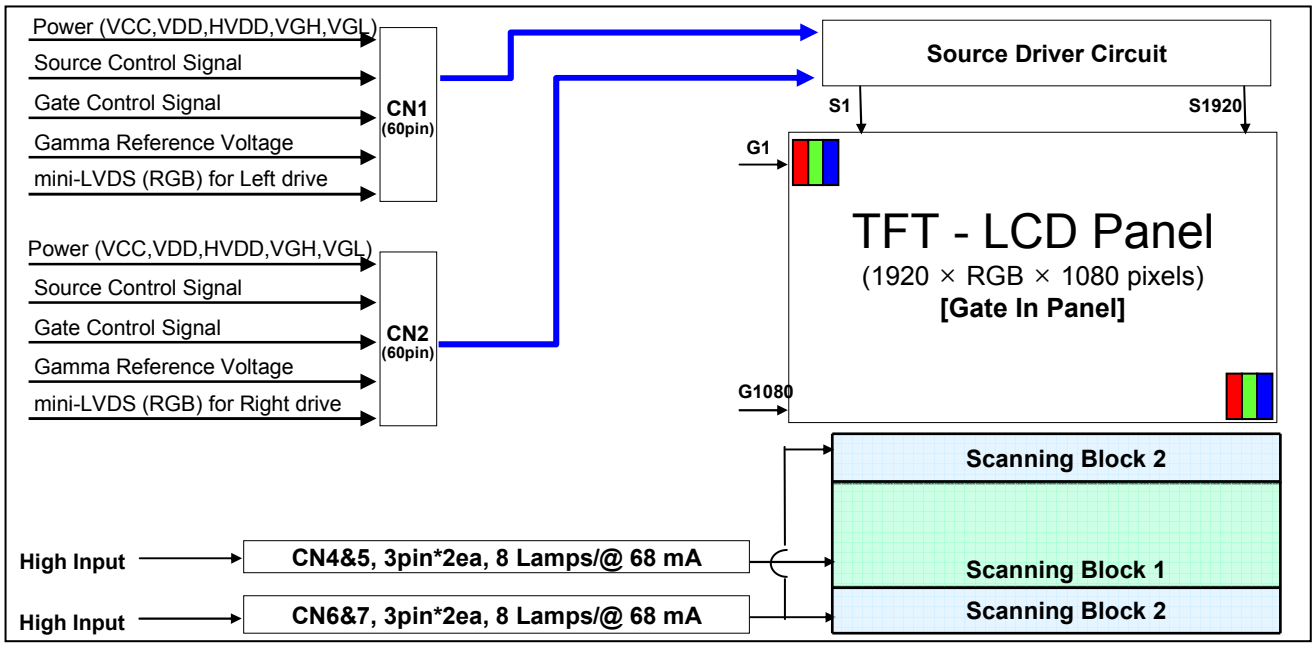
RECORD OF REVISIONS

Revision No.	Revision Date	Page	Description
1.2	Mar. 16..2010	-	Final Specification

1. General Description

The LC420WUH is a Color Active Matrix Liquid Crystal Display with an integral External Electrode Fluorescent Lamp(EEFL) backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally black mode. It has a 42.02 inch diagonally measured active display area with WUXGA resolution (1080 vertical by 1920 horizontal pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the luminance of the sub-pixel color is determined with a 8-bit gray scale signal for each dot. Therefore, it can present a palette of more than 16.7M(true) colors.
It is intended to support LCD TV, PCTV where high brightness, super wide viewing angle, high color gamut, high color depth and fast response time are important.



General Features

Active Screen Size	42.02 inches(1067.31mm) diagonal
Outline Dimension	983.0(H) x 576.0 (V) x 35.5 mm(D) (Typ.)
Pixel Pitch	0.4845 mm x 0.4845 mm
Pixel Format	1920 horiz. by 1080 vert. Pixels, RGB stripe arrangement
Color Depth	8-bit, 16.7 M colors (※ 1.06B colors @ 10 bit (D) System Output)
Drive IC Data Interface	Source D-IC : 8-bit mini-LVDS, gamma reference voltage, and control signals Gate D-IC : Gate In Panel
Luminance, White	500 cd/m^2 (Center 1point ,Typ.)
Viewing Angle (CR>10)	Viewing angle free (R/L 178 (Min.), U/D 178 (Min.))
Power Consumption	Total 158.0 W (Typ.) (Logic=9.0 W with T-CON, Backlight=149W @ with Inverter **Iout** duty : 100%)
Weight	8.7Kg (Typ.)
Display Mode	Transmissive mode, Normally black
Surface Treatment	Hard coating(3H), Anti-glare treatment of the front polarizer (Haze 10%)

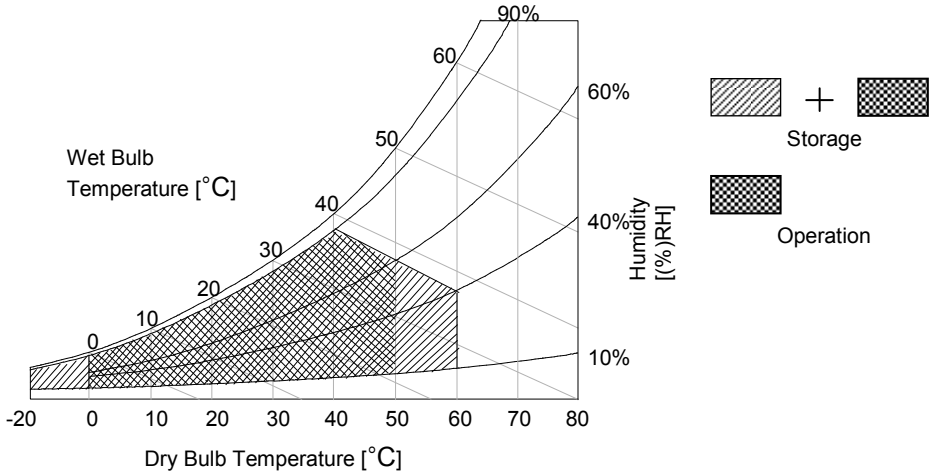
2. Absolute Maximum Ratings

The following items are maximum values which, if exceeded, may cause faulty operation or damage to the LCD module.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value		Unit	Note
		Min	Max		
Logic Power Voltage	VCC	-0.5	+4.0	VDC	1
Gate High Voltage	VGH	+18.0	+30.0	VDC	
Gate Low Voltage	VGL	-8.0	-4.0	VDC	
Source D-IC Analog Voltage	VDD	-0.3	+18.0	VDC	
Gamma Ref. Voltage (Upper)	VGMH	½VDD-0.5	VDD+0.5	VDC	
Gamma Ref. Voltage (Low)	VGML	-0.3	½ VDD+0.5	VDC	
BL Operating Input Voltage (One Side)	VBL	600	1150	VRMS	
Panel Front Temperature	TSUR	-	+68	°C	4
Operating Temperature	TOP	0	+50	°C	2,3
Storage Temperature	TST	-20	+60	°C	
Operating Ambient Humidity	HOP	10	90	%RH	
Storage Humidity	HST	10	90	%RH	

Note: 1. Ambient temperature condition (Ta = 25 ± 2 °C)
2. Temperature and relative humidity range are shown in the figure below. Wet bulb temperature should be Max 39 °C and no condensation of water.
3. Gravity mura can be guaranteed below 40℃ condition.
4. The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 68 ℃ with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 68 ℃. The range of operating temperature may degrade in case of improper thermal management in final product design.



3. Electrical Specifications

3-1. Electrical Characteristics

It requires several power inputs. The VCC is the basic power of LCD Driving power sequence, Which is used to logic power voltage of Source D-IC and GIP.

Table 2. ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Note
Logic Power Voltage	VCC	-	3.0	3.3	3.6	VDC	
Logic High Level Input Voltage	VIH		2.7		VCC	VDC	
Logic Low Level Input Voltage	VIL		0		0.6	VDC	
Source D-IC Analog Voltage	VDD	-	16.05	16.25	16.45	VDC	
Half Source D-IC Analog Voltage	H_VDD	-	7.9	8.00	8.1	VDC	
Gamma Reference Voltage	V_{GMH}	(GMA1 ~ GMA9)	½*VDD		VDD-0.2		
	V_{GML}	(GMA10 ~ GMA18)	0.2		½*VDD		
Common Voltage	Vcom	-	6.6	6.9	7.2	V	
Mini-LVDS Clock frequency	CLK	3.0V≤VCC ≤3.6V			312	MHz	
mini-LVDS input Voltage (Center)	VIB	Mini-LVDS Clock and Data	0.7 + (VID/2)		(VCC-1.2) − VID / 2	V	5
mini-LVDS input Voltage Distortion (Center)	ΔVIB				0.8	V	
mini-LVDS differential Voltage range	VID		150		800	mV	
mini-LVDS differential Voltage range Dip	ΔVID		25		800	mV	
Gate High Voltage	VGH		27.39 @ 25℃ 28.85 @ 0℃	27.69 @ 25℃ 29.15 @ 0℃	27.99 @ 25℃ 29.45 @ 0℃	VDC	
Gate Low Voltage	VGL		-5.5	-5.3	-5.1	VDC	
GIP Bi-Scan Voltage	VGI_P VGI_N	-	VGL	-	VGH	VDC	
GIP Refresh Voltage	VGH even/odd	-	VGL	-	VGH	V	
GIP Start Pulse Voltage	VST	-	VGL	-	VGH	V	
GIP Operating Clock	GCLK	-	VGL	-	VGH	V	
Total Power Current	ILCD	-	525	750	975	mA	2
Total Power Consumption	PLCD	-		9.0		Watt	2

Note:
1. The specified current and power consumption are under the V_{LCD}=12V., 25 ± 2°C, f_V=120Hz condition whereas mosaic pattern(8 x 6) is displayed and f_V is the frame frequency.
2. The above spec is based on the basic model.
3. All of the typical gate voltage should be controlled within 1% voltage level
4. Ripple voltage level is recommended under 10%
5. In case of mini-LVDS signal spec, refer to Fig 2 for the more detail.
6. Logic level Input Signal : SOE, POL, GSP, H_CONV, OPT_N
7. HVDD Voltage level is half of VDD and it should be between Gamma9 and Gamma10

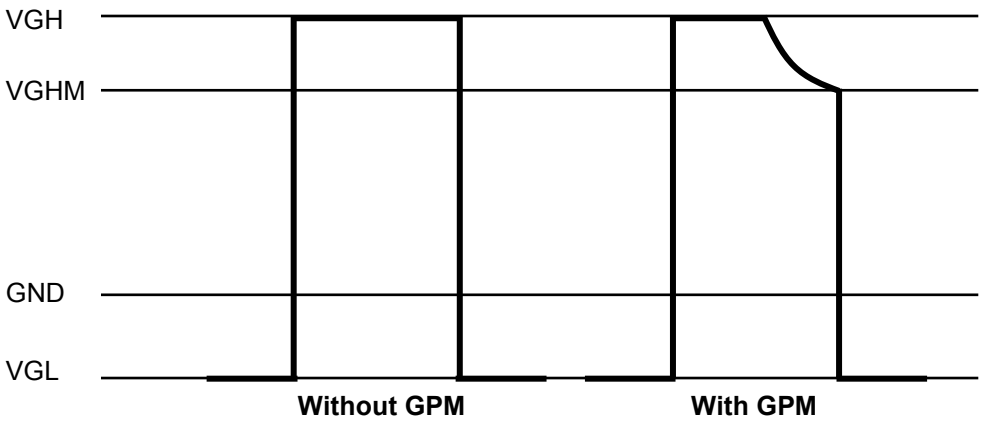


FIG. 1 Gate Output Wave form without GPM and with GPM

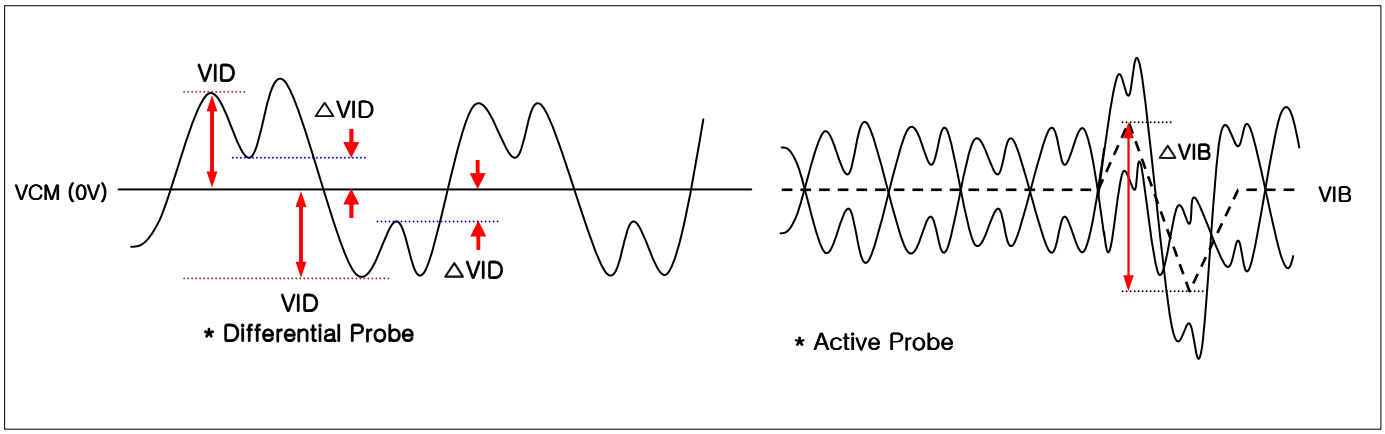


FIG. 2 Description of VID, ΔVIB, ΔVID

* Source PCB

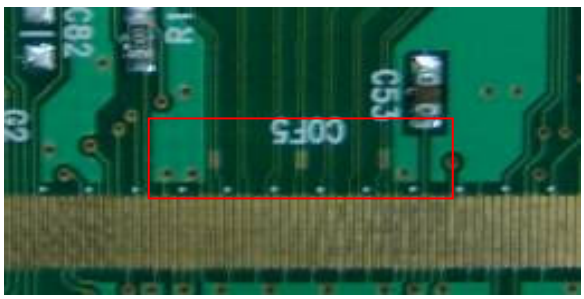


FIG. 3 Measure point

Table 3. ELECTRICAL CHARACTERISTICS (Continue)

Parameter		Symbol	Values			Unit	Note
			Min	Typ	Max		
Backlight Assembly :							
Operating Voltage (one side,fBL=63KHz, I_{BL}= 136 mA_{RMS})		V_{BL1}	-	1000	-	V_{RMS}	1, 2
		V_{BL2}	-	1000	-		
Operating Current (one side)		I_{BL1}	-	68	-	mA_{RMS}	1
		I_{BL2}	-	68	-		
Striking Voltage @ 0℃ (Open Lamp Voltage @ one side)		V_S	-	-	1110	V_{RMS}	1, 3
Operating Frequency		f_{BL}	61	63	65	kHz	4
Striking Time		S_{TIME}	1.5	-	-	sec	3
Power Consumption		P_{BL}		149		Watt	6
Burst Dimming Duty		{a/T} * 100	20		100	%	9
Burst Dimming Frequency	PAL	1/T		100		Hz	9
	NTSC			120			

Parameter	Symbol	Values			Unit	Note
		Min	Typ	Max		
Lamp : (APPENDIX-V)						
Lamp Voltage (one side)	V_{LAMP}	815	1100	1135	V_{RMS}	2
Lamp Current (one side)	I_{LAMP}	3.0	8.5	9.0	mA_{RMS}	
Discharge Stabilization Time	T_S	-	-	3	Min	5
Lamp Frequency	f_{LAMP}	661	63	65	KHz	
Established Starting Voltage @ 0℃	V_S			1110	V_{RMS}	3
Life Time		50,000	60,000		Hrs	7

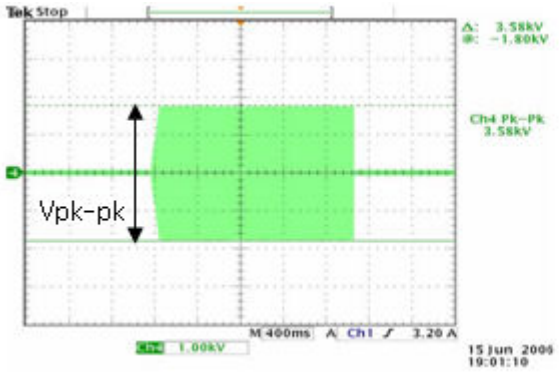
Note : The design of the inverter must have specifications for the lamp in LCD Assembly**.**
The electrical characteristics of inverter are based on High-High Driving type.
The performance of the lamps in LCM, for example life time or brightness, is extremely influenced by the characteristics of the DC-AC inverter. So, all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.
When you design or order the inverter, please make sure unwanted lighting caused by the mismatch of the lamp and the inverter (no lighting, flicker, etc) has never been occurred. When you confirm it, the LCD– Assembly should be operated in the same condition as installed in your instrument.

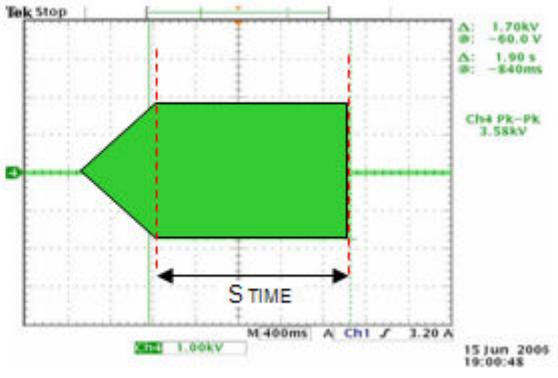
※ Do not attach a conductive tape to lamp connecting wire.
If you attach conductive tape to the lamp wire, not only luminance level can be lower than typical one but also inverter operate abnormally on account of leakage current which is generated between lamp wire and conductive tape.

1. Specified values are defined for a Backlight Assembly.
(**SCAN Block1** IBL:8 lamps, 8.5mA/Lamp and **SCAN Block2** IBL:8 lamps, 8.5mA/Lamp)
and each value is measured at duty 100%.
The lamp voltage must be synchronized between Block1 and Block2.
(The frequency and phase must be the same)

2. Operating voltage is measured at 25 ± 2°C(after 2hr.aging). The variance range for operating voltage is ± 10%.

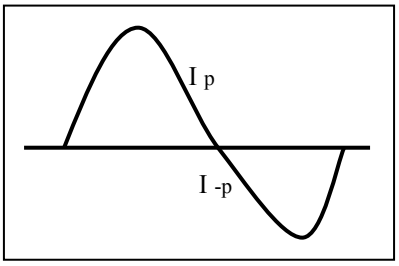
3. The Striking Voltage (Open Lamp Voltage) [Vopen] should be applied to the lamps more than Striking time (S TIME) for start-up. Inverter Striking Voltage must be more than Established Starting Voltage of lamp. Otherwise, the lamps may not be turned on. The used lamp current is typical value.
When the Striking Frequency is higher than the Operating Frequency, the parasitic capacitance can cause inverter shut down, therefore It is recommended to check it.





Vs = (Vpk-pk) / [2*root(2)]

4. Lamp frequency may produce interference with horizontal synchronous frequency. As a result this may cause beat on the display. Therefore, lamp frequency shall be away as much as possible from the horizontal synchronous frequency and its harmonics range in order to prevent interference.
   There is no reliability problem of lamp, if the operation frequency is typ ± 5KHz. But it should be applied in less than ABSOLUTE MAXIMUM RATINGS max voltage
5. The brightness of the lamp after lighted for 5minutes is defined as 100%.
   T_S is the time required for the brightness of the center of the lamp to be not less than 95% at typical current.
   The screen of LCD module may be partially dark by the time the brightness of lamp is stable after turn on.
6. Maximum level of power consumption is measured at initial turn on.
   Typical level of power consumption is measured after 2hrs aging at 25 ± 2°C.(@I out duty : 100%)
7. The life time is determined as the time at which brightness of the lamp is 50% compared to that of initial value at the typical lamp current on condition of continuous operating at 25 ± 2°C, based on duty 100%.
8. The output of the inverter must have symmetrical(negative and positive) voltage and current waveform (Unsymmetrical ratio is less than 10%). Please do not use the inverter which has not only unsymmetrical voltage and current but also spike wave.
   Requirements for a system inverter design, which is intended to achieve better display performance, power efficiency and more reliable lamp characteristics.
   It can help increase the lamp lifetime and reduce leakage current.
   a. The asymmetry rate of the inverter waveform should be less than 10%.
   b. The distortion rate of the waveform should be within √2 ±10%.
   * Inverter output waveform had better be more similar to ideal sine wave.



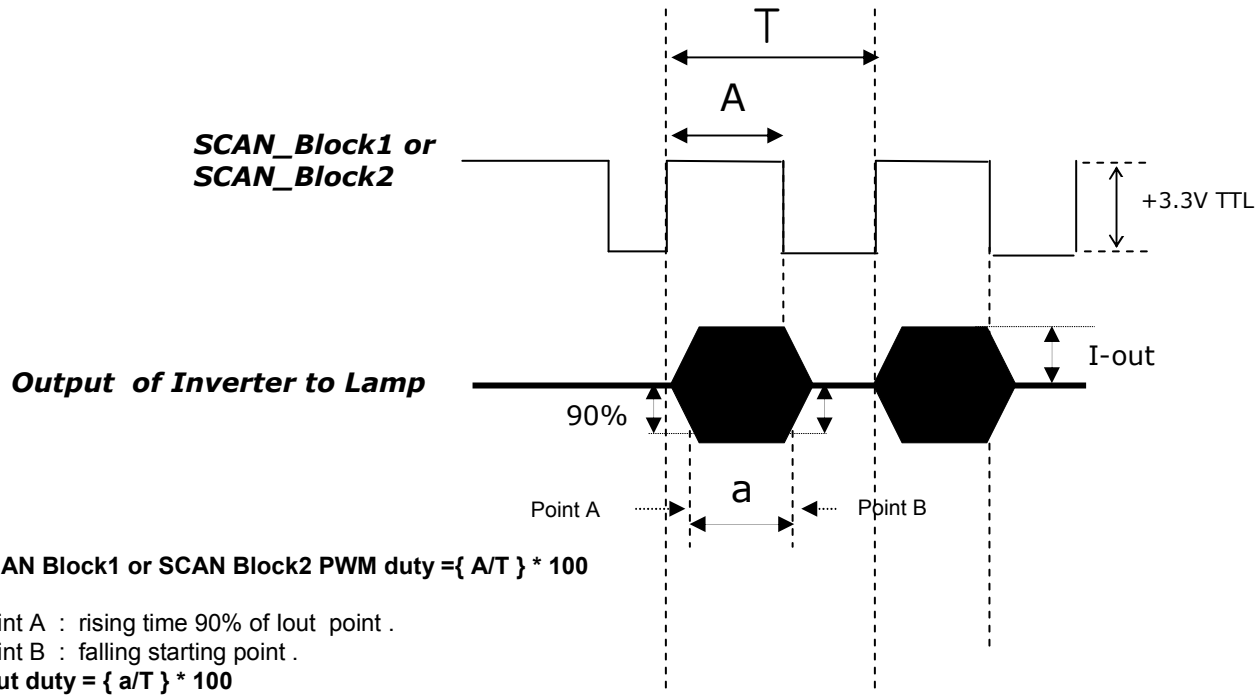
* Asymmetry rate:

$| I_p - I_{-p} | / I_{RMS} \times 100\%$

* Distortion rate

I_p (or I_{-p}) / I_{RMS}

9. The reference method of burst dimming duty ratio.



SCAN Block1 or SCAN Block2 PWM duty ={ A/T } * 100

Point A : rising time 90% of Iout point .
Point B : falling starting point .
I out duty = { a/T } * 100

SCAN Block1 or SCAN Block2 Frequency = 1/T

※ We recommend not to be much different between SCAN BLK 1 or SCAN BLK2 duty and Iout duty .
※ Dimming current output rising and falling time may produce humming and inverter trans' sound noise.
※ Burst dimming duty should be 100% for more than 1second after turn on.
※ Equipment
Oscilloscope :TDS3054B(Tektronix)
Current Probe : P6022 AC (Tektronix)
High Voltage Probe: P5100(Tektronix)

10. The Cable between the backlight connector and its inverter power supply should be connected directly with a minimized length. The longer cable between the backlight and the inverter may cause the lower luminance of lamp and may require more higher starting voltage (Vs).

11. The operating current must be measured as near as backlight assembly input.

12. The operating current unbalance between left and right side for each scanning block must be under 10% of Typical current.

| Left(Master) current – Right(Slave) Current | 〈 10% of typical current

3-2. Interface Connections

This LCD module employs two kinds of interface connection, two 60-pin FFC connector are used for the module electronics and two 3-pin Balance PCB connectors are used for the integral backlight system.

3-2-1. LCD Module

-LCD Connector (CN1): TF06L-60S-0.5SH (Manufactured by HRS) or Equivalent

Table 4-1. MODULE CONNECTOR(CN1) PIN CONFIGURATION

No	Symbol	Description	No	Symbol	Description
1	GND	Ground	31	LLV3 -	Left Mini LVDS Receiver Signal(3-)
2	LTD_OUT	LTD OUTPUT	32	LLV3 +	Left Mini LVDS Receiver Signal(3+)
3	GCLK1	GIP GATE Clock 1	33	LCLK -	Left Mini LVDS Receiver Clock Signal(-)
4	GCLK2	GIP GATE Clock 2	34	LCLK +	Left Mini LVDS Receiver Clock Signal(+)
5	GCLK3	GIP GATE Clock 3	35	LLV2 -	Left Mini LVDS Receiver Signal(2-)
6	GCLK4	GIP GATE Clock 4	36	LLV2 +	Left Mini LVDS Receiver Signal(2+)
7	GCLK5	GIP GATE Clock 5	37	LLV1 -	Left Mini LVDS Receiver Signal(1-)
8	GCLK6	GIP GATE Clock 6	38	LLV1 +	Left Mini LVDS Receiver Signal(1+)
9	VGI_N	VGL	39	LLV0 -	Left Mini LVDS Receiver Signal(0-)
10	VGI_P	VGH	40	LLV0 +	Left Mini LVDS Receiver Signal(0+)
11	VGH_ODD	GIP Panel VDD for Odd GATE TFT	41	GND	Ground
12	VGH_EVEN	GIP Panel VDD for Even GATE TFT	42	SOE	Source Output Enable SIGNAL
13	VGL	GATE Low Voltage	43	POL	Polarity Control Signal
14	VST	VERTICAL START PULSE	44	GSP	GATE Start Pulse
15	GND	Ground	45	H_CONV	"H“ H 2dot Inversion/ "L" H 1dot Inversion
16	VCOM_L_FB	VCOM Left Feed-Back Output	46	OPT_N	“H” Normal Display
17	VCOM_L	VCOM Left Input	47	GND	Ground
18	GND	Ground	48	GMA 18	GAMMA VOLTAGE 18 (Output From LCD)
19	VDD	Driver Power Supply Voltage	49	GMA 16	GAMMA VOLTAGE 16
20	VDD	Driver Power Supply Voltage	50	GMA 15	GAMMA VOLTAGE 15
21	H_VDD	Half Driver Power Supply Voltage	51	GMA 14	GAMMA VOLTAGE 14
22	H_VDD	Half Driver Power Supply Voltage	52	GMA 12	GAMMA VOLTAGE 12
23	GND	Ground	53	GMA 10	GAMMA VOLTAGE 10 (Output From LCD)
24	VCC	Logic Power Supply Voltage	54	GMA 9	GAMMA VOLTAGE 9 (Output From LCD)
25	VCC	Logic Power Supply Voltage	55	GMA 7	GAMMA VOLTAGE 7
26	GND	Ground	56	GMA 5	GAMMA VOLTAGE 5
27	LLV5 -	Left Mini LVDS Receiver Signal(5-)	57	GMA 4	GAMMA VOLTAGE 4
28	LLV5 +	Left Mini LVDS Receiver Signal(5+)	58	GMA 3	GAMMA VOLTAGE 3
29	LLV4 -	Left Mini LVDS Receiver Signal(4-)	59	GMA 1	GAMMA VOLTAGE 1(Output From LCD)
30	LLV4 +	Left Mini LVDS Receiver Signal(4+)	60	NC	No Connection

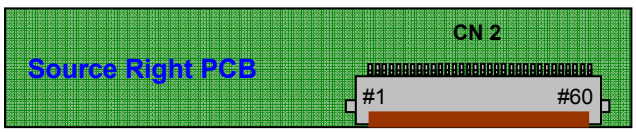
Note : 1. Please refer to application note (**Half VDD & Gamma Voltage setting & Control signal**) for details.
2. These 'input signal' (OPT_N,H_CONV) should be connected

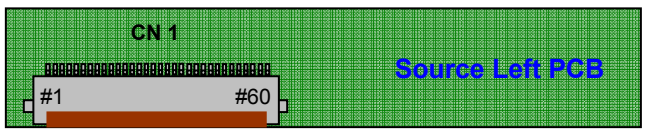
-LCD Connector (CN2): TF06L-60S-0.5SH(Manufactured by HRS) or Equivalent

Table 4-2. MODULE CONNECTOR(CN2) PIN CONFIGURATION

No	Symbol	Description		No	Symbol	Description
1	NC	No Connection		31	RLV1 -	Right Mini LVDS Receiver Signal(1-)
2	GMA 1	GAMMA VOLTAGE 1 (Output From LCD)		32	RLV1 +	Right Mini LVDS Receiver Signal(1+)
3	GMA 3	GAMMA VOLTAGE 3		33	RLV0 -	Right Mini LVDS Receiver Signal(0-)
4	GMA 4	GAMMA VOLTAGE 4		34	RLV0 +	Right Mini LVDS Receiver Signal(0+)
5	GMA 5	GAMMA VOLTAGE 5		35	GND	Ground
6	GMA 7	GAMMA VOLTAGE 7		36	VCC	Logic Power Supply Voltage
7	GMA 9	GAMMA VOLTAGE 9 (Output From LCD)		37	VCC	Logic Power Supply Voltage
8	GMA 10	GAMMA VOLTAGE 10 (Output From LCD)		38	GND	Ground
9	GMA 12	GAMMA VOLTAGE 12		39	H_VDD	Half Driver Power Supply Voltage
10	GMA 14	GAMMA VOLTAGE 14		40	H_VDD	Half Driver Power Supply Voltage
11	GMA 15	GAMMA VOLTAGE 15		41	VDD	Driver Power Supply Voltage
12	GMA 16	GAMMA VOLTAGE 16		42	VDD	Driver Power Supply Voltage
13	GMA 18	GAMMA VOLTAGE 18 (Output From LCD)		43	GND	Ground
14	GND	Ground		44	VCOM_R	VCOM Right Input
15	OPT_N	“H” Normal Display		45	VCOM_R_FB	VCOM Right Feed-Back Output
16	H_CONV	"H“ H 2dot Inversion/ "L" H 1dot Inversion		46	GND	Ground
17	GSP	GATE Start Pulse		47	VST	VERTICAL START PULSE
18	POL	Polarity Control Signal		48	VGL	GATE Low Voltage
19	SOE	Source Output Enable SIGNAL		49	VGH_EVEN	GIP Panel VDD for Even GATE TFT
20	GND	Ground		50	VGH_ODD	GIP Panel VDD for Odd GATE TFT
21	RLV5 -	Right Mini LVDS Receiver Signal(5-)		51	VGI_P	VGH
22	RLV5 +	Right Mini LVDS Receiver Signal(5+)		52	VGI_N	VGL
23	RLV4 -	Right Mini LVDS Receiver Signal(4-)		53	GCLK6	GIP GATE Clock 6
24	RLV4 +	Right Mini LVDS Receiver Signal(4+)		54	GCLK5	GIP GATE Clock 5
25	RLV3 -	Right Mini LVDS Receiver Signal(3-)		55	GCLK4	GIP GATE Clock 4
26	RLV3 +	Right Mini LVDS Receiver Signal(3+)		56	GCLK3	GIP GATE Clock 3
27	RCLK -	Right Mini LVDS Receiver Clock Signal(-)		57	GCLK2	GIP GATE Clock 2
28	RCLK +	Right Mini LVDS Receiver Clock Signal(+)		58	GCLK1	GIP GATE Clock 1
29	RLV2 -	Right Mini LVDS Receiver Signal(2-)		59	LTD_OUT	LTD OUTPUT
30	RLV2 +	Right Mini LVDS Receiver Signal(2+)		60	GND	Ground

Note : 1.Please refer to application note (**Half VDD & Gamma Voltage setting & Control signal**) for details.
2. These 'input signal' (OPT_N,H_CONV) should be connected





3-2-2. Backlight Module

[Master]

1) Balance Connector

: 65002WS-03 (manufactured by YEONHO) or equivalent

2) Mating Connector

: 65002HS-03 (manufactured by YEONHO) or equivalent.

[Slave]

1) Balance Connector

: 65002WS-03 (manufactured by YEONHO) or equivalent

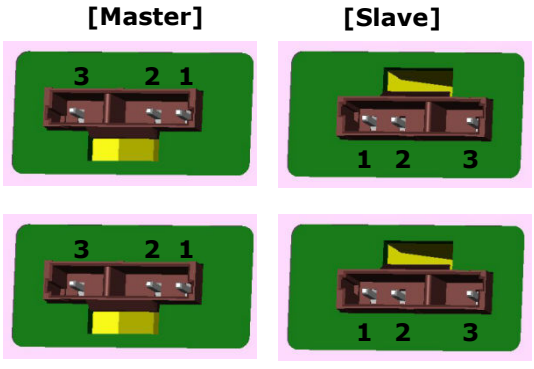
2) Mating Connector

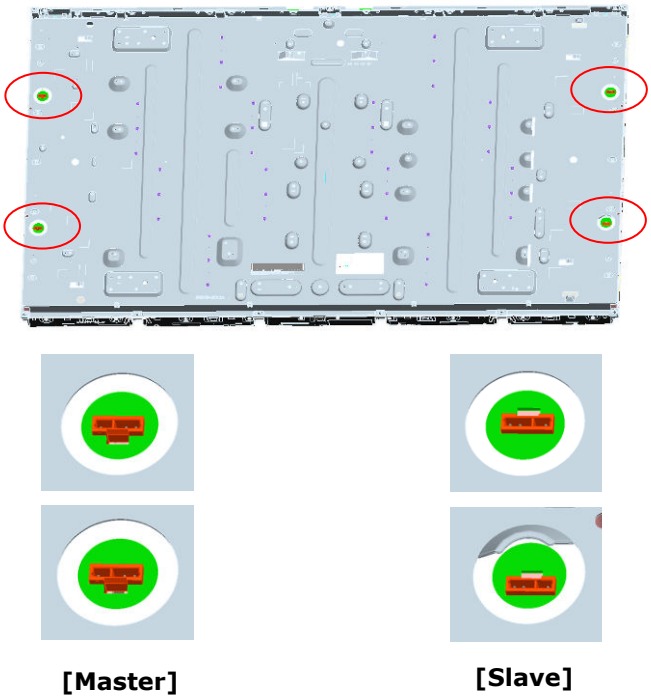
: 65002HS-03 (manufactured by YEONHO) or equivalent.

Table 5. BACKLIGHT CONNECTOR PIN CONFIGURATION(CN2,CN3)

No	Symbol	Master		Slave		Note
		Scanning BLK1	Scanning BLK2	Scanning BLK1	Scanning BLK2	
1	**H_Input**	High_Input		High_Input		
2	**H_Input**	High_Input		High_Input		
3	**FB**	NC		NC		

◆ Rear view of LCM





3-3. Signal Timing Specifications

Table 6. Timing Requirements

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Mini Clock pulse period	T_1		3.2	3.4		ns	1
Mini Clock pulse low period	T_2		1.6	-	-	ns	
Mini Clock pulse high period	T_3		1.6	-	-	ns	
Mini Data setup time	T_6		0.60	-	-	ns	
Mini Data hold time	T_7		0.60	-	-	ns	
Reset low to SOE rising time	T_8		0	-	-	ns	
SOE to Reset input time	T_9		200	-	-	ns	
Receiver off to SOE timing	T_{10}		10	-	-	CLK cycle	
POL signal to SOE setup time	T_{11}		-5	-	-	ns	
POL signal to SOE hold time	T_{12}		6	-	-	ns	
Reset High Period	T_{13}		3			CLK cycle	
SOE signal GSP setup time	T_{14}		100			ns	
SOE signal GSP Hold time	T_{15}		100			ns	
SOE signal Pulse Width	T_{16}		200			ns	

Note : 1. mini-LVDS timing measure conditions:
: 268 MHz < Clock Frequency <312 MHz , 150mV < VID < 800mV @ 3.0< VCC <3.3
2. Setup time and hold time should be satisfied at the same time

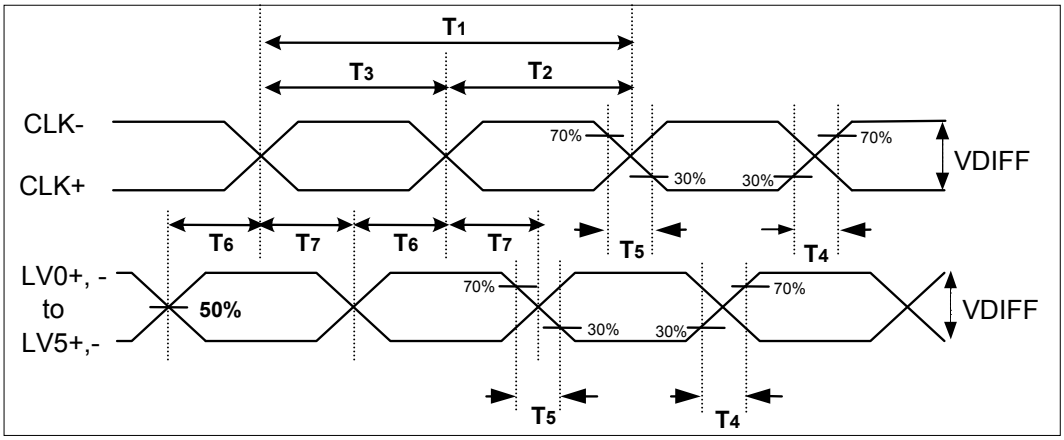


FIG 4. Source D-IC Input Data Latch Timing Waveform

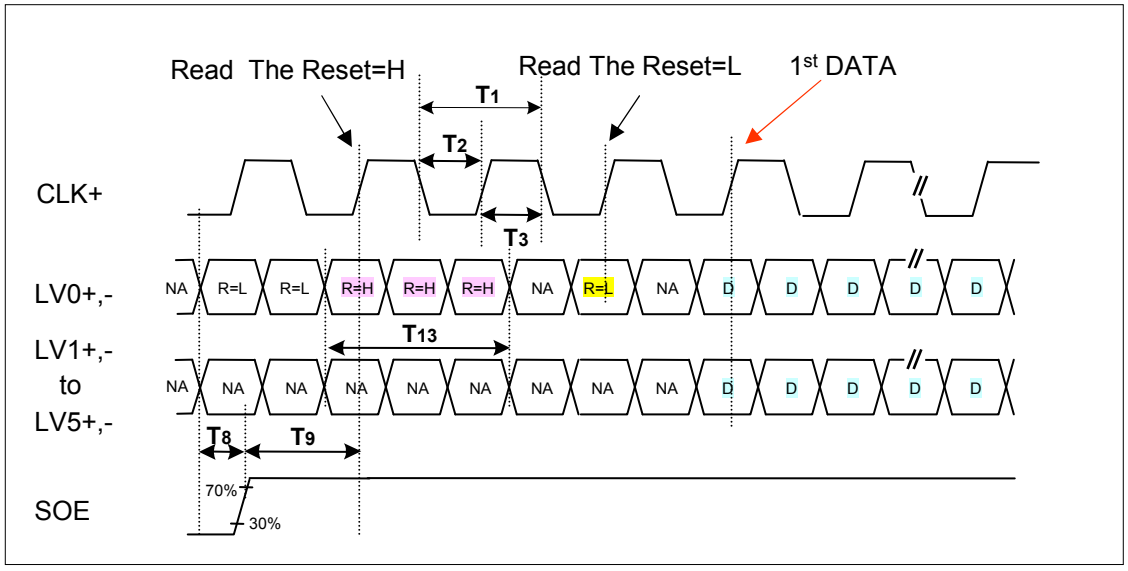


FIG 5-1. Input Data Timing for 1st Source D-IC Chip

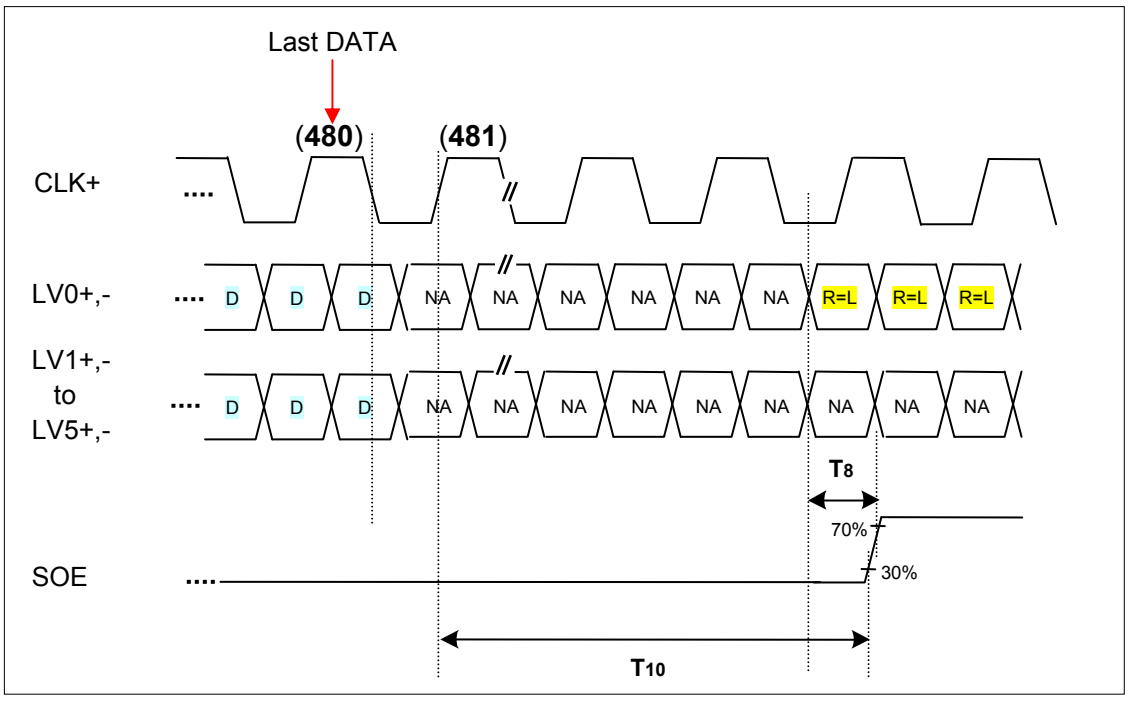


FIG 5-2. Last Data Latch to SOE Timing

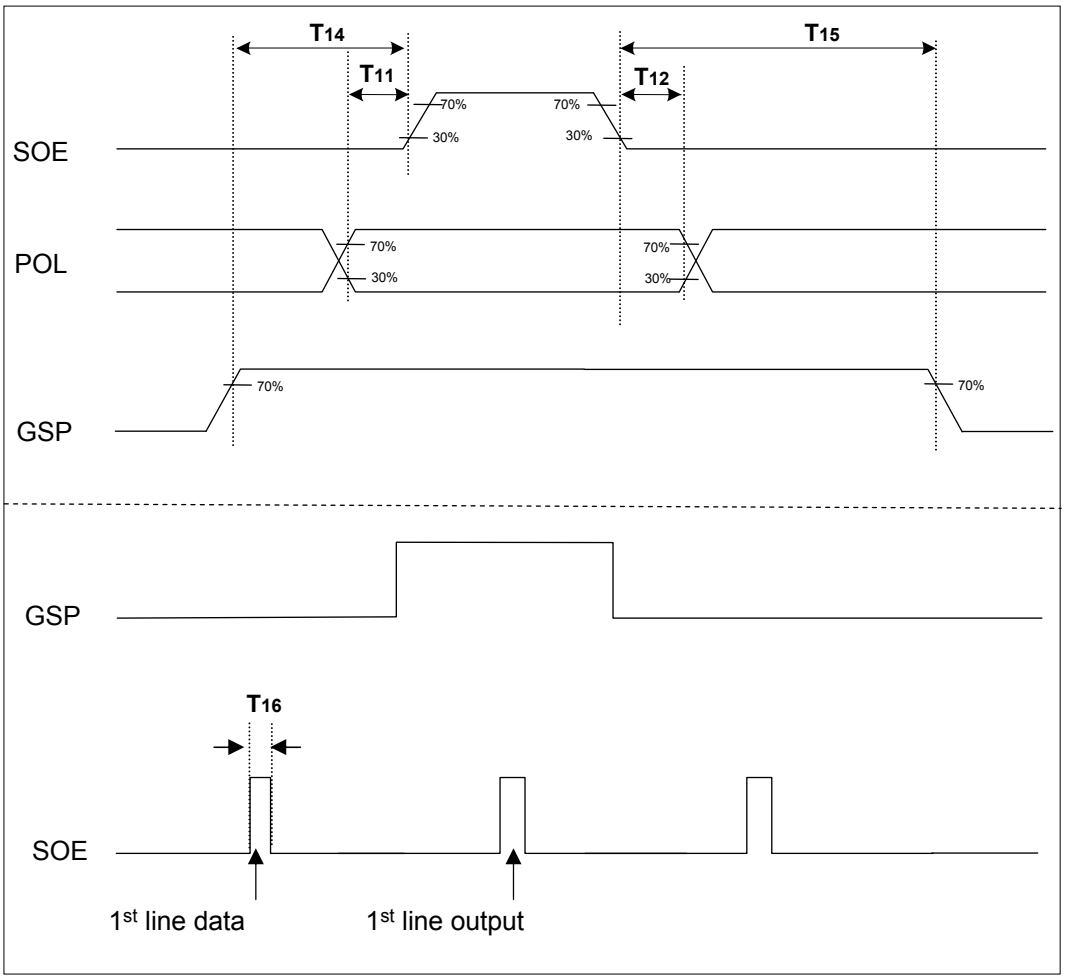
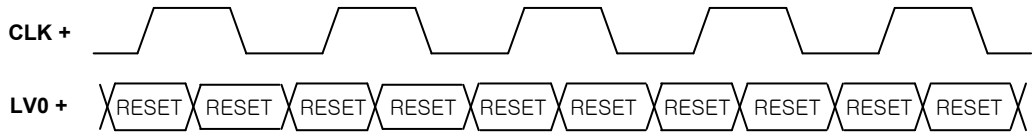


FIG 6. POL, GSP and SOE Timing Waveform

3-4. Data Mapping and Timing

Display data and control signal (RESET) are input to **LV0** to **LV5**.

3-4-1. Control signal input mode



3-4-2. Display data input mode

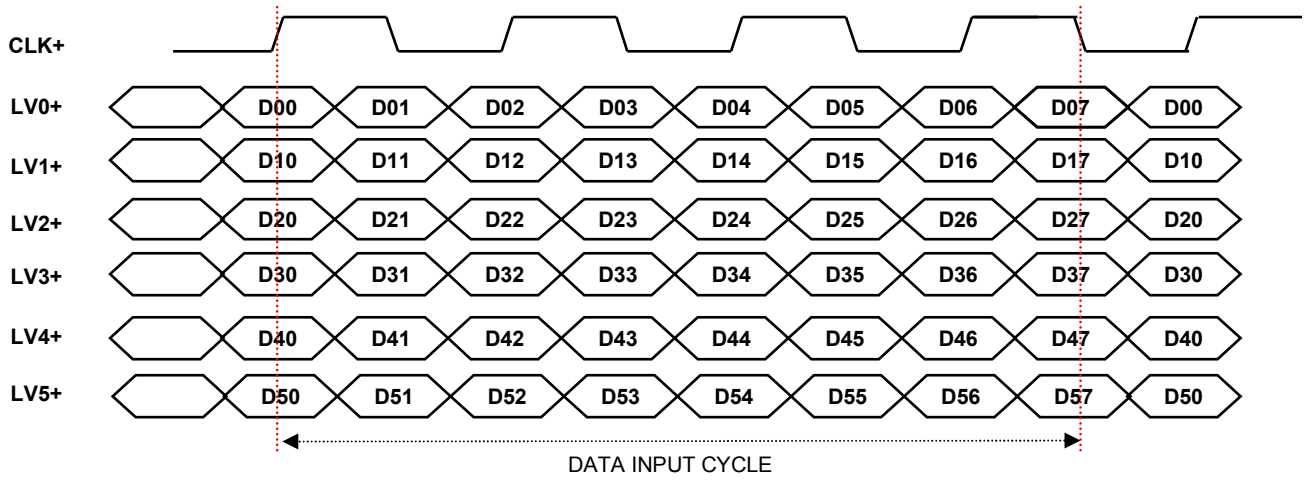


Fig. 7 Mini-LVDS Data

Note : 1. For data mapping, please refer to panel pixel structure Fig.8

3-5. Panel Pixel Structure

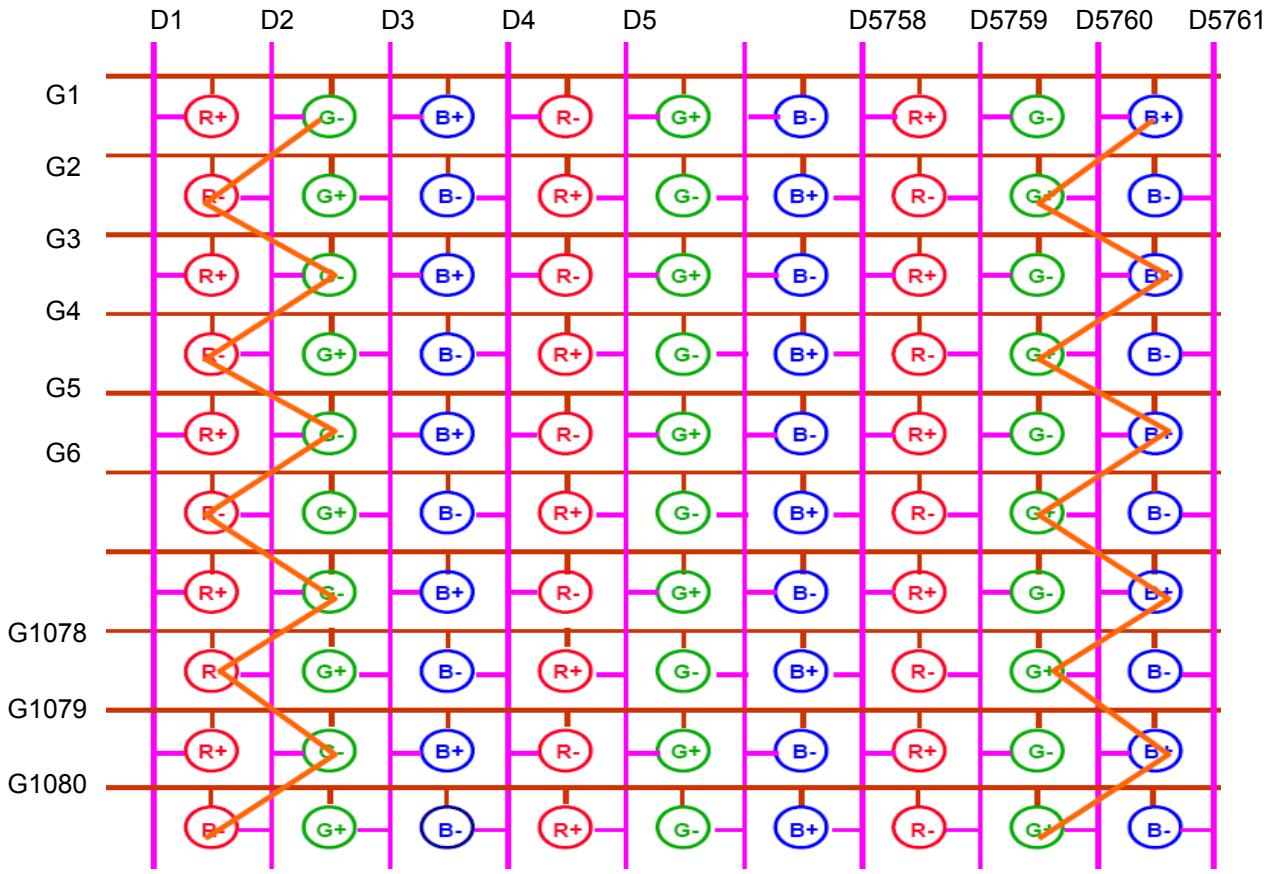


FIG. 8 Panel Pixel Structure

3-6. Power Sequence

3-6-1. LCD Driving circuit

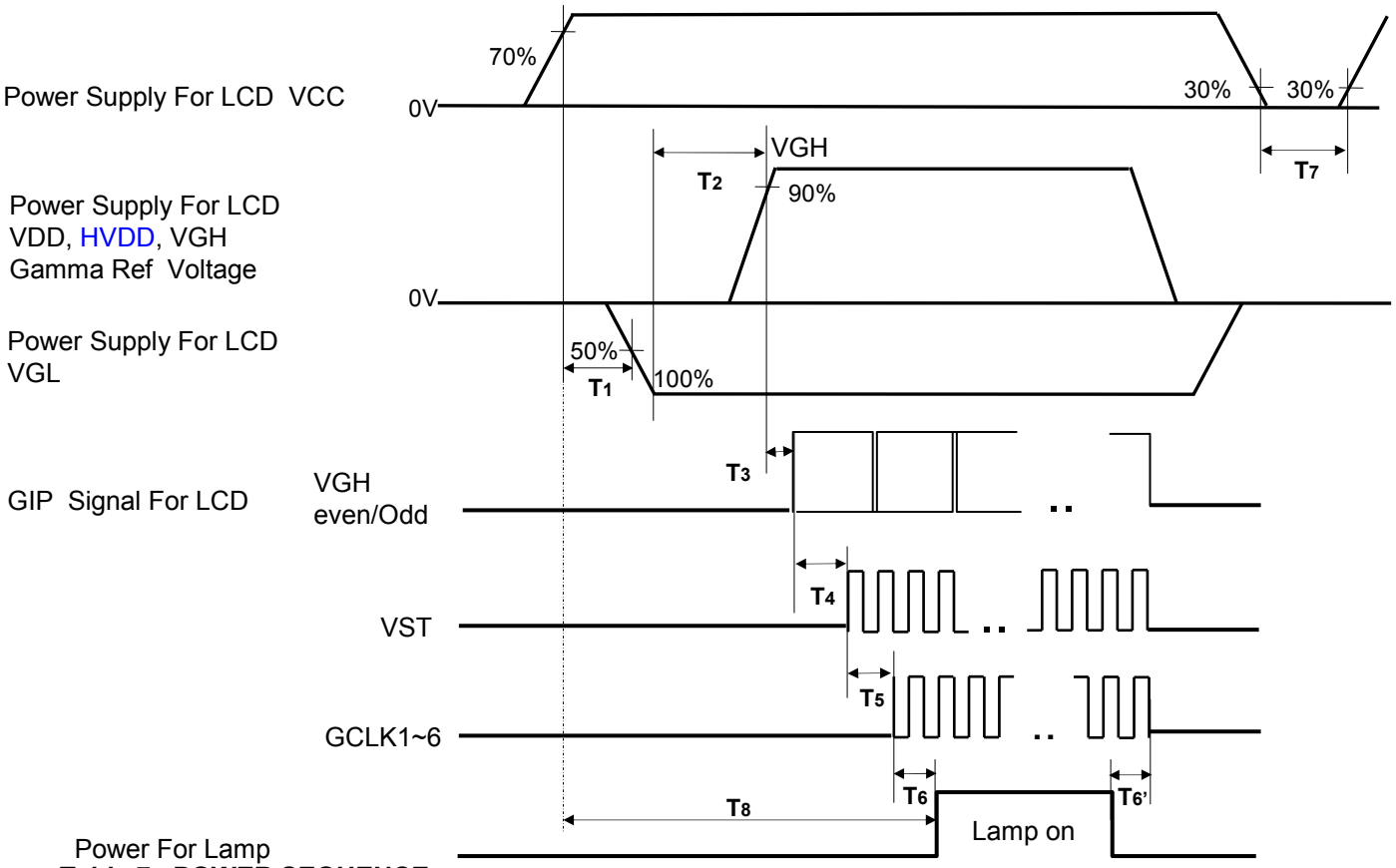


Table 7. POWER SEQUENCE

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	0.5		-	ms	
T2	0.5		-	ms	
T3	0		-	ms	
T4	10		-	ms	2
T5	0		-	ms	
T6 / T6'	20		-	ms	
T7	2		-	s	
T8	-		12	s	

Note : 1. Power sequence for Source D-IC must be kept. ※ Please refer to Appendix IV-1 for more details.
2. VGH Odd signal should be started “High” status and VGH even & odd can not be “High at the same time.
3. Power Off Sequence order is reverse of Power On Condition including Source D-IC.
4. GCLK On/Off Sequence : GCLK4 → GCLK5 →GCLK6 →GCLK1 → GCLK2 → GCLK3.
5, VDD Odd/Even transition time should be within V blank.

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable in a dark environment at 25±2°C. The values are specified at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and θ equal to 0 °.
It is presented additional information concerning the measurement equipment and method in FIG. 9.

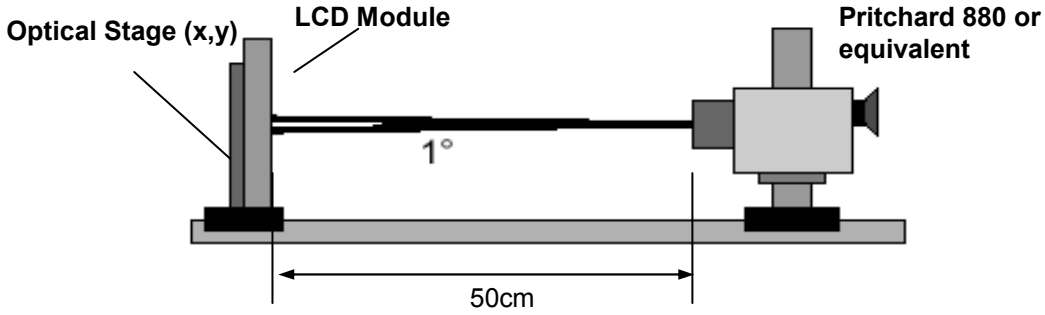


FIG. 9 Optical Characteristic Measurement Equipment and Method

Table 8. OPTICAL CHARACTERISTICS

Ta= 25±2°C, V_{LCD}=12.0V, VDD,H_VDD,VGH,VGL=typ, fv=120Hz, Dclk=74.25MHz, I_{BL1}=68 mA_{RMS} , I_{BL2}=68 $mA_{RMS,}$ I out Duty = 100%

Parameter		Symbol	Value			Unit	Note
			Min	Typ	Max		
Contrast Ratio		CR	1100	1450	-		1
Surface Luminance, white		L_{WH}	400	500	-	cd/m^2	2
Luminance Variation		δ_{WHITE} 5P	-	-	1.3		3
Response Time	Rising	Tr	-	8	12	ms	4
	Falling	Tf	-	10	14		
Color Coordinates [CIE1931]	RED	Rx	Typ -0.03	0.636	Typ +0.03		
		Ry		0.335			
	GREEN	Gx		0.291			
		Gy		0.603			
	BLUE	Bx		0.146			
		By		0.061			
	WHITE	Wx		0.279			
		Wy		0.292			
Color Temperature				10,000		K	
Color Gamut				72		%	
Viewing Angle (CR>10)							
	x axis, right(ϕ=0°)	θr	89	-	-	degree	5
	x axis, left (ϕ=180°)	θl	89	-	-		
	y axis, up (ϕ=90°)	θu	89	-	-		
	y axis, down (ϕ=270°)	θd	89	-	-		
Gray Scale			-	-	-		6

Note : 1. Contrast Ratio(CR) is defined mathematically as :

$$CR = \frac{\text{Surface Luminance at all white pixels}}{\text{Surface Luminance at all black pixels}}$$

It is measured at center 1-point.

2. Surface luminance is determined after the unit has been 'ON' and 1Hour after lighting the backlight in a dark environment at 25±2°C. Surface luminance is the luminance value at center 1-point across the LCD surface 50cm from the surface with all pixels displaying white. For more information see the FIG. 10.

3. The variation in surface luminance , δ WHITE is defined as :
δ WHITE(5P) = Maximum(L_{on1},L_{on2}, L_{on3}, L_{on4}, L_{on5}) / Minimum(L_{on1},L_{on2}, L_{on3}, L_{on4}, L_{on5})
Where L_{on1} to L_{on5} are the luminance with all pixels displaying white at 5 locations .
For more information, see the FIG. 10.

4. Response time is the time required for the display to transit from G(255) to G(0) (Rise Time, Tr_R) and from G(0) to G(255) (Decay Time, Tr_D).

5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD module surface. For more information, see the FIG. 12.

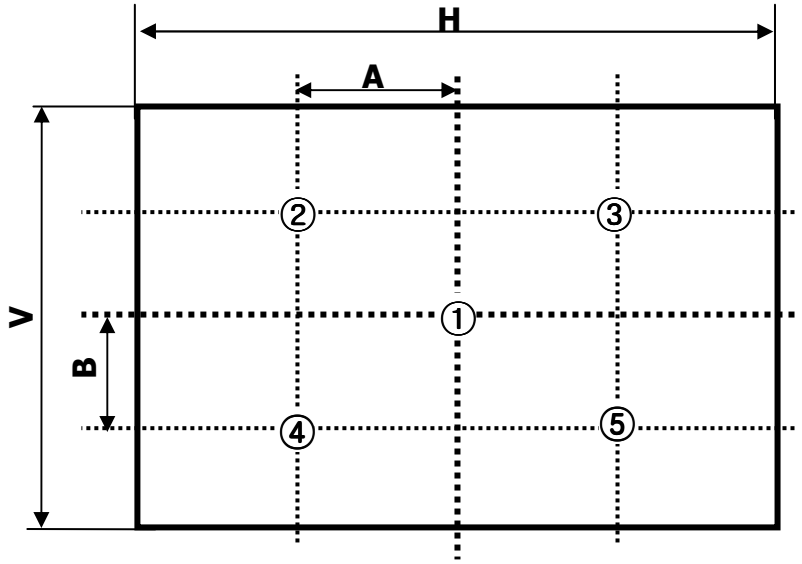
6. Gray scale specification
Gamma Value is approximately 2.2. For more information, see the Table 9.

Table 9. GRAY SCALE SPECIFICATION

Gray Level	Luminance [%] (Typ)
L0	0.067
L15	0.27
L31	1.04
L47	2.49
L63	4.68
L79	7.66
L95	11.5
L111	16.1
L127	21.6
L143	28.1
L159	35.4
L175	43.7
L191	53.0
L207	63.2
L223	74.5
L239	86.7
L255	100

	Gray Level	Gamma Ref.
Positive Voltage	L0	Gamma9
	L1	Gamma8
	L31	Gamma7
	L63	Gamma6
	L127	Gamma5
	L191	Gamma4
	L223	Gamma3
	L255	Gamma1
Negative Voltage	L255	Gamma18
	L223	Gamma16
	L191	Gamma15
	L127	Gamma14
	L63	Gamma13
	L31	Gamma12
	L1	Gamma11
	L0	Gamma10

Measuring point for surface luminance & luminance variation



A : H / 4 mm
B : V / 4 mm
@ H,V : Active Area

FIG.10 5 Points for Luminance Measure

Response time is defined as the following figure and shall be measured by switching the input signal for "Gray(N)" and "Gray(M)".

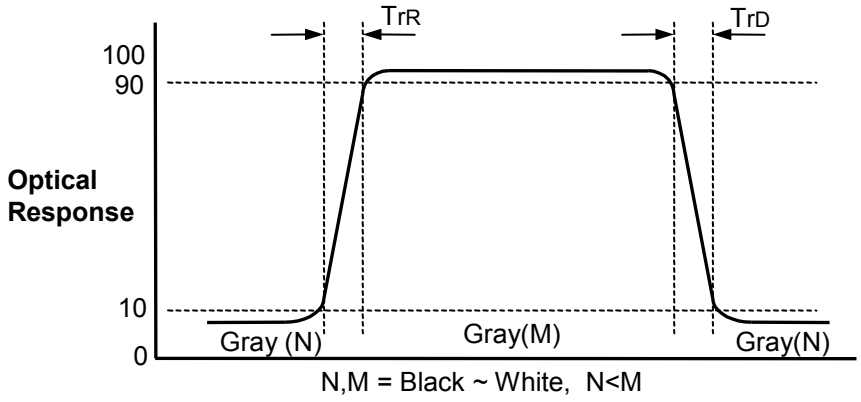


FIG.11 Response Time

Dimension of viewing angle range

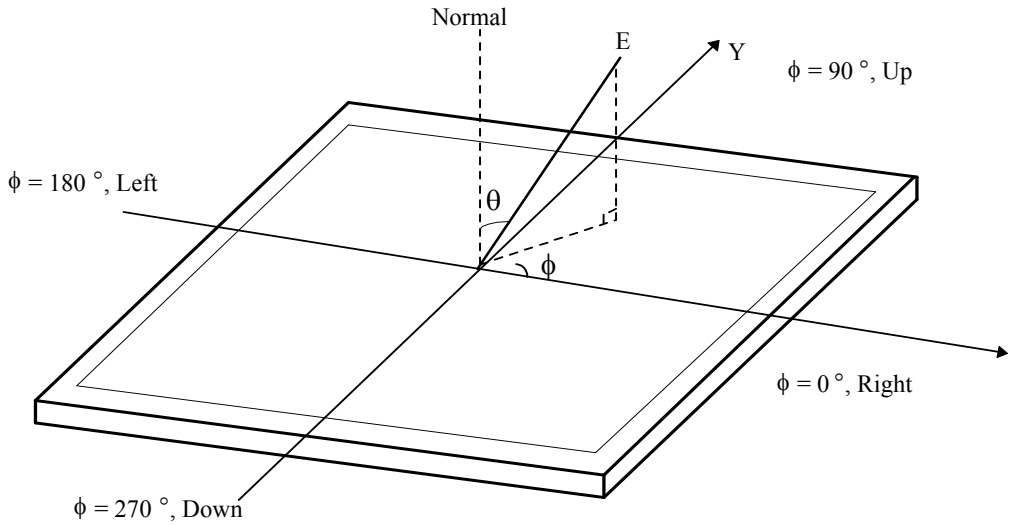


FIG.12 Viewing Angle

5. Mechanical Characteristics

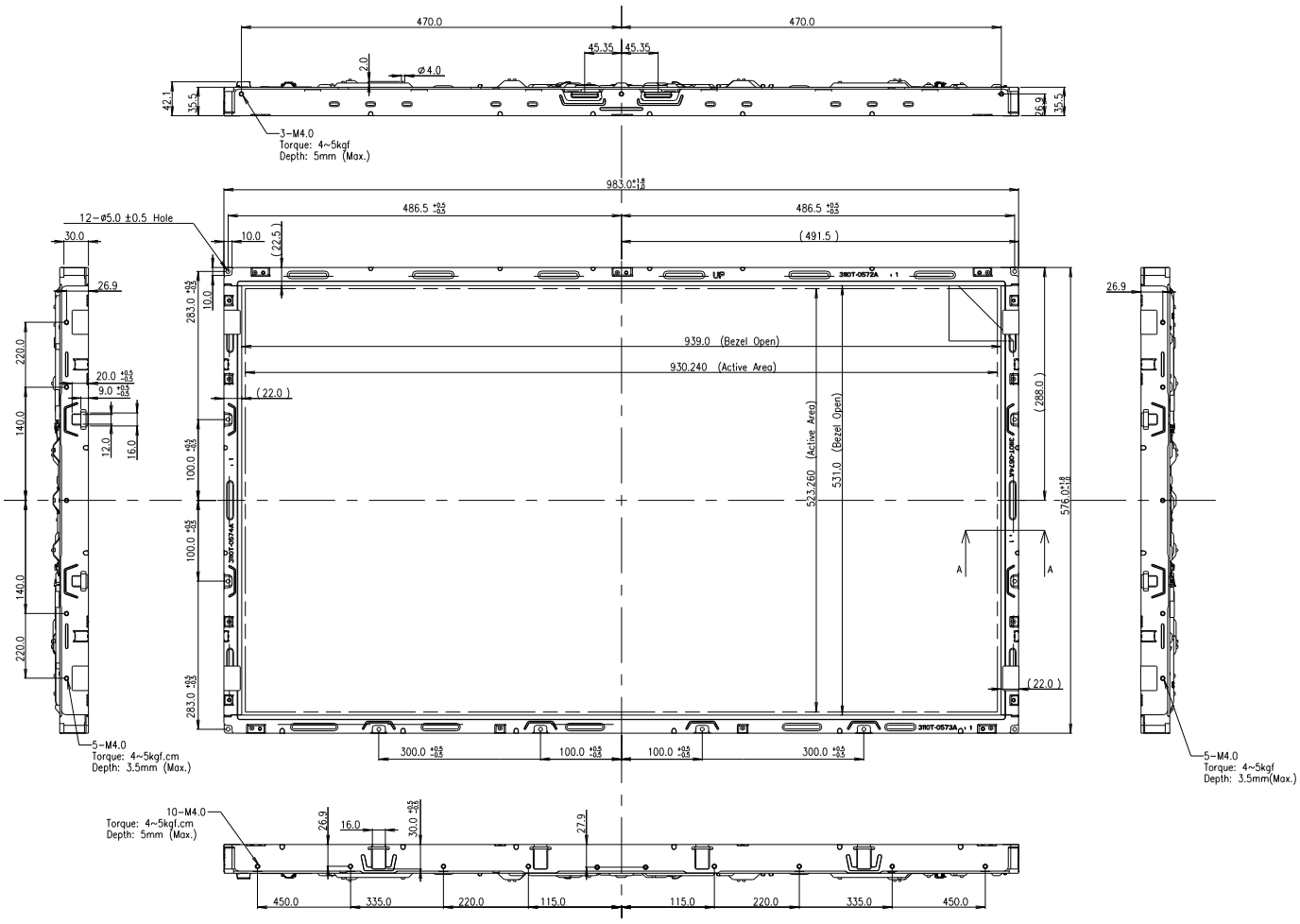
Table 10 provides general mechanical characteristics.

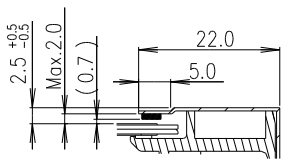
Table 10. MECHANICAL CHARACTERISTICS

Item	Value	
Outline Dimension	Horizontal	983.0 mm
	Vertical	576.0 mm
	Depth	35.5 mm
Bezel Area	Horizontal	939.0 mm
	Vertical	531.0 mm
Active Display Area	Horizontal	930.24 mm
	Vertical	523.26 mm
Weight	8.7 Kg (Typ.) , 9.6Kg (Max.)	

Note : Please refer to a mechanical drawing in terms of tolerance at the next page.

[FRONT VIEW]

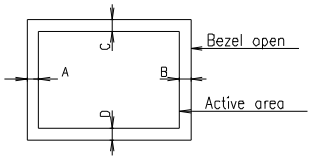




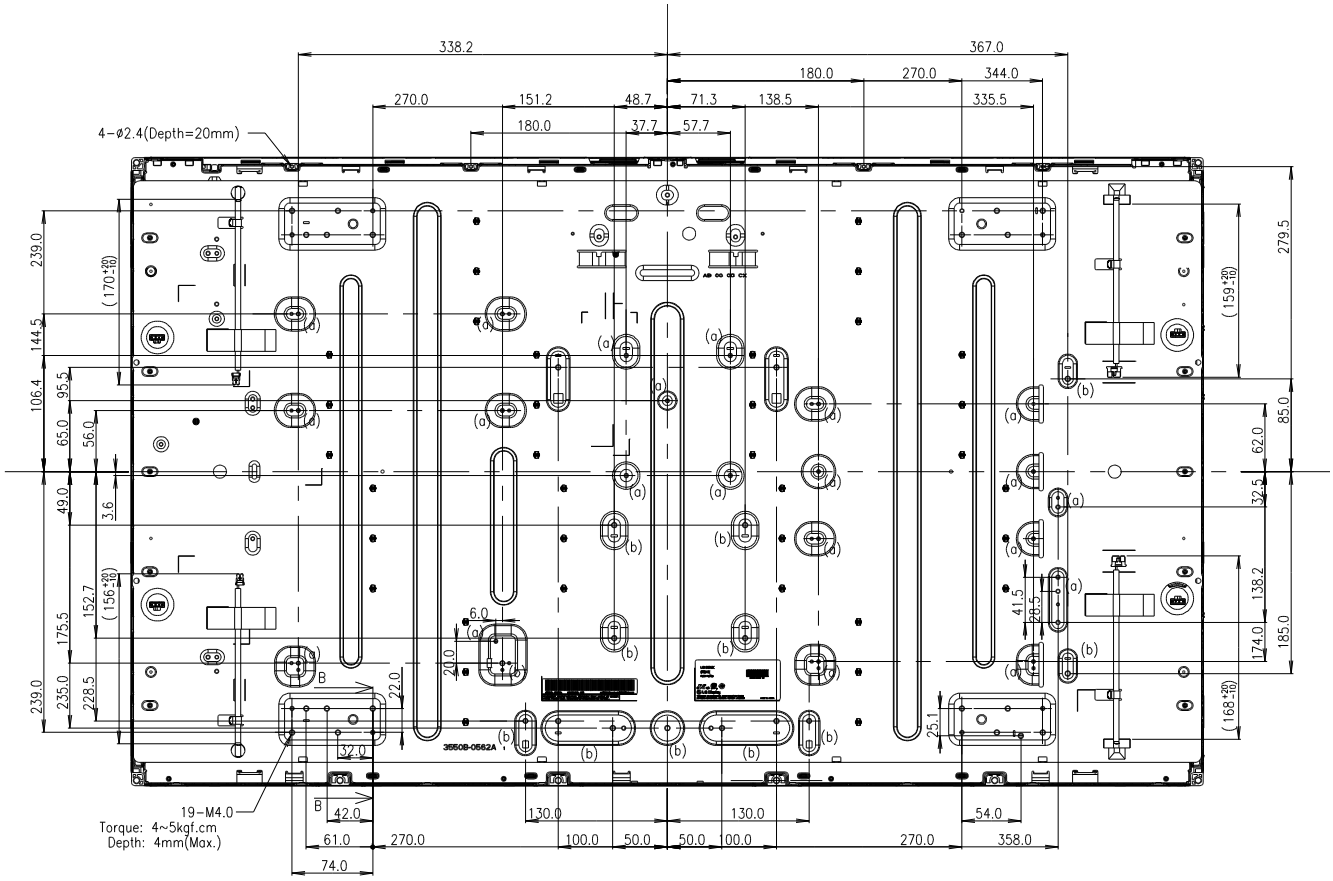
SECTION A-A
SCALE 1/1

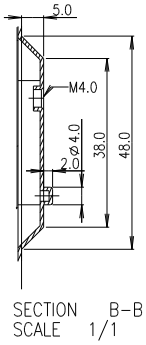
NOTES

1. Unspecified tolerances are to be ±1.0mm.
2. The length of mounting screw is MAX. 5.0mm
3. Tilt and partial disposition tolerance of display area is as following.
   (1) X-Direction : IA-BI ≤ 1.5mm
   (2) Y-Direction : IC-DI ≤ 1.5mm
4. IPB Wire Spec. : UL3239-HF VW-1, AWG#24(LS CABLE) or compatible, Rating Voltage 6kV, UL File No. : E52853 or compatible
5. IPB Connector : UL94 V-0, BDEMR-02VS(JST) or compatible, UL File No. : E60389 or compatible
6. Shrink Tube : UL94 V-1, NP-HF-TUBE, AWG#6(N.PLASTECH) or compatible, UL File No. : E321606 or compatible
7. Screw (a) : M3, Max Torque 6kgf
   Screw (b) : M4, Max Torque 8kgf



[REAR VIEW]





SECTION B-B
SCALE 1/1

6. Reliability

Table 11. ENVIRONMENT TEST CONDITION

No.	Test Item	Condition
1	High temperature storage test	Ta= 60°C 240h
2	Low temperature storage test	Ta= -20°C 240h
3	High temperature operation test	Ta= 50°C 50%RH 240h
4	Low temperature operation test	Ta= 0°C 240h
5	Vibration test (non-operating)	Wave form : random Vibration level : 1.0Grms Bandwidth : 10-300Hz Duration : X,Y,Z, 30 min Each direction per 10 min
6	Shock test (non-operating)	Shock level : 50Grms Waveform : half sine wave, 11ms Direction : ±X, ±Y, ±Z One time each direction
7	Humidity condition Operation	Ta= 40 °C ,90%RH
8	Altitude operating storage / shipment	0 - 15,000 ft 0 - 40,000 ft

Note : Before and after Reliability test, LCM should be operated with normal function.

7. International Standards

7-1. Safety

a) UL 60065, Seventh Edition, Underwriters Laboratories Inc.
Audio, Video and Similar Electronic Apparatus - Safety Requirements.

b) CAN/CSA C22.2 No.60065:03, Canadian Standards Association.
Audio, Video and Similar Electronic Apparatus - Safety Requirements.

c) EN 60065:2002 + A11:2008, European Committee for Electrotechnical Standardization (CENELEC).
Audio, Video and Similar Electronic Apparatus - Safety Requirements.

d) IEC 60065:2005 + A1:2005, The International Electrotechnical Commission (IEC).
Audio, Video and Similar Electronic Apparatus - Safety Requirements.

7-2. Environment

a) RoHS, Directive 2002/95/EC of the European Parliament and of the council of 27 January 2003

8. Packing

8-1. Information of LCM Label

a) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M

A,B,C : SIZE(INCH)
D : YEAR
E : MONTH
F ~ M : SERIAL NO.

Note

1. YEAR

Year	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
Mark	1	2	3	4	5	6	7	8	9	0

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	4	4	5	6	7	8	9	A	B	C

b) Location of Lot Mark

Serial NO. is printed on the label. The label is attached to the backside of the LCD module.
This is subject to change without prior notice.

8-2. Packing Form

a) Package quantity in one Pallet : 13 pcs

b) Pallet Size : 1150 mm X 1020 mm X 815 mm.

9. Precautions

Please pay attention to the followings when you use this TFT LCD module.

9-1. Mounting Precautions

(1) You must mount a module using specified mounting holes (Details refer to the drawings).
(2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
(4) You should adopt radiation structure to satisfy the temperature specification.
(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzine. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(9) Do not open the case because inside circuits do not have sufficient strength.

9-2. Operating Precautions

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
V=±200mV(Over and under shoot voltage)
(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer
(4) Be careful for condensation at sudden temperature change.Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.
(7) Please do not give any mechanical and/or acoustical impact to LCM. Otherwise, LCM can't be operated its full characteristics perfectly.
(8) A screw which is fastened up the steels should be a machine screw.
(if not, it can causes conductive particles and deal LCM a fatal blow)
(9) Please do not set LCD on its edge.
(10) The conductive material and signal cables are kept away from transformers to prevent abnormal display, sound noise and temperature rising.
(11) Partial darkness may happen during 3~5 minutes when LCM is operated initially in condition that luminance is under 40% at low temperature (under 5℃). This phenomenon which disappears naturally after 3~5 minutes is not a problem about reliability but LCD characteristic.

(12) Partial darkness may happen under the long-term operation of any dimming without power on/off. This phenomenon which disappears naturally after 5 minutes is not a problem about reliability but LCD characteristics.

9-3. Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9-4. Precautions for Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

9-5. Storage

When storing modules as spares for a long time, the following precautions are necessary.

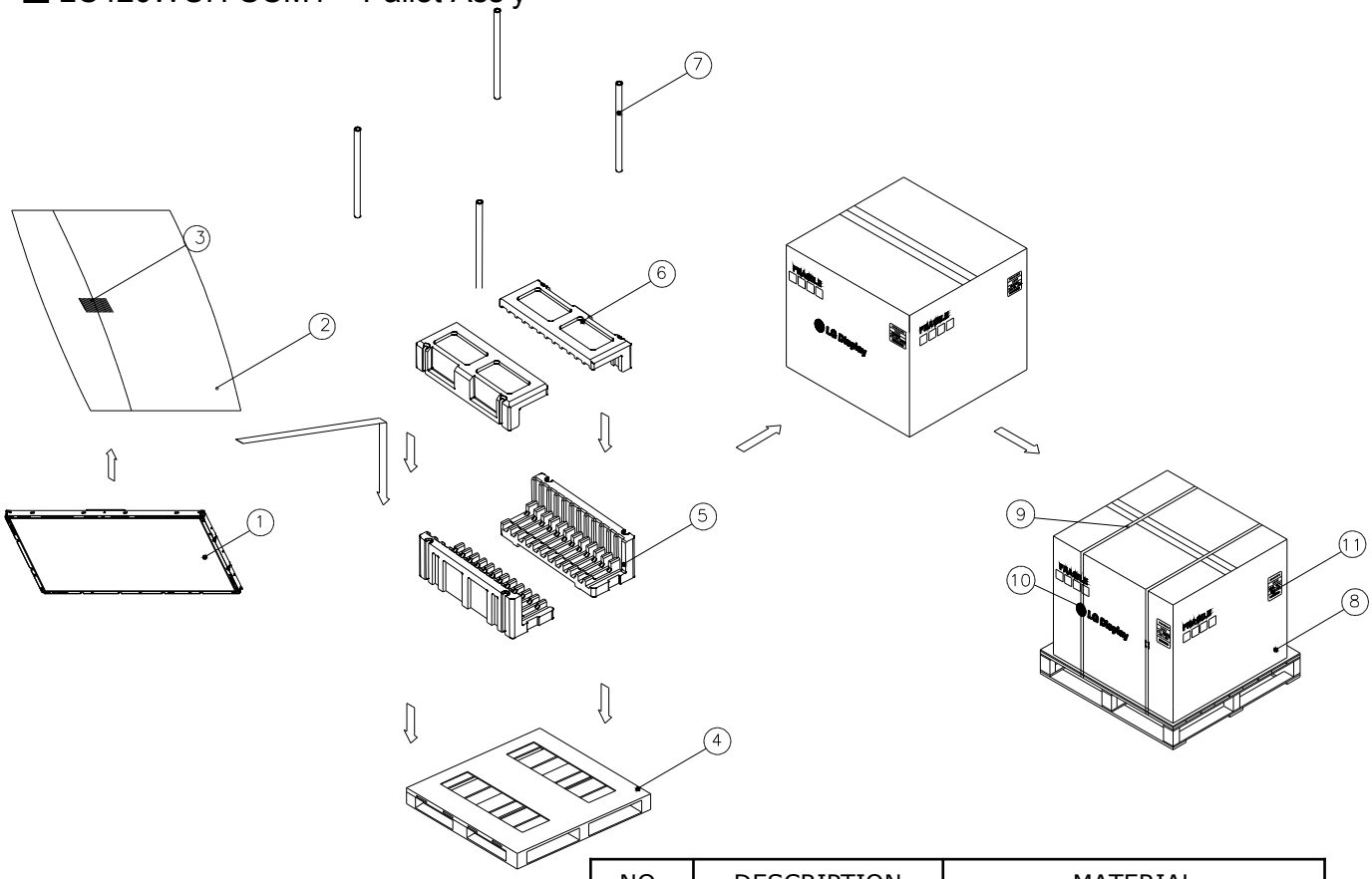
(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
(2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

9-6. Handling Precautions for Protection Film

(1) The protection film is attached to the bezel with a small masking tape.
When the protection film is peeled off, static electricity is generated between the film and polarizer.
This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
(2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.
(3) You can remove the glue easily. When the glue remains on the bezel surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

APPENDIX-I

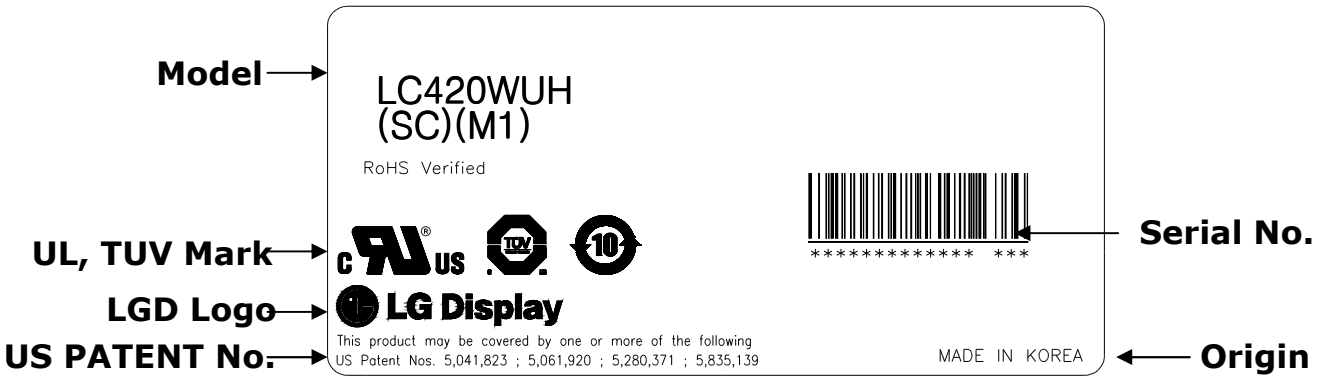
■ LC420WUH-SCM1 – Pallet Ass'y



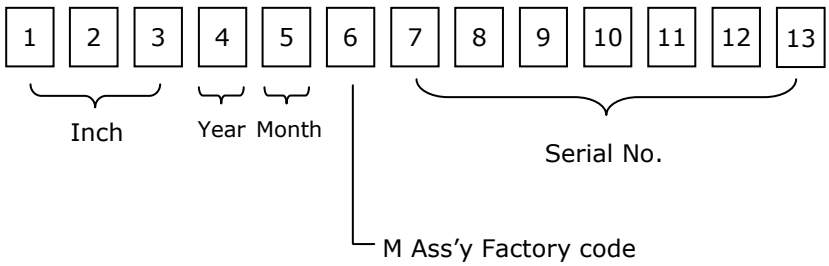
NO.	DESCRIPTION	MATERIAL
1	LCD Module	
2	BAG	42INCH
3	TAPE	MASKING 20MM X 50M
4	PALLET	Plywood (1140X990X125.5)
5	PACKING	EPS
6	PACKING	EPS
7	ANGLE PACKING	PAPER
8	ANGLE COVER	PAPER
9	BAND,CLIP	STEEL
10	BAND	PP
11	LABEL	YUPO PAPER 80G 100X100

 # APPENDIX- II

■ LC420WUH-SCM1-LCM Label

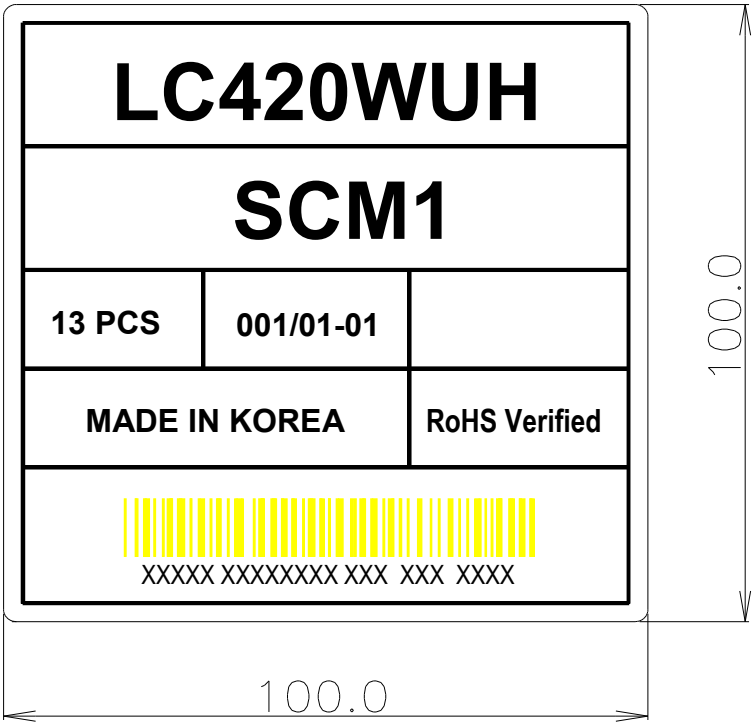


■ **Serial No. (See CAS 30 page for more information)**



 # APPENDIX- III

■ LC420WUH-SCM1-Pallet Label



APPENDIX- IV-1

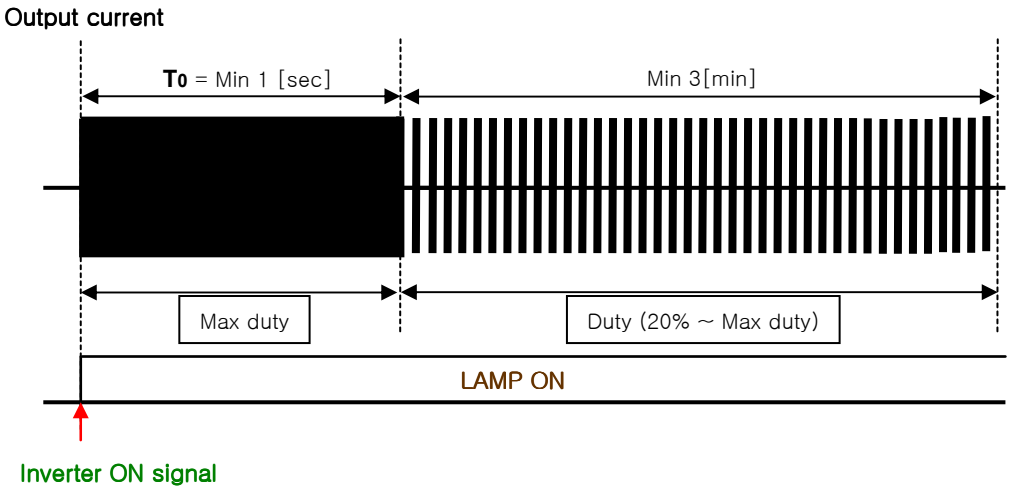
■ **Mega DCR** Using Condition (1)

● After Inverter ON, Output current max duty should be sustained during 1sec.

●The Deep Dimming means using the output current duty less than 20% duty.

The deep dimming must be used very carefully due to limitation of lamp characteristics and specification.

1) For stable lamp on, its duty condition should follow below the condition.
After Inverter ON signal, T0 duration should be sustained.



2) B/L may not satisfy some of LCM specification at the Deep Dimming.

- Duration : The Deep Dimming must be limited within 10 minutes.

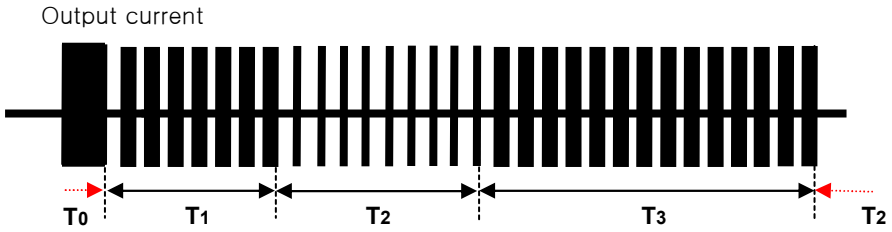
- Ratio : The operation time of the Deep Dimming must be less than 1/5 time of the Normal Duty(20%~Max duty) operation in a certain period to prevent unwanted operation.

- FOS : Partial darkness or darkness of center area during the low duty might be happened due to insufficient lamp current.

- Warm up : Normal Duty(20%~Max duty) must be used 3 min after the lamps “ON”. In case of low temperature, more warm up time may be needed.

APPENDIX- IV-2

■ **Mega DCR** Using Condition (2)



Parameter	Value			Unit	Condition
	Min	Typ	Max		
T_1	3	-	-	min	Output current Duty[20%~Max duty]
T_2	-	-	10	min	Output current Duty[0~20%]
T_3	T_2 x 5	-	-	min	Output current Duty[20%~Max duty]

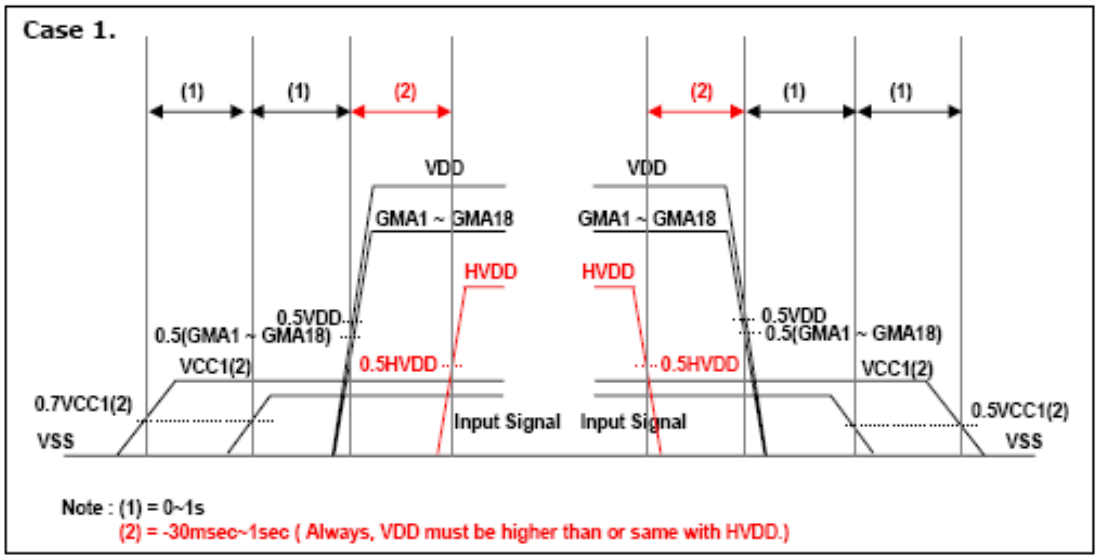
3) The output current duty may not be same as input PWM duty due to rise/fall time of output.

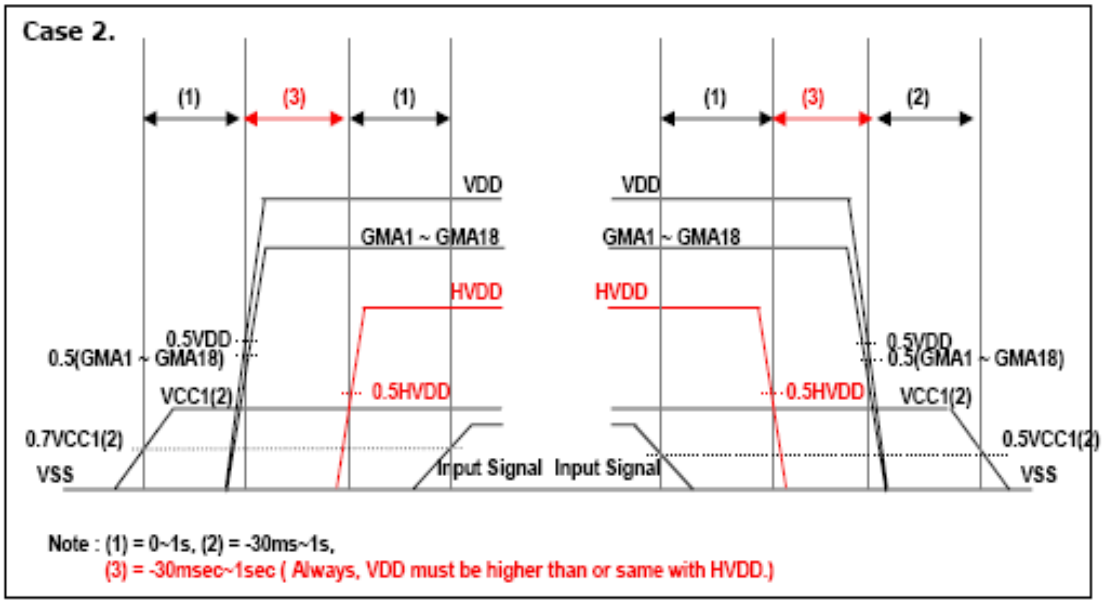
4) Following the recommended conditions as aforementioned, there is no difference of lamp lifetime between conventional method and new one.

APPENDIX- V-1

■ LC420WUH-SCM1-Source D-IC Power Sequence

-. Logic level Input Signal : SOE, POL, GSP, H_CONV, OPT_N





APPENDIX- V-2

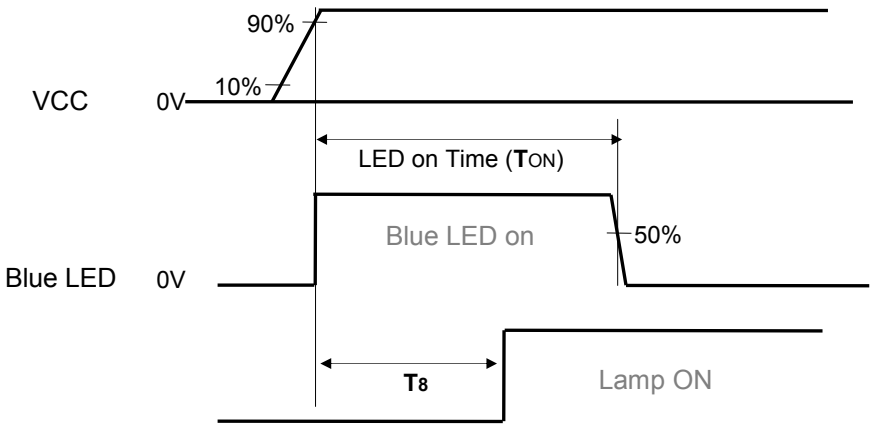
■ Blue LED On Time

This is only the reference data of Blue LED on Time for LC420WUH-SCA1 model.

1. Model : LC420WUH-SCA1

2. Test condition : VCC = 3.3V

3. Sample Size : 10pcs



4. Current Status

Sample	#1	#2	#3	#4	#5	Min	Max	Avg.
LED on Time (TON)	6.8s	8.8s	7.2s	7.4s	8.0s	6.8s	8.4s	7.7s
Sample	**#6**	**#7**	**#8**	**#9**	**#10**			
LED on Time (TON)	8.4s	8.1s	8.0s	7.3s	7.0s			

APPENDIX- V

■ Lamp Electrical Spec

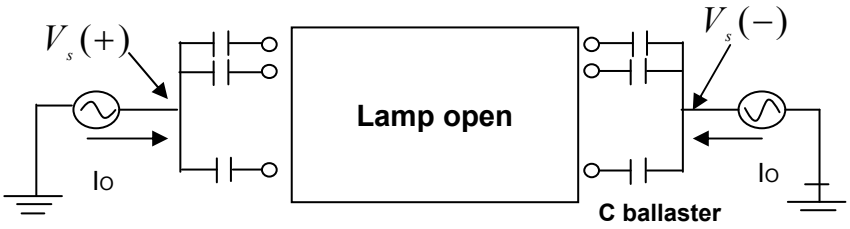
	Item	Uint	Standards(Hi-Hi)	Remark
1	Lamp Voltage (VL)	Vrms	1,630±7%, IL=3.0 mA 2,200±7%, IL=8.5 mA 2,270±7%, IL=9.0 mA	
2	Lamp Current (IL)	mArms	Min 3.0 Typ 8.5 Max 9.5	
3	Lamp Power (VL×IL)	W	4.0, IL=3.0mA 10.6, IL=8.5mA 11.3, IL=9.0mA	
4	Starting Voltage (Vs)	Vrms	2,220 Max	Ta=0℃
5	Operating Frequency	kHz	63kHz	
6	Life Time	Hrs	Min. 50,000 (at 9.0mA)	
7	Discharge Stabilization Time	Sec	180	
8	Luminance Uniformity lighted after 60 seconds	%	80 Min	

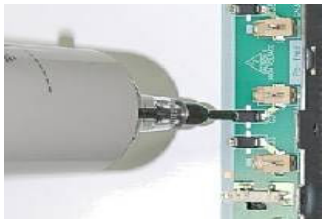
APPENDIX- VI

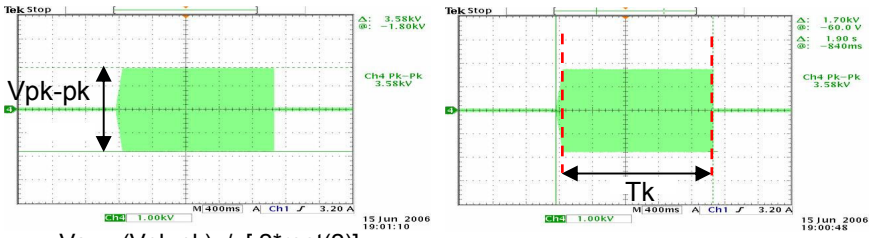
■ Starting (Striking) Voltage measurement method

※ Measure the high voltage point of Balance Ass'y after removing all lamp.

a) CCFL Cap balance Structure







Vs = (Vpk-pk) / [2*root(2)]

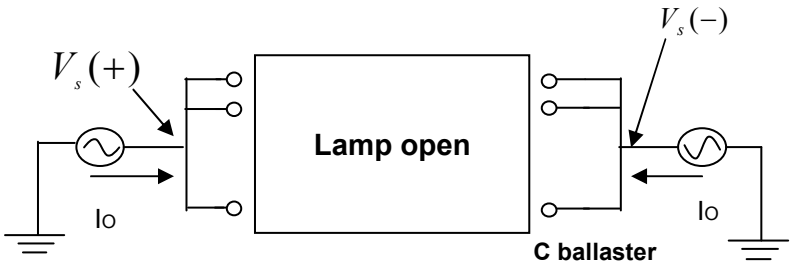
※Equipment

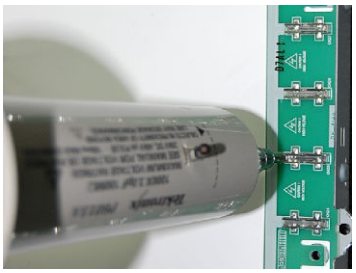
1.TDS7254B(Tek.)

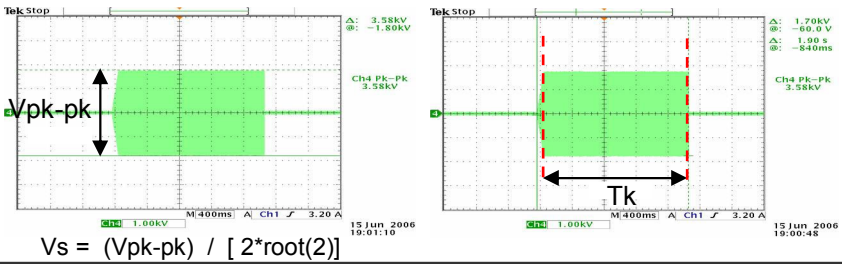
2.P6015(Tek.)

Figure 1 . CCFL Vopen

b) EEFL Structure







Vs = (Vpk-pk) / [2*root(2)]

※Equipment

1.TDS7254B(Tek.)

2.P6015(Tek.)

Figure 2 . EEFL Vopen