SPECIFICATION
FOR
APPROVAL

( ) Preliminary Specification
(●) Final Specification

Title	47.0" WUXGA TFT LCD

BUYER	LGE
LCM MODEL	LC470MUK-SCA1
SET MODEL	

SUPPLIER	LG.Display Co., Ltd.
*MODEL	LC470MUK
SUFFIX	SCA1 (RoHS Verified)

*When you obtain standard approval,
please use the above model name without suffix

APPROVED BY	SIGNATURE / DATE
/	
/	
/	

Please return 1 copy for your confirmation with your signature and comments.

APPROVED BY	SIGNATURE / DATE
P.Y. Kim / Team Leader	'10.01.07
REVIEWED BY	
Y.J. Heo / Project Leader	'10. 01. 07
PREPARED BY	
Q-H. Jo / Engineer	Jan. 7, 2010

TV Products Development Dept.
LG. Display Co., Ltd

CONTENTS

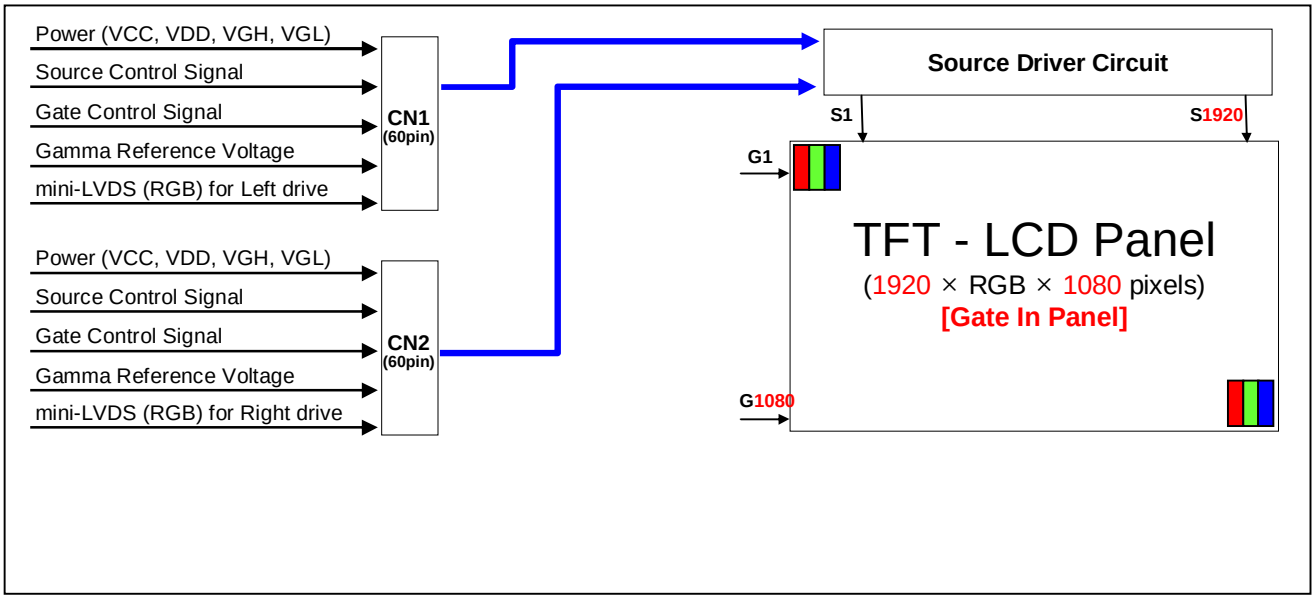
Number	ITEM	Page
	COVER	0
	CONTENTS	1
	RECORD OF REVISIONS	2
1	GENERAL DESCRIPTION	3
2	ABSOLUTE MAXIMUM RATINGS	4
3	ELECTRICAL SPECIFICATIONS	5
3-1	ELECTRICAL CHARACTERISTICS	5
3-2	INTERFACE CONNECTIONS	7
3-3	SIGNAL TIMING SPECIFICATIONS	9
3-4	DATA MAPPING AND TIMING	12
3-5	PANEL PIXEL STRUCTURE	13
3-6	POWER SEQUENCE	14
4	OPTICAL SPECIFICATIONS	15
5	MECHANICAL CHARACTERISTICS	19
6	RELIABILITY	21
7	INTERNATIONAL STANDARDS	22
7-1	ENVIRONMENT	22
8	PACKING	23
8-1	PACKING FORM	23
9	PRECAUTIONS	24
9-1	ASSEMBLY PRECAUTIONS	24
9-2	OPERATING PRECAUTIONS	24
9-3	ELECTROSTATIC DISCHARGE CONTROL	25
9-4	PRECAUTIONS FOR STRONG LIGHT EXPOSURE	25
9-5	STORAGE	25

RECORD OF REVISIONS

Revision No.	Revision Date	Page	Description
0.1	Sep. 18, 2009	-	Preliminary Specification(First Draft)
0.2	Sep. 25, 2009	7, 8	Corrected the 'MODULE CONNECTOR(CN1) PIN CONFIGURATION'
		10	Corrected the 'Last Data Latch to SOE Timing'
0.3	Nov. 13, 2009	5	Corrected the 'ELECTRICAL CHARACTERISTICS'
		29	Added the 'APPENDIX- IV'
0.4	Nov. 20, 2009	7,8	Corrected the 'LCD Connector (CN1) and (CN2)'
0.5	Dec. 30, 2009	5	Changed the 'ELECTRICAL CHARACTERISTICS' and the 'Note'
		7,8	Modified the 'MODULE CONNECTOR(CN1, CN2) PIN CONFIGURATION' for normal operation.
		7,8	Modified the 'Note' for 'MODULE CONNECTOR(CN1, CN2) PIN CONFIGURATION'
		14	Modified the 'Note' for 'POWER SEQUENCE'
		15	Added the 'Color Coordinates' in 'Table 6'
0.6	Jan. 7, 2010	5	Modified the 'Common Voltage'
1.0	Jan. 7, 2010	-	Final Specification

1. General Description

The LC470MUK is a Color Active Matrix Liquid Crystal Display with an integral the Source PCB and Gate implanted on Panel (GIP). The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally black mode. It has a 46.96 inch diagonally measured active display area with WUXGA resolution (1080 vertical by 1920 horizontal pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the luminance of the sub-pixel color is determined with a 8-bit gray scale signal for each dot. Therefore, it can present a palette of more than 16.7M(true) colors.
It is intended to support LCD TV, PCTV where high brightness, super wide viewing angle, high color gamut, high color depth and fast response time are important.



General Features

Active Screen Size	46.96 inches(1192.78mm) diagonal
Outline Dimension	1061.8 (H) x 606.8 (V) x 1.8 (D) mm (Typ.)
Pixel Pitch	0.5415 mm x 0.5415 mm
Pixel Format	1920 horiz. by 1080 vert. Pixels, RGB stripe arrangement
Color Depth	8-bit, 16.7 M colors
Drive IC Data Interface	Source D-IC : 8-bit mini-LVDS, gamma reference voltage, and control signals Gate D-IC : Gate In Panel
Viewing Angle (CR>10)	Viewing angle free (R/L 178 (Min.), U/D 178 (Min.))
Weight	2.50Kg (Typ.)
Display Mode	Transmissive mode, Normally black
Surface Treatment (Top)	Hard coating(3H), Anti-glare treatment (Haze **10**%)

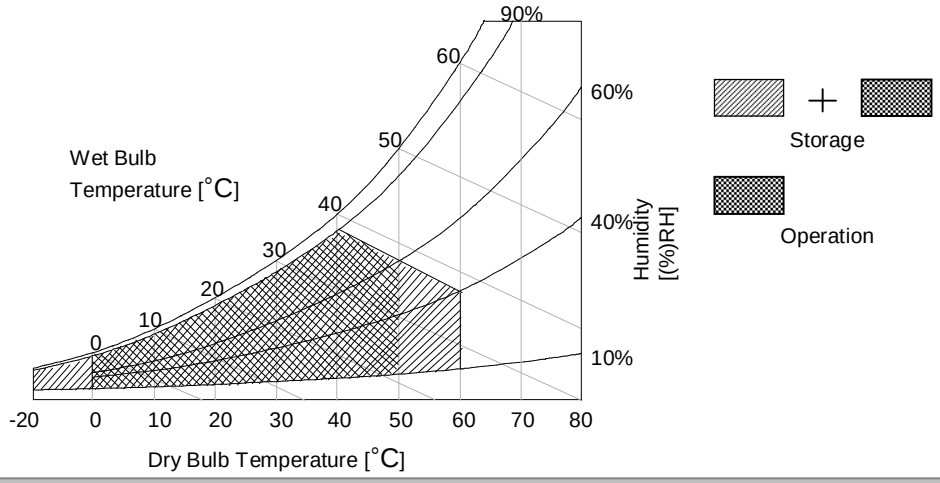
2. Absolute Maximum Ratings

The following items are maximum values which, if exceeded, may cause faulty operation or damage to the LCD module.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value		Unit	Note
		Min	Max		
Logic Power Voltage	VCC	-0.5	+4.0	VDC	1
Gate High Voltage	VGH	+18.0	+30.0	VDC	
Gate Low Voltage	VGL	-8.0	-4.0	VDC	
Source D-IC Analog Voltage	VDD	-0.3	+18.0	VDC	
Gamma Ref. Voltage (Upper)	VGMH	½VDD-0.5	VDD+0.5	VDC	
Gamma Ref. Voltage (Low)	VGML	-0.3	½ VDD+0.5	VDC	
Panel Front Temperature	TSUR	-	+68	˚C	4
Operating Temperature	TOP	0	+50	˚C	2,3
Storage Temperature	TST	-20	+60	˚C	
Operating Ambient Humidity	HOP	10	90	%RH	
Storage Humidity	HST	10	90	%RH	

Note: 1. Ambient temperature condition (Ta = 25 ± 2 ˚C)
2. Temperature and relative humidity range are shown in the figure below. Wet bulb temperature should be Max 39 ˚C and no condensation of water.
3. Gravity mura can be guaranteed below 40℃ condition.
4. The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 68 ℃ with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 68 ℃. The range of operating temperature may degrade in case of improper thermal management in final product design.



3. Electrical Specifications

3-1. Electrical Characteristics

It requires several power inputs. The VCC is the basic power of LCD Driving power sequence, Which is used to logic power voltage of Source D-IC and GIP.

Table 2. ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Note
Logic Power Voltage	VCC	-	3.0	3.3	3.6	VDC	
Logic High Level Input Voltage	VIH		2.7		VCC	VDC	
Logic Low Level Input Voltage	VIL		0		0.6	VDC	
Source D-IC Analog Voltage	VDD	-	15.3	15.5	15.7	VDC	
Half Source D-IC Analog Voltage	H_VDD	-	7.45	7.68	7.82	VDC	7
Gamma Reference Voltage	V_{GMH}	(GMA1 ~ GMA9)	½*VDD		VDD-0.2		
	V_{GML}	(GMA10 ~ GMA18)	0.2		½*VDD		
Common Voltage	Vcom	Normal	6.47	6.77	7.07	V	
		Reverse	6.47	6.77	7.07	V	
Mini-LVDS Clock frequency	CLK	3.0V≤VCC ≤3.6V			312	MHz	
mini-LVDS input Voltage (Center)	VIB	Mini-LVDS Clock and Data	0.7 + (VID/2)		(VCC-1.2) − VID / 2	V	5
mini-LVDS input Voltage Distortion (Center)	ΔVIB				0.8	V	
mini-LVDS differential Voltage range	VID		150		800	mV	
mini-LVDS differential Voltage range Dip	ΔVID		25		800	mV	
Gate High Voltage	VGH	@ 25℃	27.7	28	28.3	VDC	
		@ 0℃	28.7	29	29.3	VDC	
Gate Low Voltage	VGL		-5.2	-5.0	-4.8	VDC	
GIP Bi-Scan Voltage	VGI_P VGI_N	-	VGL	-	VGH	VDC	
GIP Refresh Voltage	VGH even/odd	-	VGL	-	VGH	V	
GIP Start Pulse Voltage	VST	-	VGL	-	VGH	V	
GIP Operating Clock	GCLK	-	VGL	-	VGH	V	
Total Power Current	ILCD	-		800	1040	mA	2
Total Power Consumption	PLCD	-		8.53	11.09	Watt	2

Note: 1. The specified current and power consumption are under the V_{LCD}=12V., 25 ± 2°C, f_V=120Hz condition whereas mosaic pattern(8 x 6) is displayed and f_V is the frame frequency.
2. The above spec is based on the basic model.
3. All of the typical gate voltage should be controlled within 1% voltage level
4. Ripple voltage level is recommended under 10%
5. In case of mini-LVDS signal spec, refer to Fig 2 for the more detail.
6. Logic Level Input Signal : SOE,POL,GSP,H_CONV,OPT_N
7. HVDD Voltage level is half of VDD and it should be between Gamma9 and Gamma10.

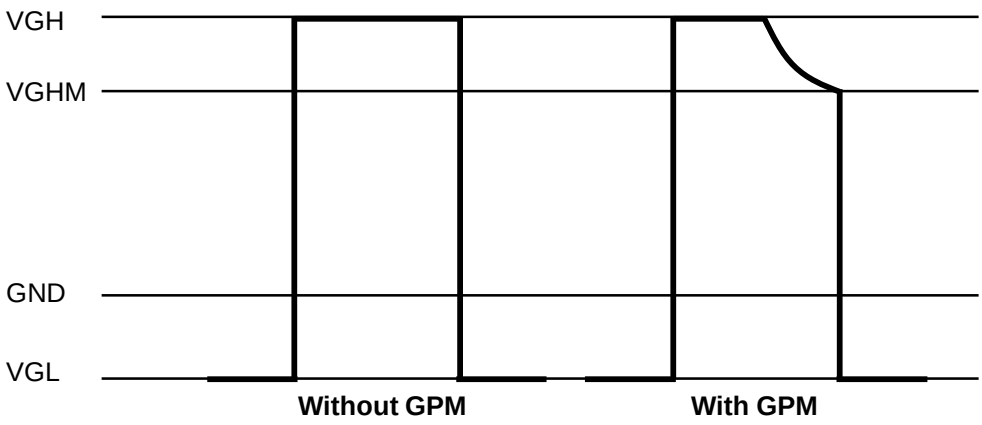


FIG. 1 Gate Output Wave form without GPM and with GPM

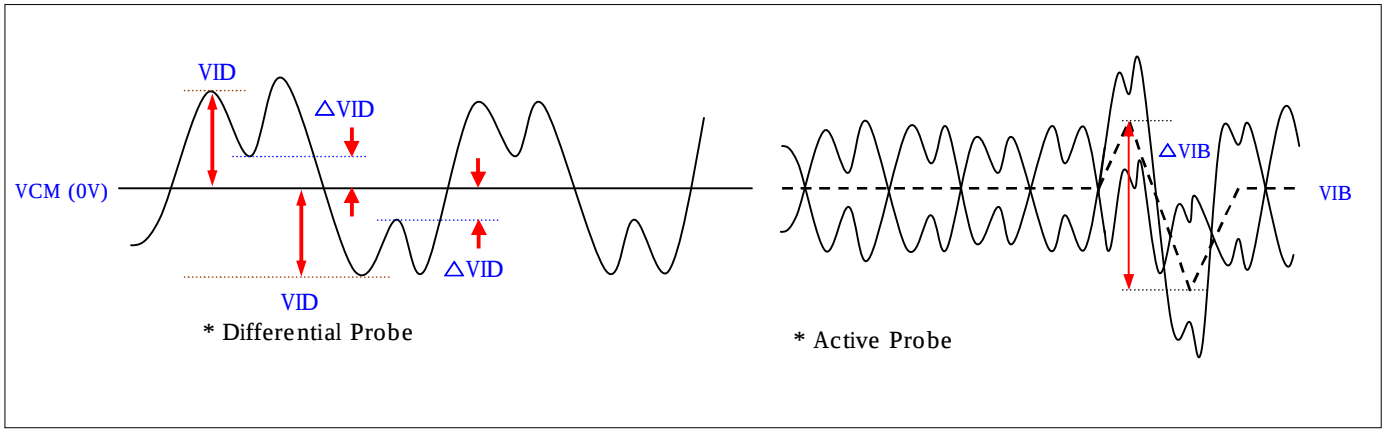


FIG. 2 Description of VID, ΔVIB, ΔVID

* Source PCB

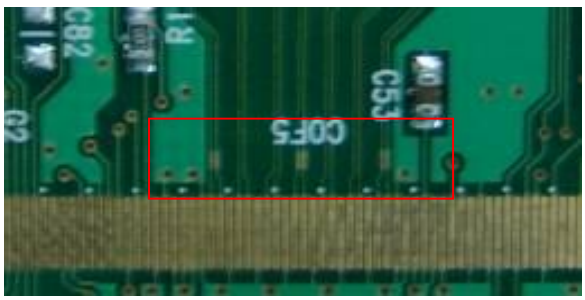


FIG. 3 Measure point

3-2. Interface Connections

This LCD panel employs two kinds of interface connection, two 60-pin FFC connector are used for the module electronics.

3-2-1. LCD Module

-LCD Connector (CN1): TF06L-60S-0.5SH (Manufactured by HRS) or Equivalent

Table 4-1. MODULE CONNECTOR(CN1) PIN CONFIGURATION

No	Symbol	Description	No	Symbol	Description
1	GND	Ground	31	LLV3 -	Left Mini LVDS Receiver Signal(3-)
2	LTD_OUT	LTD OUTPUT	32	LLV3 +	Left Mini LVDS Receiver Signal(3+)
3	GCLK1	GIP GATE Clock 1	33	LCLK -	Left Mini LVDS Receiver Clock Signal(-)
4	GCLK2	GIP GATE Clock 2	34	LCLK +	Left Mini LVDS Receiver Clock Signal(+)
5	GCLK3	GIP GATE Clock 3	35	LLV2 -	Left Mini LVDS Receiver Signal(2-)
6	GCLK4	GIP GATE Clock 4	36	LLV2 +	Left Mini LVDS Receiver Signal(2+)
7	GCLK5	GIP GATE Clock 5	37	LLV1 -	Left Mini LVDS Receiver Signal(1-)
8	GCLK6	GIP GATE Clock 6	38	LLV1 +	Left Mini LVDS Receiver Signal(1+)
9	VGI_N	GIP Bi-Scan (Normal =VGL Rotate = VGH)	39	LLV0 -	Left Mini LVDS Receiver Signal(0-)
10	VGI_P	GIP Bi-Scan (Normal =VGH Rotate = VGL)	40	LLV0 +	Left Mini LVDS Receiver Signal(0+)
11	VGH_ODD	GIP Panel VDD for Odd GATE TFT	41	GND	Ground
12	VGH_EVEN	GIP Panel VDD for Even GATE TFT	42	SOE	Source Output Enable SIGNAL
13	VGL	GATE Low Voltage	43	POL	Polarity Control Signal
14	VST	VERTICAL START PULSE	44	GSP	GATE Start Pulse
15	GND	Ground	45	H_CONV	"H“ H 2dot Inversion/ "L" H 1dot Inversion
16	VCOM_L_FB	VCOM Left Feed-Back Output	46	OPT_N	“H” Normal Display / “L” Rotation Display
17	VCOM_L	VCOM Left Input	47	GND	Ground
18	GND	Ground	48	GMA 18	GAMMA VOLTAGE 18 (Output From LCD)
19	VDD	Driver Power Supply Voltage	49	GMA 16	GAMMA VOLTAGE 16
20	VDD	Driver Power Supply Voltage	50	GMA 15	GAMMA VOLTAGE 15
21	H_VDD	Half Driver Power Supply Voltage	51	GMA 14	GAMMA VOLTAGE 14
22	H_VDD	Half Driver Power Supply Voltage	52	GMA 12	GAMMA VOLTAGE 12
23	GND	Ground	53	GMA 10	GAMMA VOLTAGE 10 (Output From LCD)
24	VCC	Logic Power Supply Voltage	54	GMA 9	GAMMA VOLTAGE 9 (Output From LCD)
25	VCC	Logic Power Supply Voltage	55	GMA 7	GAMMA VOLTAGE 7
26	GND	Ground	56	GMA 5	GAMMA VOLTAGE 5
27	LLV5 -	Left Mini LVDS Receiver Signal(5-)	57	GMA 4	GAMMA VOLTAGE 4
28	LLV5 +	Left Mini LVDS Receiver Signal(5+)	58	GMA 3	GAMMA VOLTAGE 3
29	LLV4 -	Left Mini LVDS Receiver Signal(4-)	59	GMA 1	GAMMA VOLTAGE 1 (Output From LCD)
30	LLV4 +	Left Mini LVDS Receiver Signal(4+)	60	GND	Ground

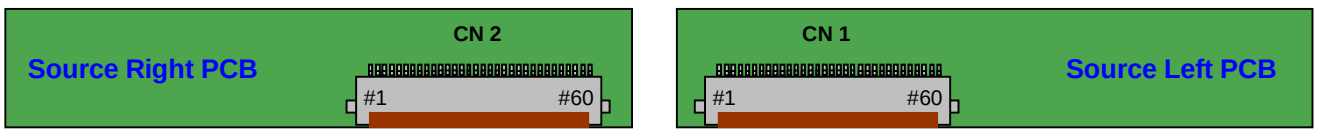
Note : 1. Please refer to application note for details.
(**GIP** & **Half VDD & Gamma Voltage & H_CONV setting**)
2. These 'input signal' (OPT_N,H_CONV) should be connected.

-LCD Connector (CN2): TF06L-60S-0.5SH(Manufactured by HRS) or Equivalent

Table 4-2. MODULE CONNECTOR(CN2) PIN CONFIGURATION

No	Symbol	Description		No	Symbol	Description
1	GND	Ground		31	RLV1 -	Right Mini LVDS Receiver Signal(1-)
2	GMA 1	GAMMA VOLTAGE 1 (Output From LCD)		32	RLV1 +	Right Mini LVDS Receiver Signal(1+)
3	GMA 3	GAMMA VOLTAGE 3		33	RLV0 -	Right Mini LVDS Receiver Signal(0-)
4	GMA 4	GAMMA VOLTAGE 4		34	RLV0 +	Right Mini LVDS Receiver Signal(0+)
5	GMA 5	GAMMA VOLTAGE 5		35	GND	Ground
6	GMA 7	GAMMA VOLTAGE 7		36	VCC	Logic Power Supply Voltage
7	GMA 9	GAMMA VOLTAGE 9 (Output From LCD)		37	VCC	Logic Power Supply Voltage
8	GMA 10	GAMMA VOLTAGE 10 (Output From LCD)		38	GND	Ground
9	GMA 12	GAMMA VOLTAGE 12		39	H_VDD	Half Driver Power Supply Voltage
10	GMA 14	GAMMA VOLTAGE 14		40	H_VDD	Half Driver Power Supply Voltage
11	GMA 15	GAMMA VOLTAGE 15		41	VDD	Driver Power Supply Voltage
12	GMA 16	GAMMA VOLTAGE 16		42	VDD	Driver Power Supply Voltage
13	GMA 18	GAMMA VOLTAGE 18 (Output From LCD)		43	GND	Ground
14	GND	Ground		44	VCOM_R	VCOM Right Input
15	OPT_N	“H” Normal Display / “L” Rotation Display		45	VCOM_R_FB	VCOM Right Feed-Back Output
16	H_CONV	"H“ H 2dot Inversion/ "L" H 1dot Inversion		46	GND	Ground
17	GSP	GATE Start Pulse		47	VST	VERTICAL START PULSE
18	POL	Polarity Control Signal		48	VGL	GATE Low Voltage
19	SOE	Source Output Enable SIGNAL		49	VGH_EVEN	GIP Panel VDD for Even GATE TFT
20	GND	Ground		50	VGH_ODD	GIP Panel VDD for Odd GATE TFT
21	RLV5 -	Right Mini LVDS Receiver Signal(5-)		51	VGI_P	GIP Bi-Scan (Normal =VGH Rotate = VGL)
22	RLV5 +	Right Mini LVDS Receiver Signal(5+)		52	VGI_N	GIP Bi-Scan (Normal =VGL Rotate = VGH)
23	RLV4 -	Right Mini LVDS Receiver Signal(4-)		53	GCLK6	GIP GATE Clock 6
24	RLV4 +	Right Mini LVDS Receiver Signal(4+)		54	GCLK5	GIP GATE Clock 5
25	RLV3 -	Right Mini LVDS Receiver Signal(3-)		55	GCLK4	GIP GATE Clock 4
26	RLV3 +	Right Mini LVDS Receiver Signal(3+)		56	GCLK3	GIP GATE Clock 3
27	LCLK -	Right Mini LVDS Receiver Clock Signal(-)		57	GCLK2	GIP GATE Clock 2
28	LCLK +	Right Mini LVDS Receiver Clock Signal(+)		58	GCLK1	GIP GATE Clock 1
29	RLV2 -	Right Mini LVDS Receiver Signal(2-)		59	LTD_OUT	LTD OUTPUT
30	RLV2 +	Right Mini LVDS Receiver Signal(2+)		60	GND	Ground

Note : 1. Please refer to application note for details.
(**GIP** & **Half VDD & Gamma Voltage & H_CONV setting**)
2. These 'input signal' (OPT_N,H_CONV) should be connected.



3-3. Signal Timing Specifications

Table 6. Timing Requirements

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Mini Clock pulse period	T_1		3.2	3.4		ns	1
Mini Clock pulse low period	T_2		1.6	-	-	ns	
Mini Clock pulse high period	T_3		1.6	-	-	ns	
Mini Data setup time	T_6		0.6	-	-	ns	
Mini Data hold time	T_7		0.6	-	-	ns	
Reset low to SOE rising time	T_8		0	-	-	ns	
SOE to Reset input time	T_9		200	-	-	ns	
Receiver off to SOE timing	T_{10}		10	-	-	CLK cycle	
POL signal to SOE setup time	T_{11}		-5	-	-	ns	
POL signal to SOE hold time	T_{12}		6	-	-	ns	
Reset High Period	T_{13}		3			CLK cycle	
SOE signal GSP setup time	T_{14}		100			ns	
SOE signal GSP Hold time	T_{15}		100			ns	
SOE signal Pulse Width	T_{16}		200			ns	

Note : 1. Mini-LVDS timing measure conditions
: 268MHz < Clock Frequency < 312MHz , 150mV < VID < 800mV @ 3.0<VCC<3.3
2. Setup time and hold time couldn't be satisfied at the same time

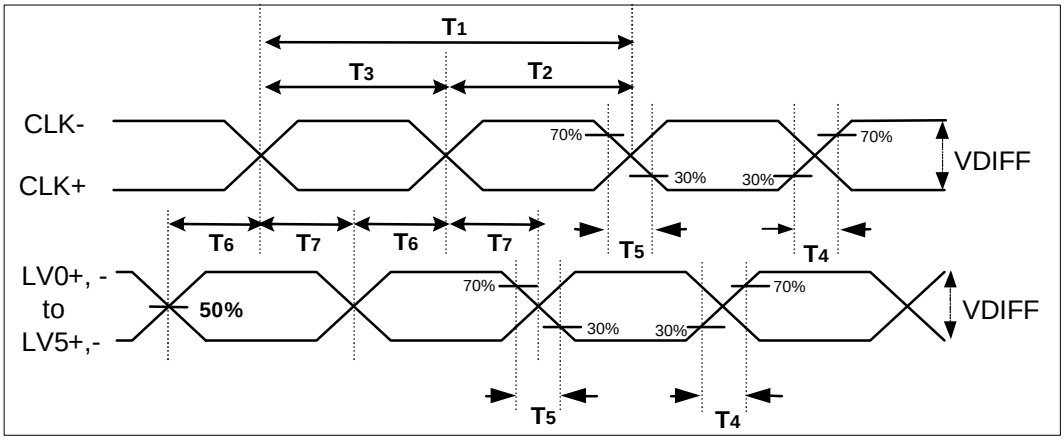


FIG 4. Source D-IC Input Data Latch Timing Waveform

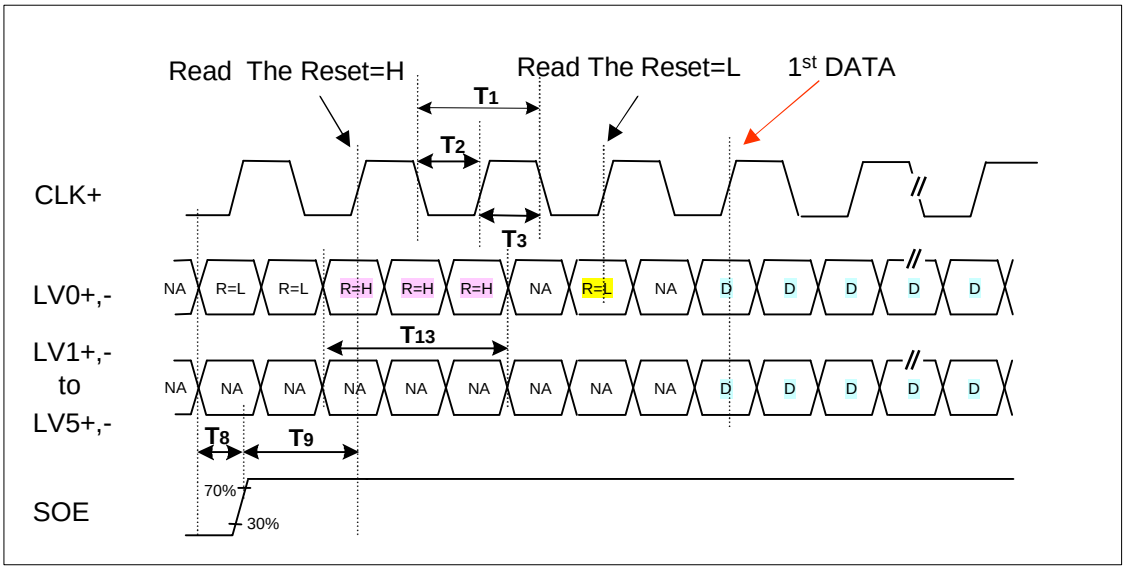


FIG 5-1. Input Data Timing for 1st Source D-IC Chip

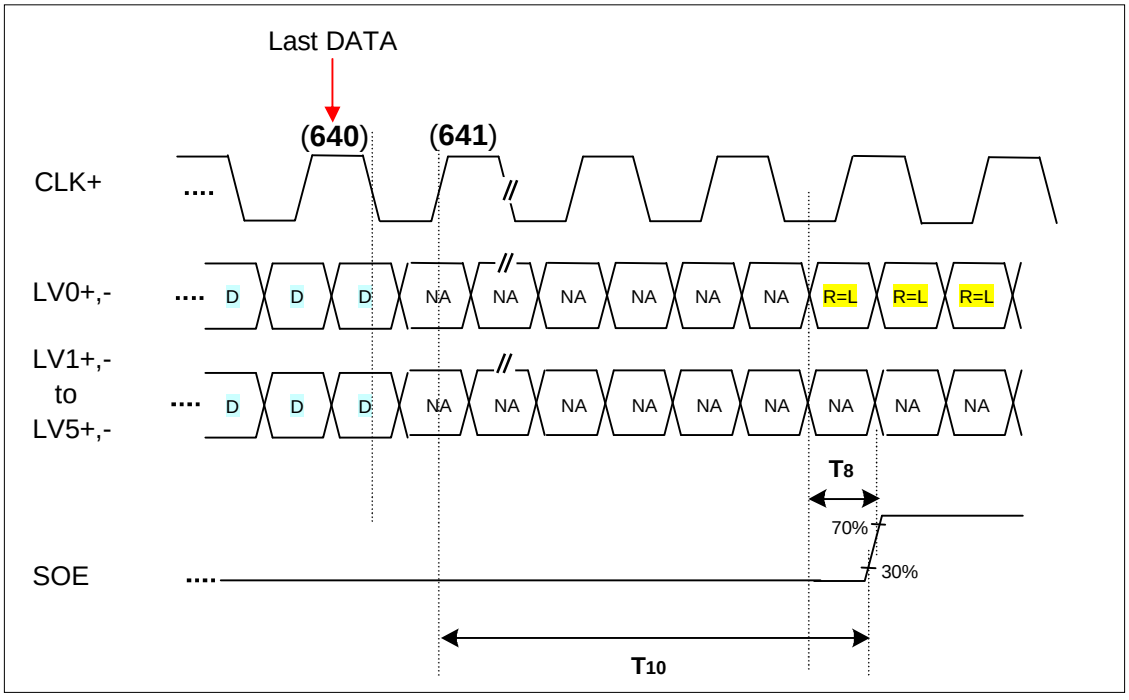


FIG 5-2. Last Data Latch to SOE Timing

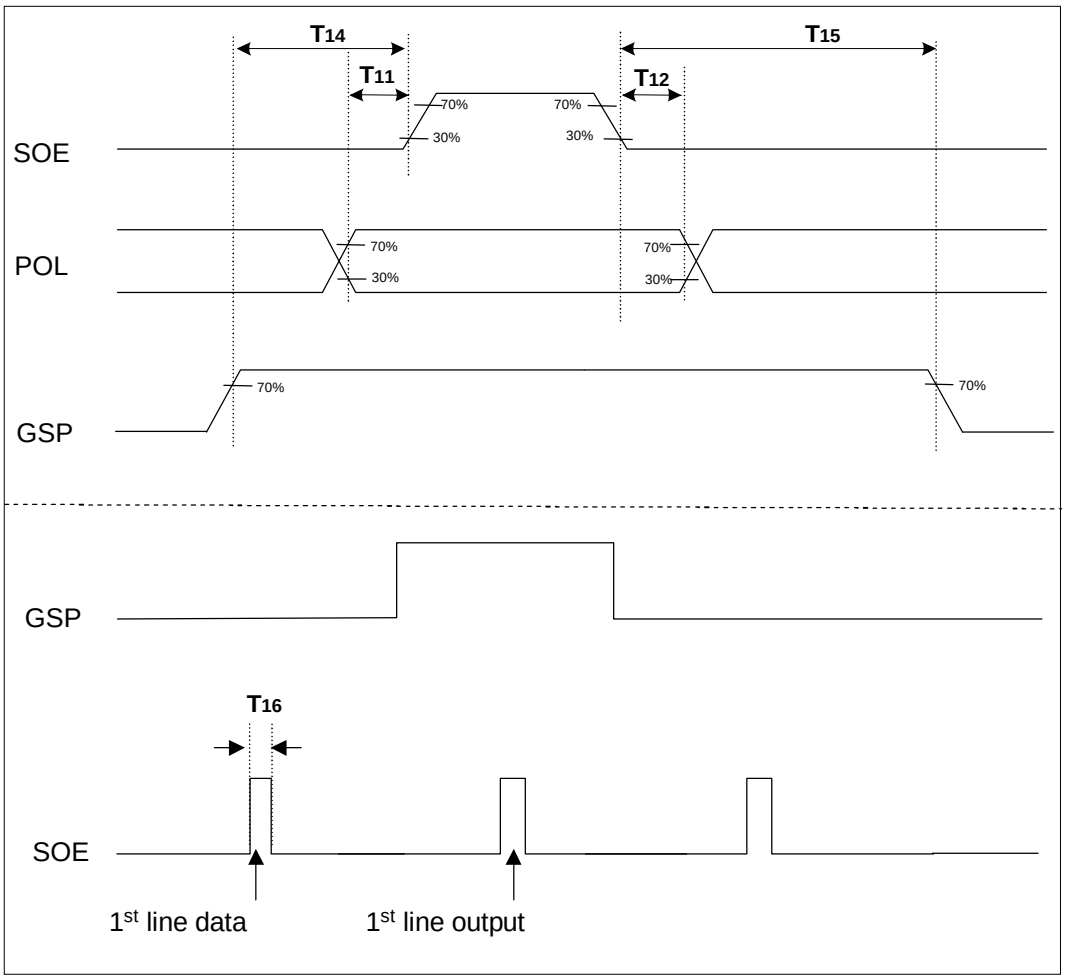
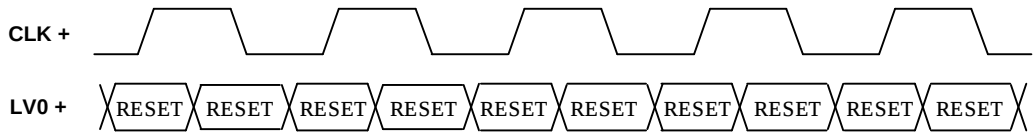


FIG 6. POL, GSP and SOE Timing Waveform

3-4. Data Mapping and Timing

Display data and control signal (RESET) are input to **LV0** to **LV5**.

3-4-1. Control signal input mode



3-4-2. Display data input mode

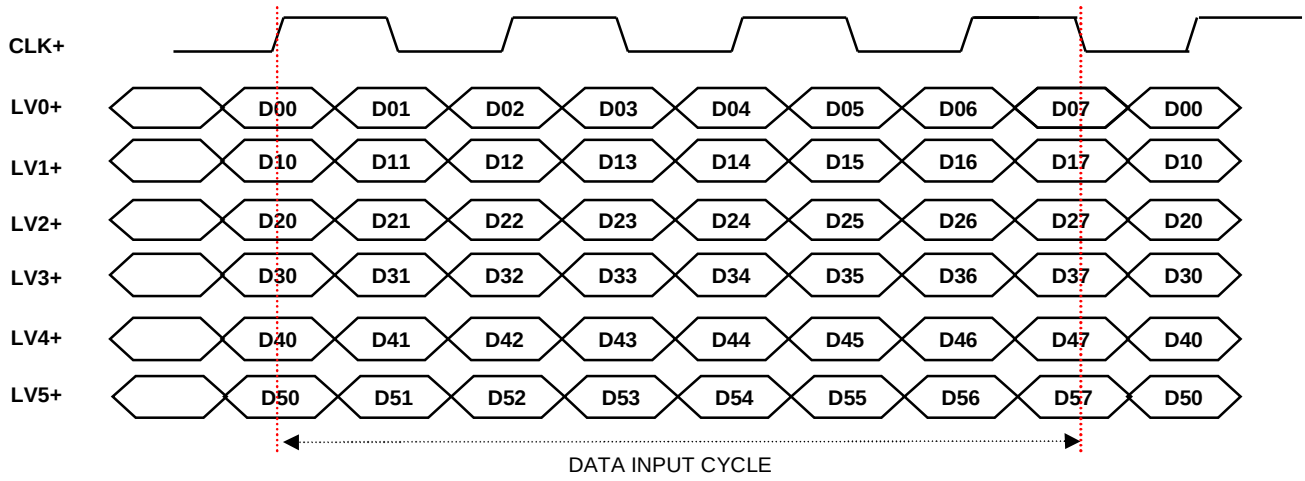


Fig. 7 Mini-LVDS Data

Note : 1. For data mapping, please refer to panel pixel structure Fig.8

3-5. Panel Pixel Structure

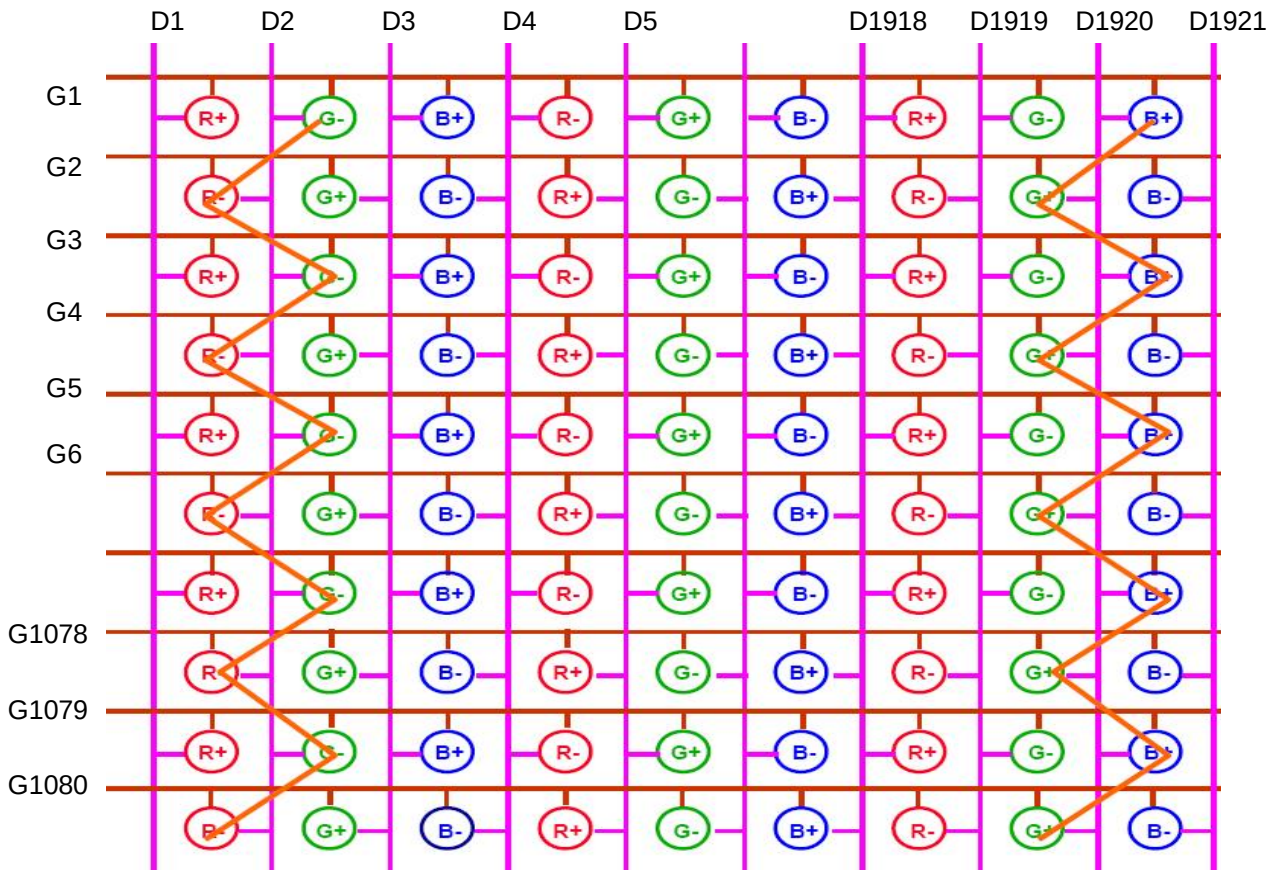


FIG. 8 Panel Pixel Structure

3-6. Power Sequence

3-6-1. LCD Driving circuit

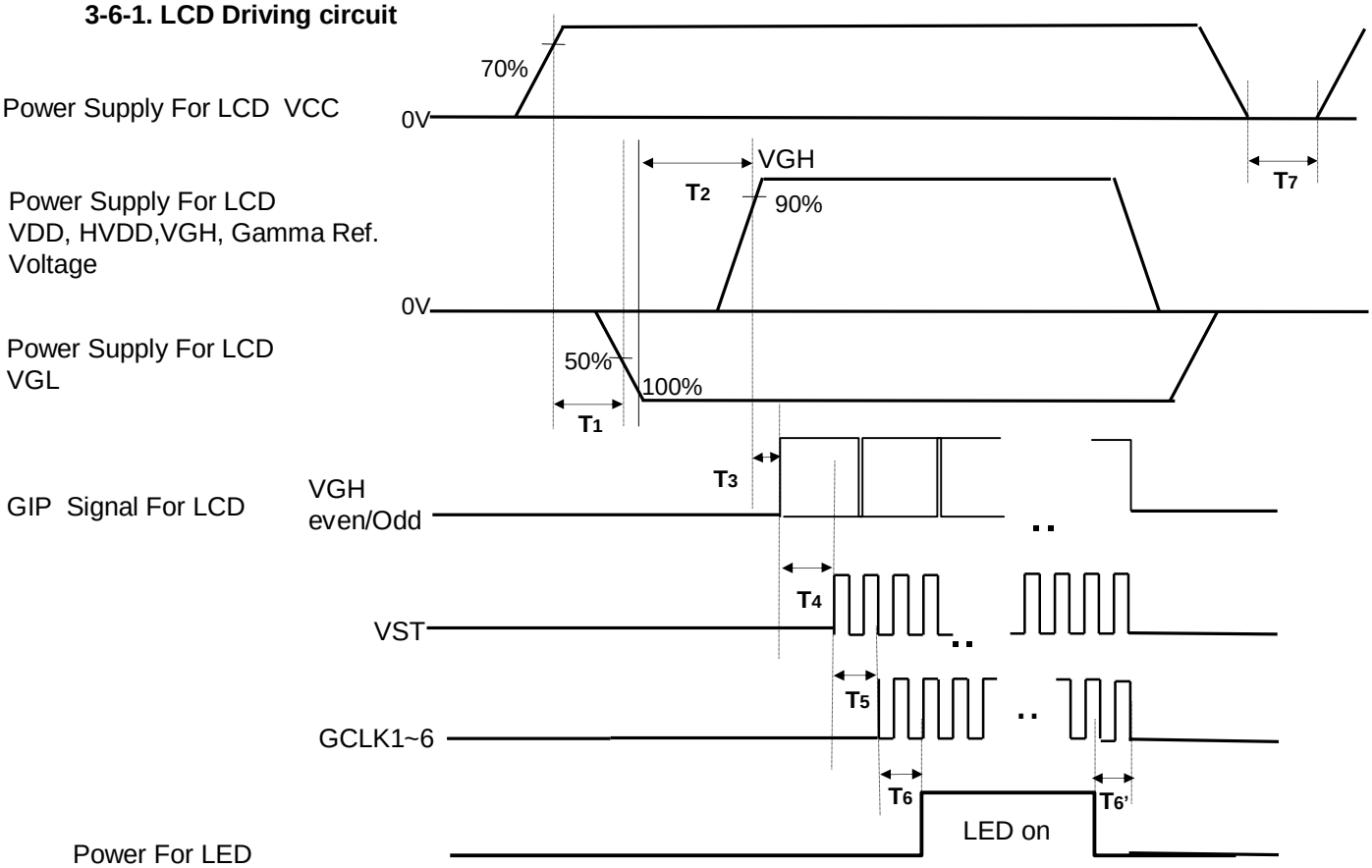


Table 7. POWER SEQUENCE

Ta= 25±2°C, fv=120Hz, Dclk=74.25MHz

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	0.5		-	ms	
T2	0.5		-	ms	
T3	0		-	ms	
T4	10		-	ms	2
T5	0		-	ms	
T6 / T6'	20		-	ms	
T7	2		-	sec	

Note : 1. Power sequence for Source D-IC must follow the Case1 & 2.
※ Please refer to Appendix V for more details.
2. VGH Odd signal should be started “High” status and VGH even & odd can not be “High at the same time.
3. Power Off Sequence order is reverse of Power On Condition including Source D-IC.
4. GCLK On/Off Sequence
Normal : GCLK4 **à** GCLK5 **à** GCLK6 **à** GCLK1 **à** GCLK2 **à** GCLK3.
Reverse : GCLK3 **à** GCLK2 **à** GCLK1 **à** GCLK6 **à** GCLK5 **à** GCLK4.
5. VDD_odd/even transition time should be within V_blank

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable in a dark environment at 25±2°C. The values are specified at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and θ equal to 0 °.
It is presented additional information concerning the measurement equipment and method in FIG. 9.

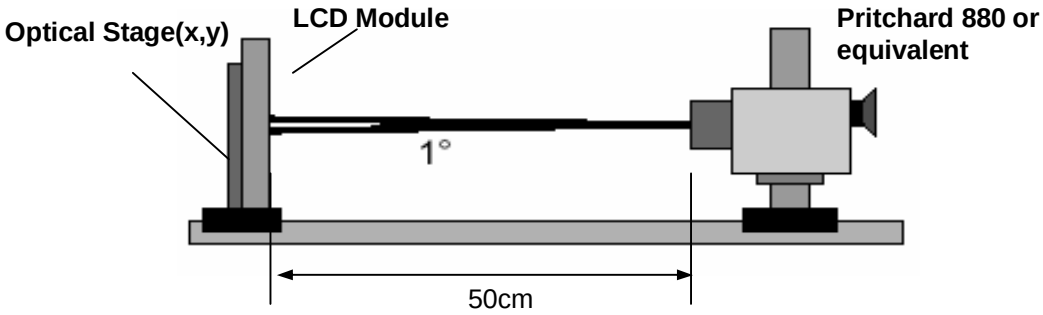


FIG. 9 Optical Characteristic Measurement Equipment and Method

Ta= 25±2°C, VDD,H_VDD,VGH,VGL=typ,
fv=120Hz, Dclk=74.25MHz,
EXTVBR-B =100% Back Light : LGD B/L

Table 6. OPTICAL CHARACTERISTICS

Parameter		Symbol	Value			Unit	Note
			Min	Typ	Max		
Contrast Ratio		CR	1000	1400	-		1
Response Time	Rising	Tr	-	8	12	ms	4
	Falling	Tf	-	10	14		
Color Coordinates [CIE1931]	RED	Rx	Typ -0.03	0.649	Typ +0.03		
		Ry		0.332			
	GREEN	Gx		0.307			
		Gy		0.595			
	BLUE	Bx		0.149			
		By		0.059			
Viewing Angle (CR>10)							
	x axis, right(ϕ=0°)	θr	89	-	-	degree	5
	x axis, left (ϕ=180°)	θl	89	-	-		
	y axis, up (ϕ=90°)	θu	89	-	-		
	y axis, down (ϕ=270°)	θd	89	-	-		
Gray Scale			-	-	-		6

Note : 1. Contrast Ratio(CR) is defined mathematically as :

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

It is measured at center 1-point.

2. Response time is the time required for the display to transition from G(0) to G(255) (Rise Time, Tr_R) and from G(0) to G(255) (Decay Time, Tr_D). For additional information see the FIG. 11.

3. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD module surface. For more information, see the FIG. 12.

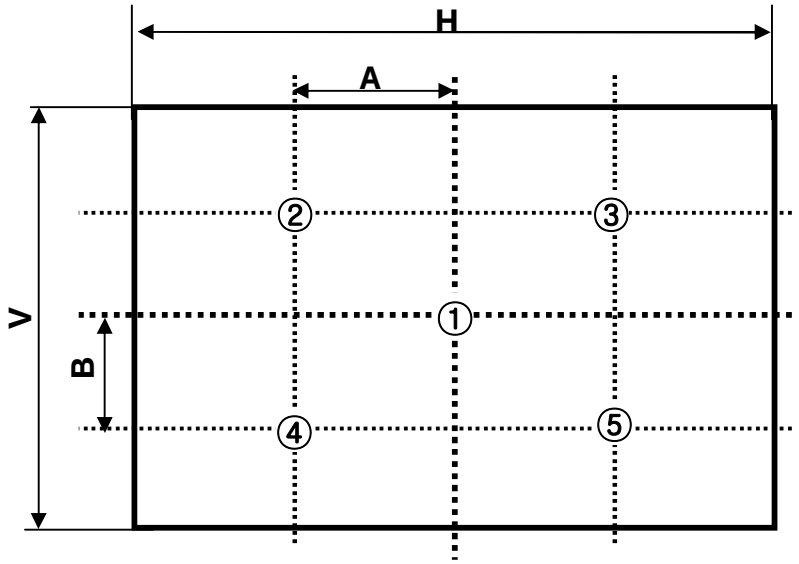
4. Gray scale specification
Gamma Value is approximately 2.2. For more information, see the Table 7.

Table 7. GRAY SCALE SPECIFICATION

Gray Level	Luminance [%] (Typ)
L0	0.07
L15	0.27
L31	1.04
L47	2.49
L63	4.68
L79	7.66
L95	11.5
L111	16.1
L127	21.6
L143	28.1
L159	35.4
L175	43.7
L191	53.0
L207	63.2
L223	74.5
L239	86.7
L255	100

	Gray Level	Gamma Ref.
Positive Voltage	L0	Gamma9
	L1	Gamma8
	L31	Gamma7
	L63	Gamma6
	L127	Gamma5
	L191	Gamma4
	L223	Gamma3
	L255	Gamma1
Negative Voltage	L255	Gamma18
	L223	Gamma16
	L191	Gamma15
	L127	Gamma14
	L63	Gamma13
	L31	Gamma12
	L1	Gamma11
	L0	Gamma10

Measuring point for surface luminance & luminance variation



A : H / 4 mm
B : V / 4 mm
@ H,V : Active Area

FIG. 10 5 Points for Luminance Measure

Response time is defined as the following figure and shall be measured by switching the input signal for "Gray(N)" and "Gray(M)".

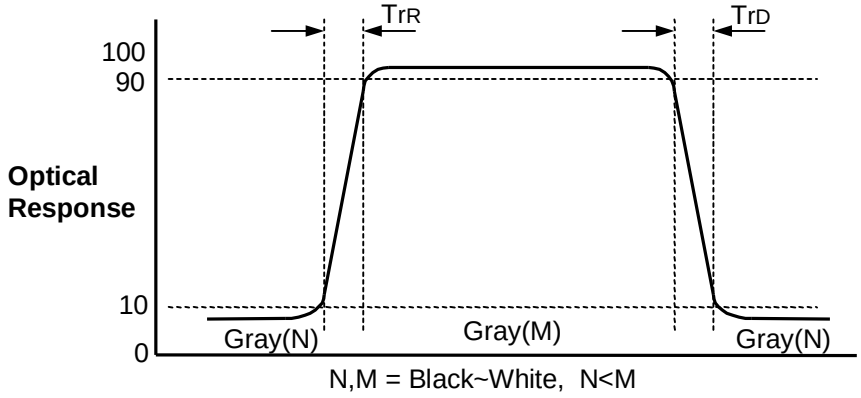


FIG. 11 Response Time

Dimension of viewing angle range

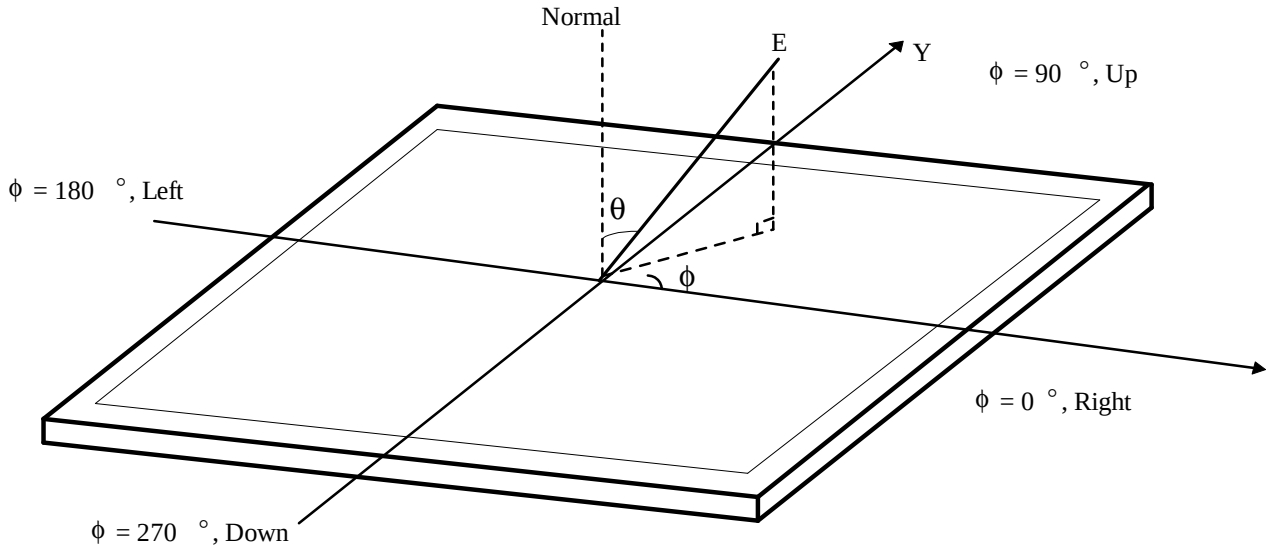


FIG.12 Viewing Angle

5. Mechanical Characteristics

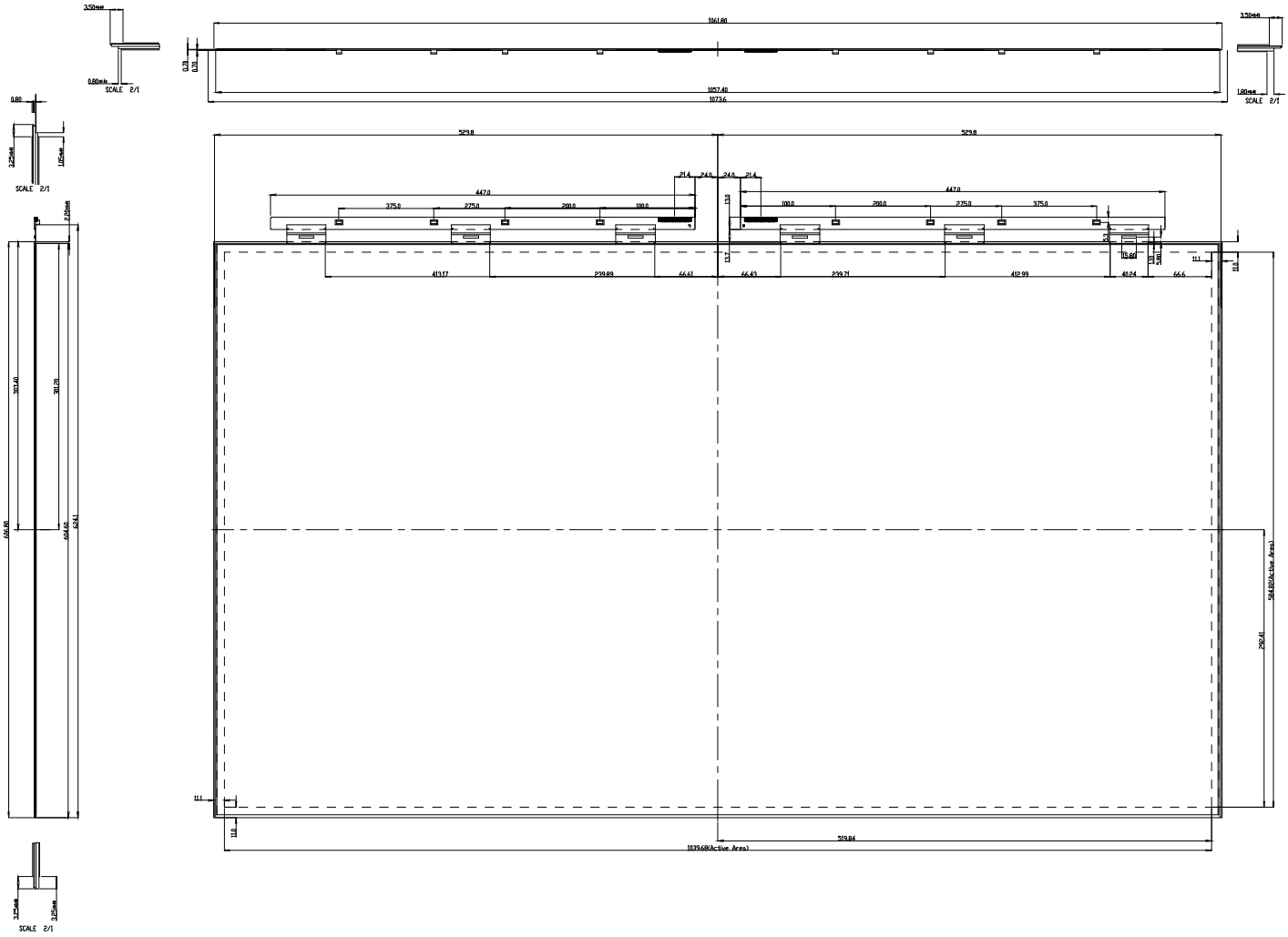
Table 8 provides general mechanical characteristics.

Table 8. MECHANICAL CHARACTERISTICS

Item	Value	
Outline Dimension	Horizontal	1061.8 mm
	Vertical	606.8 mm
	Depth	1.8 mm
Active Display Area	Horizontal	1039.68 mm
	Vertical	584.82 mm
Weight	2.50 Kg (Typ.) , 2.75 Kg (Max.)	
Surface Treatment	Hard coating(3H) Anti-glare treatment of the front polarizer(10%)	

Note : Please refer to a mechanical drawing in terms of tolerance at the next page.

[FRONT VIEW]



6. Reliability

Table 9. ENVIRONMENT TEST CONDITION

No.	Test Item	Condition
1	High temperature storage test	Ta= 60°C 240h
2	Low temperature storage test	Ta= -20°C 240h
3	High temperature operation test	Ta= 50°C 50%RH 240h
4	Low temperature operation test	Ta= 0°C 240h
5	Humidity condition Operation	Ta= 40 °C ,90%RH
6	Altitude operating storage / shipment	0 - 15,000 ft 0 - 40,000 ft

Note : Before and after Reliability test, Board ass'y should be operated with normal function.

7. International Standards

7-1. Environment

a) RoHS, Directive 2002/95/EC of the European Parliament and of the council of 27 January 2003

8. Packing

8-1. Packing Form

a) Package quantity in one Pallet : 70 pcs

b) Pallet Size : 1250 **mm(L) X 800 mm(W) X 1105 mm(H)**

9. Precautions

Please pay attention to the followings when you use this TFT LCD panel.

9-1. Assembly Precautions

(1) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
(2) You should adopt radiation structure to satisfy the temperature specification.
(3) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(4) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
(5) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzine. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer
(6) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(7) Board ass'y should be put on the mold frame properly.
(8) FFC Cable should be connected between System board and Source PCB correctly.
(9) Mechanical structure for backlight system should be designed for sustaining board ass'y safely.

9-2. Operating Precautions

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
V=±200mV(Over and under shoot voltage)
(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer
(4) Be careful for condensation at sudden temperature change.Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.
(7) Please do not give any mechanical and/or electrical impact to board assy. Otherwise, it can't be operated its full characteristics perfectly.

9-3. Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly. Panel ground path should be connected to metal ground.

9-4. Precautions for Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

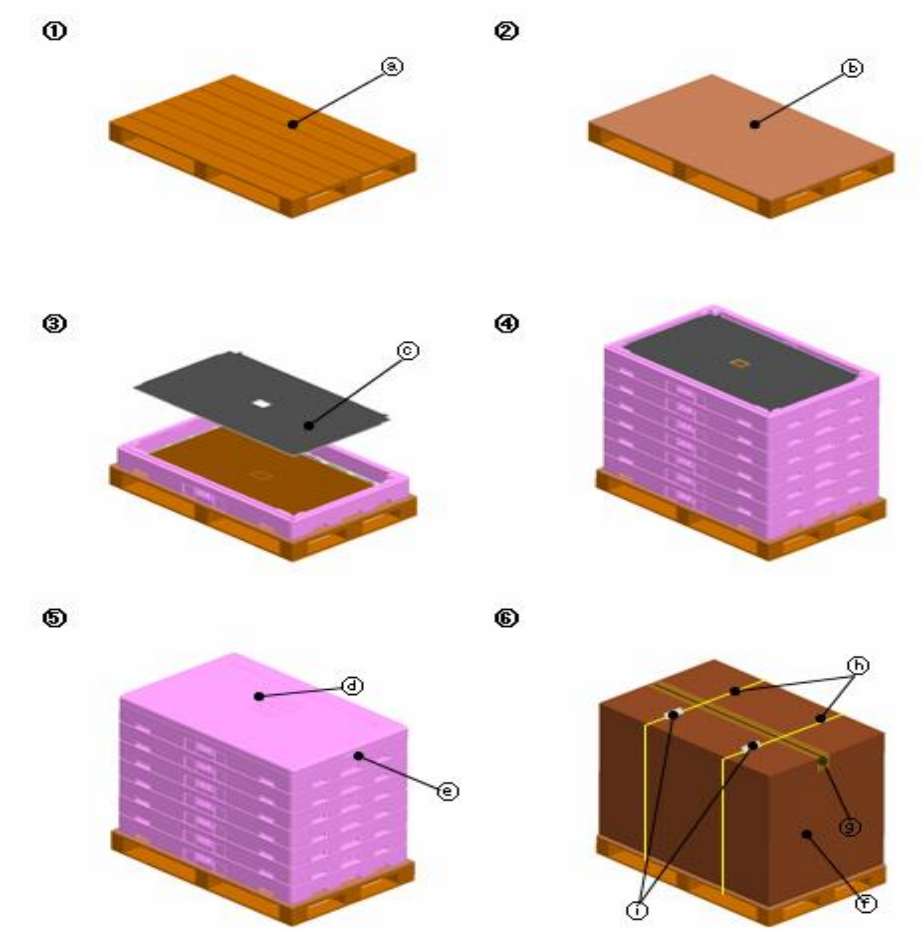
9-5. Storage

When storing the board ass'y as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the board ass'y to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
(2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

APPENDIX- I

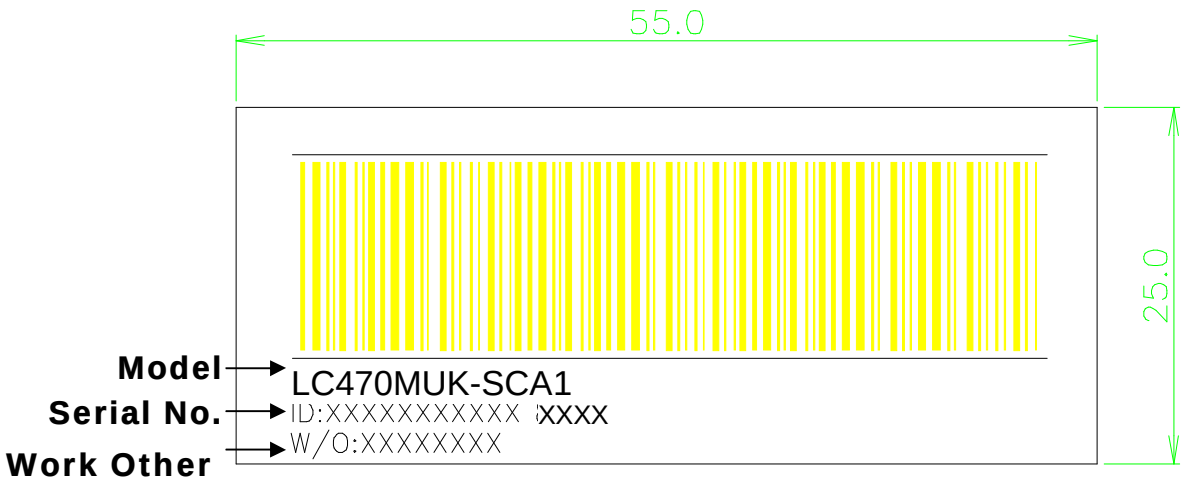
■ LC470MUK-SCA1-Pallet Ass'y



No.	Description	Material
ⓐ	Pallet	Plywood
ⓑ	Carton Plate	Single Wall
ⓒ	PE Sheet	Carbon
ⓓ	Top Packing	EPP
ⓔ	Bottom Packing	EPP
ⓕ	Angle Packing	Single Wall
ⓖ	Tape	OPP
ⓗ	Band	PP
ⓘ	Clip	Steel

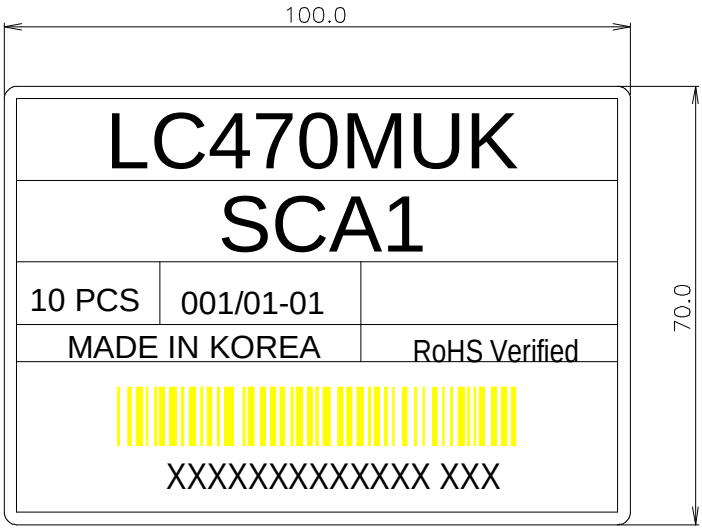
APPENDIX- II

■ LC470MUK-SCA1-Serial Label



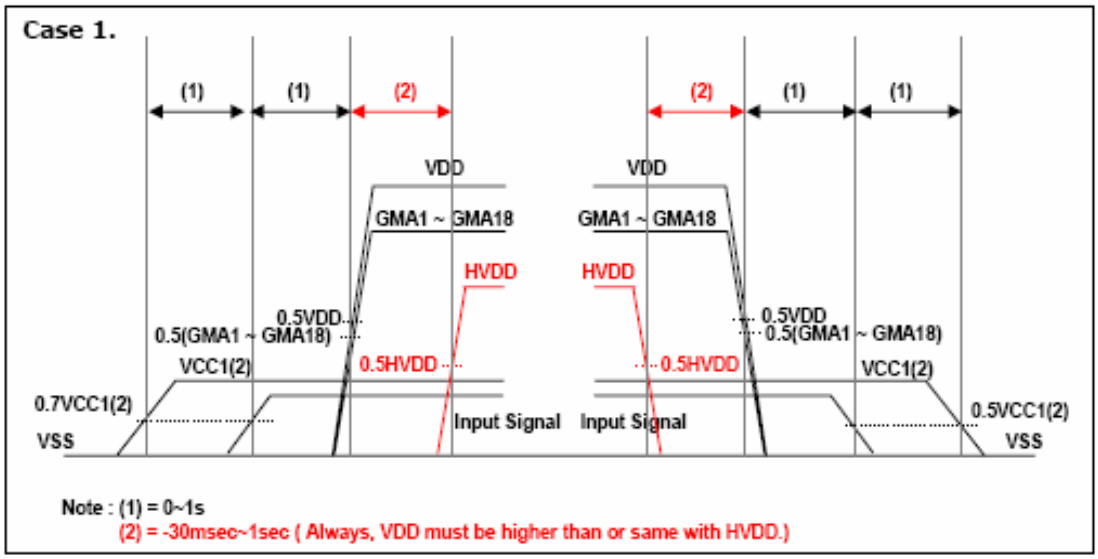
 # APPENDIX- III

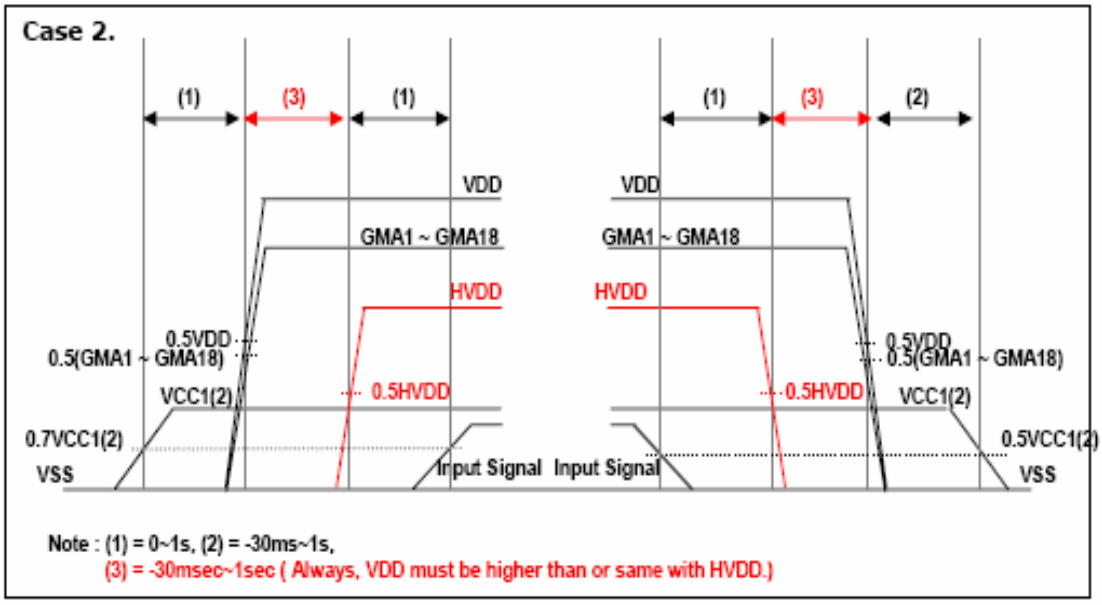
■ LC470MUK-SCA1-Pallet Label



APPENDIX- IV

■ LC470MUK-SCA1-Source D-IC Power Sequence





- Input Signal : SOE,POL,GSP,H_CONV,OPT_N