SPECIFICATION
FOR
APPROVAL

(●) **Preliminary Specification**

( ) **Final Specification**

Title	50.0” QWUXGA TFT LCD

BUYER	General
SET MODEL	

SUPPLIER	LG Display Co., Ltd.
*MODEL	LC500EQY
SUFFIX	SKM1 (RoHS Verified)

APPROVED BY	SIGNATURE / DATE
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/	

Please return 1 copy for your confirmation with your signature and comments.

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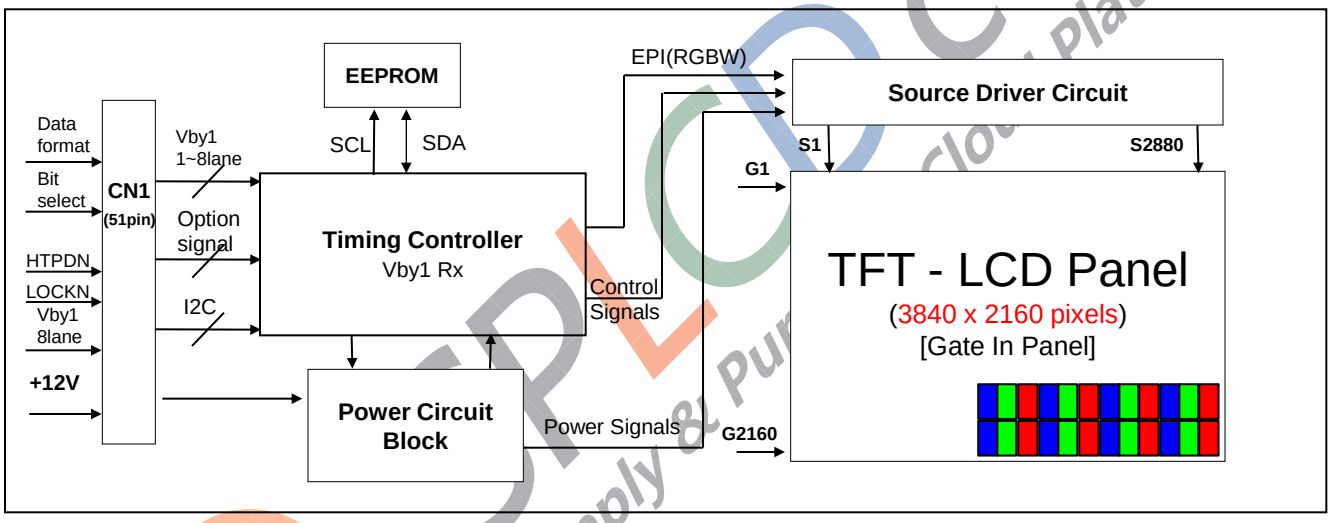
RECORD OF REVISIONS

Revision No.	Revision Date	Page	Description
0.0	Jun, 13, 2016	-	Preliminary Specification (First Draft)
0.1	Aug, 09, 2016	5	Updated Power Consumption
		13	Updated Color Coordinates
		25	Updated Pallet Ass'y Information
		26	Updated Control PCB Packing Ass'y Information

1. General Description

The LC500EQY is a Color Active Matrix Liquid Crystal Display with an integral the Source PCB and Gate implanted on Panel (GIP). The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally black mode. It has a 49.51 inch diagonally measured active display area with QWUXGA resolution (2160 vertical by 3840 horizontal pixel array). Each pixel is divided into Red, Green, Blue and White sub-pixels or dots which are arranged in vertical stripes. Gray scale or the luminance of the sub-pixel color is determined with a 10-bit gray scale signal for each dot. Therefore, it can present a palette of more than 1.07Bilion colors.
It has been designed to apply the 10-bit 8 Lane V by One interface.
It is intended to support LCD TV, PCTV where high brightness, super wide viewing angle, high color gamut, high color depth and fast response time are important.



General Features

Active Screen Size	49.51 inches(1257.5mm) diagonal
Outline Dimension	1107.8 (H) x 630.2 (V) x 1.3 (D) mm(Typ.)
Pixel Pitch	0.28542 mm x 0.28542 mm
Pixel Format	3840 horiz. by 2160 vert. Pixels,
Color Depth	10bit(D), 1.07Billon colors
Drive IC Data Interface	Source D-IC : 8-bit EPI, gamma reference voltage, and control signals Gate D-IC : Gate In Panel
Transmittance (With POL)	5.09 %(Typ.)
Viewing Angle (CR>10)	Viewing angle free (R/L 178 (Min.), U/D 178 (Min.))
Weight	2.1Kg (Typ.)
Display Mode	Transmissive mode, Normally black
Surface Treatment (Top)	Hard coating(2H), Anti-glare low reflection treatment of the front polarizer (Haze 3%(Typ.))

2. Absolute Maximum Ratings

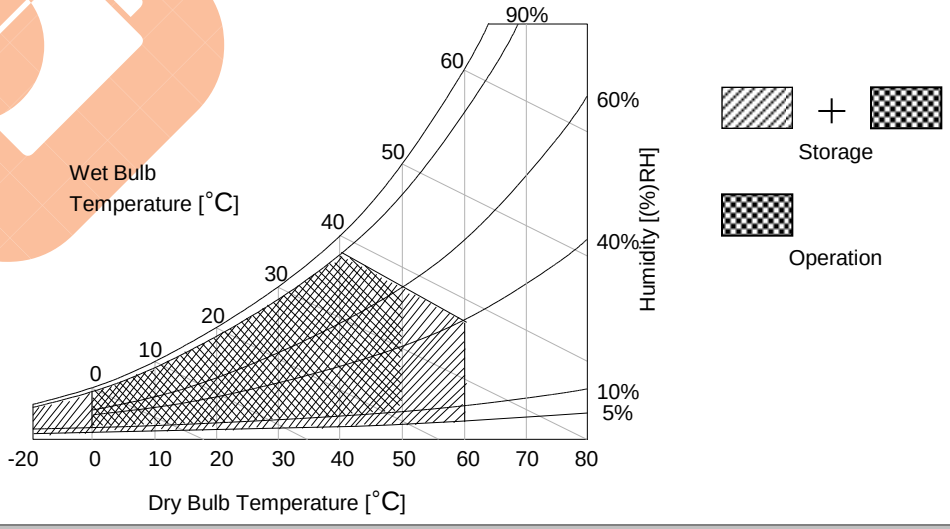
The following items are maximum values which, if exceeded, may cause faulty operation or permanent damage to the LCD module.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value		Unit	Note
			Min	Max		
Power Input Voltage	LCD Circuit	VLCD	-0.3	+14.0	VDC	1
T-Con Option Selection Voltage		VLOGIC	-0.3	+4.0	VDC	
Operating Temperature		TOP	0	+50	°C	2,3
Storage Temperature (without packing)		TST	-20	+60	°C	
Panel Front Temperature		TSUR	-	+68	°C	4
Operating Ambient Humidity		HOP	10	90	%RH	2,3
Storage Humidity		HST	5	90	%RH	

Note1. Ambient temperature condition (Ta = 25 ± 2 °C)

2. Temperature and relative humidity range are shown in the figure below.
   Wet bulb temperature should be Max 39°C, and no condensation of water.
3. Gravity mura can be guaranteed below 40°C condition.
4. The maximum operating temperatures is based on the test condition that the surface temperature of display area is less than or equal to 68°C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 68℃. The range of operating temperature may be degraded in case of improper thermal management in final product design.



3. Electrical Specifications

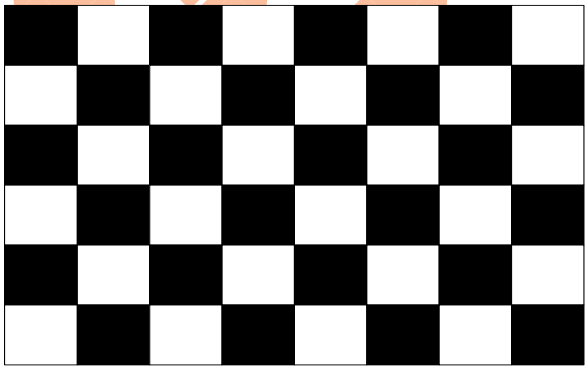
3-1. Electrical Characteristics

Table 2. ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Value			Unit	Note
			Min	Typ	Max		
Circuit :							
Power Input Voltage		V_{LCD}	10.8	12.0	13.2	V_{DC}	
Power Input Current		I_{LCD}	-	920(TBD)	1195(TBD)	mA	1
			-	1340(TBD)	1740(TBD)	mA	2
T-CON Option Selection Voltage	Input High Voltage	V_{IH}	2.7	-	3.6	V_{DC}	
	Input Low Voltage	V_{IL}	0	-	0.7	V_{DC}	
Power Consumption		P_{LCD}	-	11.04(TBD)	14.35(TBD)	Watt	1
Rush current		I_{RUSH}	-	-	5.0	A	3

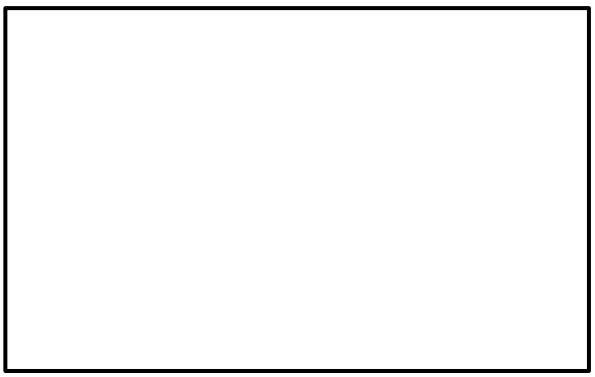
Note
1. The specified current and power consumption are under the V_{LCD}=12.0V, Ta=25 ± 2°C, f_V=60Hz condition, and mosaic pattern(8 x 6) is displayed and f_V is the frame frequency.
2. The current is specified at the maximum current pattern.
3. The duration of rush current is about 2ms and rising time of power input is 0.5ms (min.).
4. Ripple voltage level is recommended under ±5% of typical voltage

White : 1023Gray, Black : 0 Gray



Mosaic Pattern(8 x 6)

White
R : 1023Gray, G : 0Gray, B : 1023Gray



Max Current Pattern

3-2. Interface Connections

This LCD module employs one kind of interface connection, 51-pin connector is used for the module electronics.

3-2-1. LCD Module

- LCD Connector(CN1) : FI-RE51S-HF(manufactured by JAE) or GT05P-51S-H38(manufactured by LSM) or IS050-C51B-C39(manufactured by UJU)
- Mating Connector : FI-R51HL(manufactured by JAE) or compatible

Table 3. MODULE CONNECTOR(CN1) PIN CONFIGURATION

No	Symbol	Description	No	Symbol	Description
1	VLCD	Power Supply +12.0V	27	GND	Ground
2	VLCD	Power Supply +12.0V	28	Rx0n	V-by-One HS Data Lane 0
3	VLCD	Power Supply +12.0V	29	Rx0p	V-by-One HS Data Lane 0
4	VLCD	Power Supply +12.0V	30	GND	Ground
5	VLCD	Power Supply +12.0V	31	Rx1n	V-by-One HS Data Lane 1
6	VLCD	Power Supply +12.0V	32	Rx1p	V-by-One HS Data Lane 1
7	VLCD	Power Supply +12.0V	33	GND	Ground
8	VLCD	Power Supply +12.0V	34	Rx2n	V-by-One HS Data Lane 2
9	NC	NO CONNECTION	35	Rx2p	V-by-One HS Data Lane 2
10	GND	Ground	36	GND	Ground
11	GND	Ground	37	Rx3n	V-by-One HS Data Lane 3
12	GND	Ground	38	Rx3p	V-by-One HS Data Lane 3
13	GND	Ground	39	GND	Ground
14	NC	NO CONNECTION	40	Rx4n	V-by-One HS Data Lane 4
15	NC	NO CONNECTION	41	Rx4p	V-by-One HS Data Lane 4
16	NC	NO CONNECTION	42	GND	Ground
17	NC	NO CONNECTION	43	Rx5n	V-by-One HS Data Lane 5
18	SDA	SDA (For I2C)	44	Rx5p	V-by-One HS Data Lane 5
19	SCL	SCL (For I2C)	45	GND	Ground
20	NC	NO CONNECTION	46	Rx6n	V-by-One HS Data Lane 6
21	Bit SEL	'H' or NC= 10bit(D) , 'L' = 8bit	47	Rx6p	V-by-One HS Data Lane 6
22	Data format	'L' : Non division, 'H' 2 division	48	GND	Ground
23	AGP or NSB	'H' or NC : AGP 'L' : NSB (No signal Black)	49	Rx7n	V-by-One HS Data Lane 7
24	NC	NO CONNECTION	50	Rx7p	V-by-One HS Data Lane 7
25	HTPDN	Hot plug detect	51	GND	Ground
26	LOCKN	Lock detect	-	-	-

Note
1. All GND (ground) pins should be connected together to the LCD module's metal frame.
2. All Input levels of V-by-One signals are based on the V-by-One-HS Standard Version 1.4
3. #20 & #24 NC(No Connection) : These pins are used only for LGD (Do not connect)
4. About specific pin(#22), Please see the Appendix Ⅷ.
5. Specific pin No. #23 is used for "No signal detection" of system signal interface.
   It should be GND for NSB (No Signal Black) while the system interface signal is not.
   If this pin is "H", LCD Module displays AGP (Auto Generation Pattern).

3-3. Signal Timing Specifications

Table 4 shows the signal timing required at the input of the Vx1 transmitter. All of the interface signal timings should be satisfied with the following specification for normal operation.

Table 4. TIMING TABLE (DE Only Mode)

ITEM		Symbol	Min	Typ	Max	Unit	Note
Horizontal	Display Period	t_{HV}	480	480	480	t_{CLK}	3840/8
	Blank	t_{HB}	50	70	120	t_{CLK}	1
	Total	t_{HP}	530	550	600	t_{CLK}	
Vertical	Display Period	t_{VV}	2160	2160	2160	Lines	
	Blank	t_{VB}	40	90	600	Lines	1
	Total	t_{VP}	2200	2250	2760	Lines	

ITEM		Symbol	Min	Typ	Max	Unit	Note
Frequency	DCLK	f_{CLK}	60	74.25	78.00	MHz	594/8
	Horizontal	f_H	121.8	135	140	KHz	2
	Vertical	f_V	47	60	63	Hz	2

Notes: 1. The input of HSYNC & VSYNC signal does not have an effect on normal operation (DE Only Mode). If you use spread spectrum of EMI, add some additional clock to minimum value for clock margin.

2. The performance of the electro-optical characteristics may be influenced by variance of the vertical refresh rate and the horizontal frequency

※ Timing should be set based on clock frequency.

3-4. V by One input signal Characteristics

3-4-1. V by One Input Signal Timing Diagram

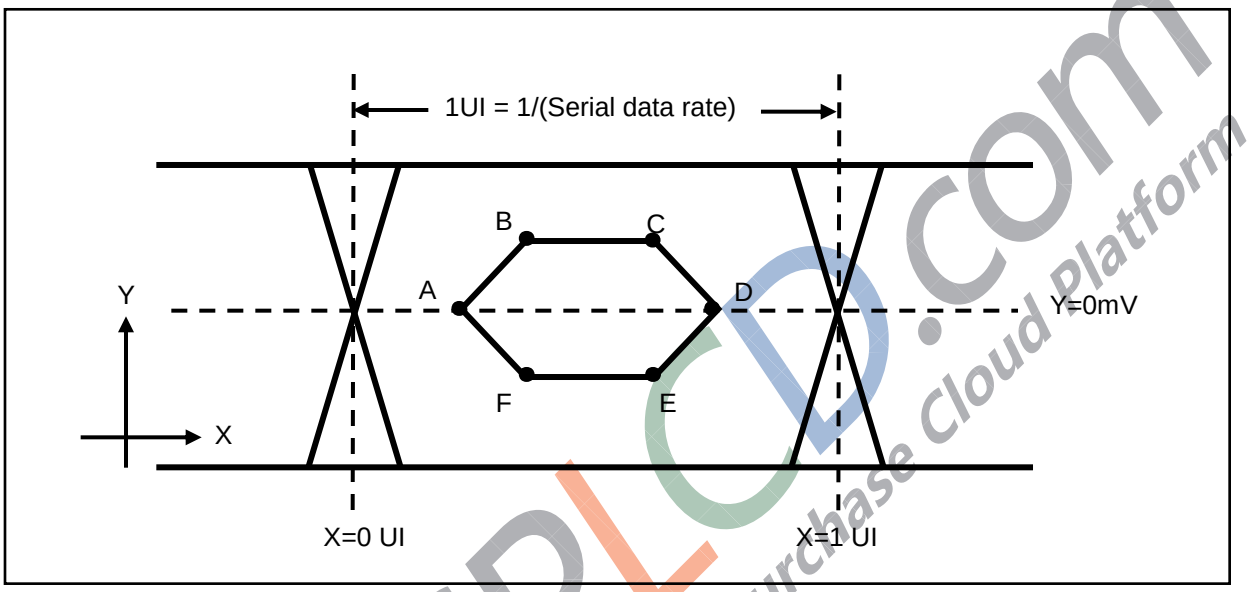
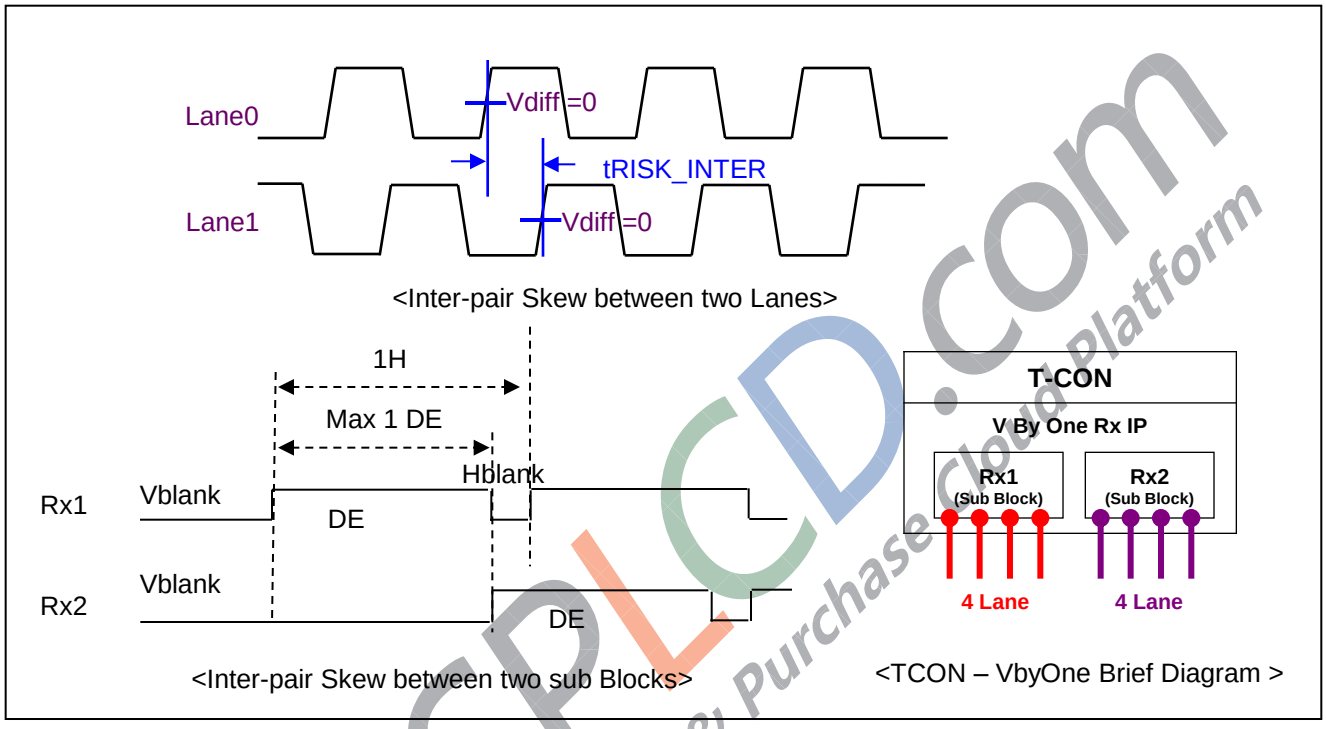


Table5. Eye Mask Specification

	X[UI]	Note	Y[mV]	Note
A	0.25 (max)	2	0	-
B	0.3 (max)	2	50	3
C	0.7(min)	3	50	3
D	0.75(min)	3	0	-
E	0.7(min)	3	I -50 I	3
F	0.3(max)	2	I -50 I	3

notes 1. All Input levels of V by One signals are based on the V by One HS Standard Ver. 1.4
2. This is allowable maximum value.
3. This is allowable minimum value.
4. The eye diagram is measured by the oscilloscope and receiver CDR characteristic must be emulated.
   - PLL bandwidth : 20 Mhz
   - Damping Factor : 1.5

3-4-2. V by One Input Signal Characteristics



Description	Symbol	Min	Max	Unit	notes
Allowable inter-pair skew between lanes	tRISK_INTER	-	5	UI	1,3
Allowable iner-pair skew between sub-blocks	tRISK_BLOCK	-	1	DE	1,4

Notes 1.1UI = 1/serial data rate

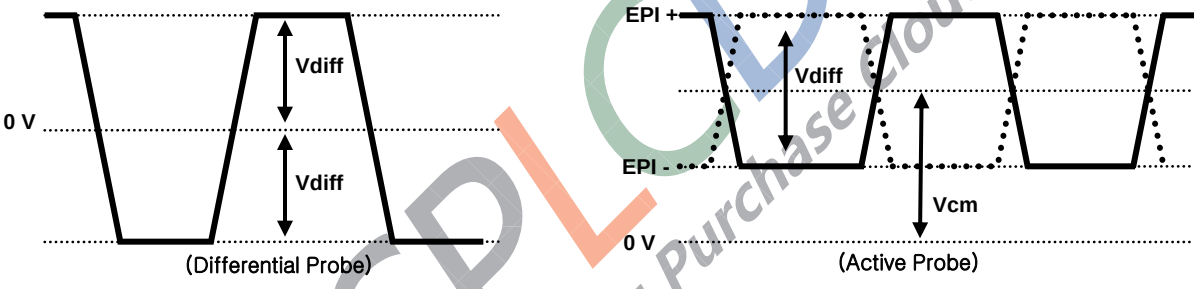
2. it is the time difference between the true and complementary single-ended signals.
3. it is the time difference of the differential voltage between any two lanes in one sub block.
4. it is the time difference of the differential voltage between any two blocks in one IP.

3-5. Intra interface Signal Specification

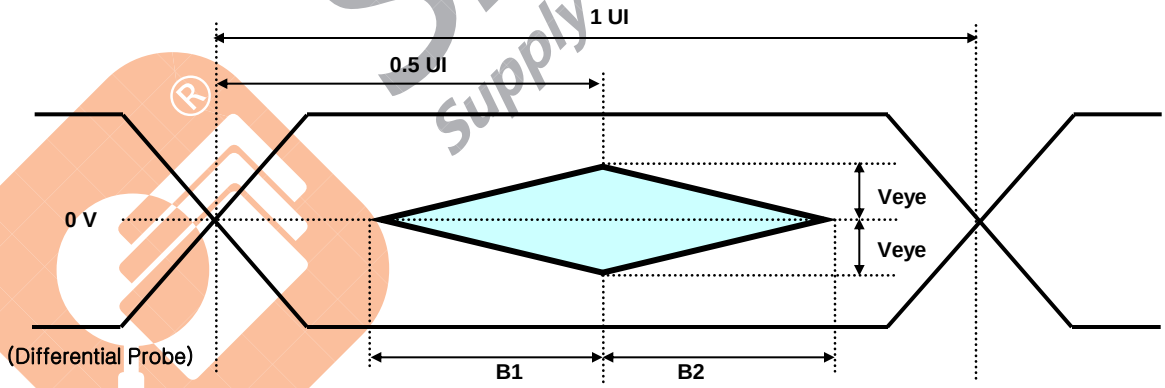
3-5-1. EPI Signal Specification

Table 6. ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	notes
Logic & EPI Power Voltage	VCC	-	1.62	1.8	1.98	VDC	
EPI input common voltage	VCM	CML Type	0.8	-	1.2-Vdiff/2	V	
EPI input differential voltage	Vdiff	-	150	-	500	mV	
EPI Input eye diagram	Veye	-	90	-	-	mV	
Effective Veye width time	B1&B2		0.25	-	-	UI	



EPI Differential signal characteristics



Eye Pattern of EPI Input

*Source PCB

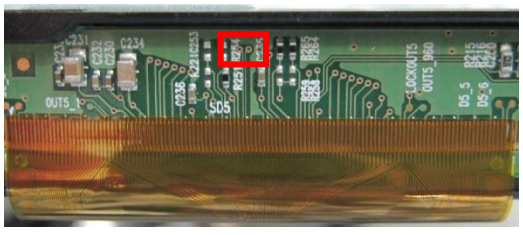


FIG. 3 Measure point

3-6. Color Data Reference

The brightness of each primary color (red, green, blue) is based on the 10bit or 8bit gray scale data input for the color. The higher binary input, the brighter the color. Table 7 provides a reference for color versus data input.

Table 7. COLOR DATA REFERENCE

Packer input & Unpacker output		30bpp RGB (10bit)	24bpp RGB (8bit)
Byte0	D[0]	R[2]	R[0]
	D[1]	R[3]	R[1]
	D[2]	R[4]	R[2]
	D[3]	R[5]	R[3]
	D[4]	R[6]	R[4]
	D[5]	R[7]	R[5]
	D[6]	R[8]	R[6]
	D[7]	R[9]	R[7]
Byte1	D[8]	G[2]	G[0]
	D[9]	G[3]	G[1]
	D[10]	G[4]	G[2]
	D[11]	G[5]	G[3]
	D[12]	G[6]	G[4]
	D[13]	G[7]	G[5]
	D[14]	G[8]	G[6]
	D[15]	G[9]	G[7]
Byte2	D[16]	B[2]	B[0]
	D[17]	B[3]	B[1]
	D[18]	B[4]	B[2]
	D[19]	B[5]	B[3]
	D[20]	B[6]	B[4]
	D[21]	B[7]	B[5]
	D[22]	B[8]	B[6]
	D[23]	B[9]	B[7]
Byte3	D[24]	Don't care	
	D[25]	Don't care	
	D[26]	B[0]	
	D[27]	B[1]	
	D[28]	G[0]	
	D[29]	G[1]	
	D[30]	R[0]	
	D[31]	R[1]	

3-7. Power Sequence

3-7-1. LCD Driving circuit

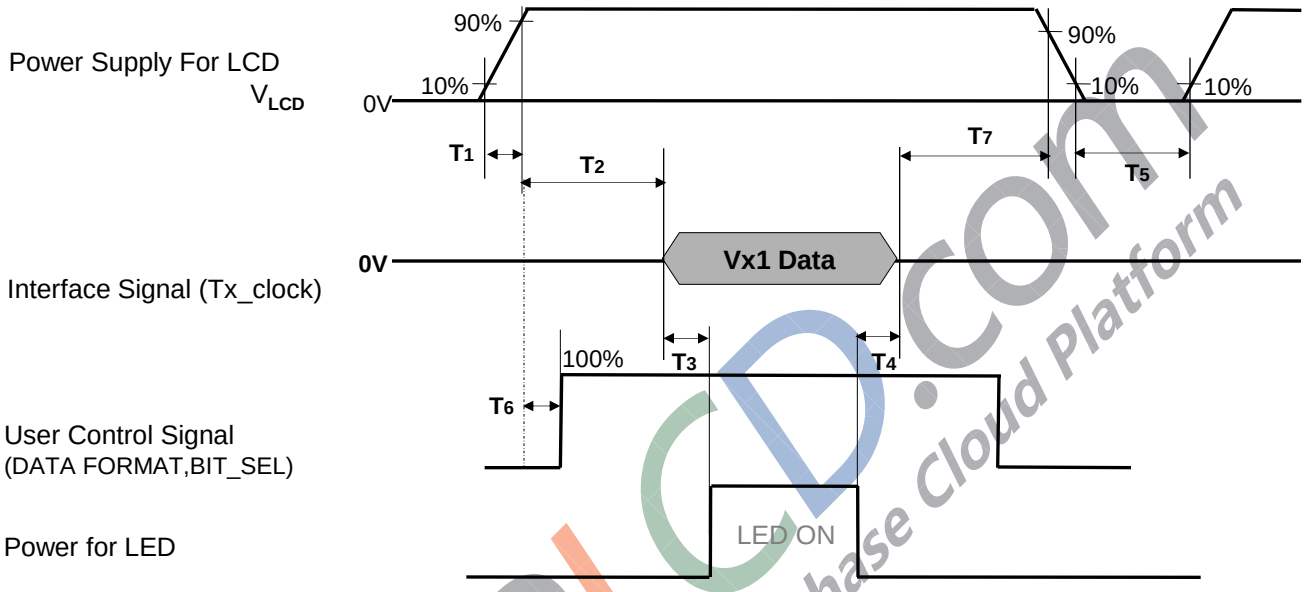


Table 8. POWER SEQUENCE

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	0.5	-	20	ms	1
T2	0	-	-	ms	2
T3	400	-	-	ms	3
T4	100	-	-	ms	3
T5	1.0	-	-	s	4
T6	0	-	T2	ms	5
T7	0	-	-	ms	6

Note :
1. Even though T1 is over the specified value, there is no problem if I2T spec of fuse is satisfied.
2. If T2 is satisfied with specification after removing V by One Cable, there is no problem.
3. The T3 / T4 is recommended value, the case when failed to meet a minimum specification, abnormal display would be shown. There is no reliability problem.
4. T5 should be measured after the Module has been fully discharged between power off and on period.
5. If the on time of signals (Interface signal and user control signals) precedes the on time of Power (V_{LCD}), it will be happened abnormal display. When T6 is NC status, T6 doesn't need to be measured.
6. It is recommendation specification that T7 has to be 0ms as a minimum value.

※ Please avoid floating state of interface signal at invalid period.

※ When the power supply for LCD (VLCD) is off, be sure to pull down the valid and invalid data to 0V.

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable in a dark environment at 25±2°C. The values are specified at distance 50cm from the LCD surface at a viewing angle of Φ and θ equal to 0 °. FIG. 1 shows additional information concerning the measurement equipment and method.

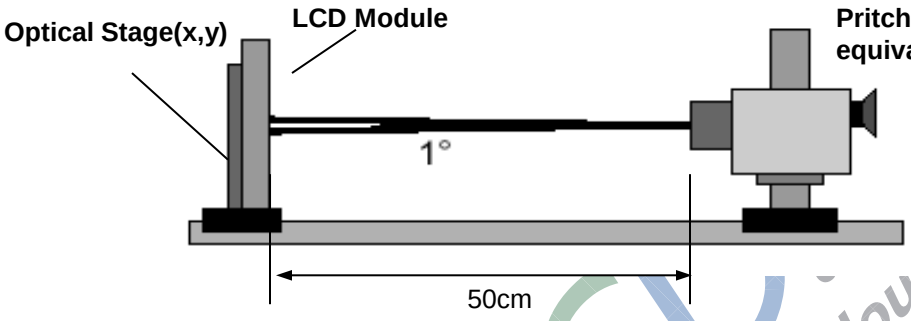


FIG. 1 Optical Characteristic Measurement Equipment and Method

Table 9. OPTICAL CHARACTERISTICS

Ta= 25±2°C, V_{LCD}=12.0V, fV=60Hz, Dclk=74.25MHz, Light Source : D65 Standard

Parameter		Symbol	Value			Unit	Note
			Min	Typ	Max		
Contrast Ratio		CR	900	1200(TBD)	-		1
Response Time	Variation	G to G $_{\sigma}$		6	9		3
	Gray to Gray (BW)	G to G BW		9	13	ms	2
Transmittance		T		5.09		%	4
Color Coordinates [CIE1931]	RED	Rx	Typ -0.03	0.659(TBD)	Typ +0.03		5
		Ry		0.328(TBD)			
	GREEN	Gx		0.282(TBD)			
		Gy		0.583(TBD)			
	BLUE	Bx		0.135(TBD)			
		By		0.121(TBD)			
Viewing Angle (CR>10)							
	x axis, right(ϕ=0°)	θr	89	-	-	degree	6
	x axis, left (ϕ=180°)	θl	89	-	-		
	y axis, up (ϕ=90°)	θu	89	-	-		
	y axis, down (ϕ=270°)	θd	89	-	-		
Gray Scale			-	-	-		7

Note : 1. Contrast Ratio(CR) is defined mathematically as :

CR(Contrast Ratio) = Maximum CRn (n=1, 2, 3, 4, 5)

$$CRn = \frac{\text{Surface Luminance at position n with all white pixels}}{\text{Surface Luminance at position n with all black pixels}}$$

n = the Position number(1, 2, 3, 4, 5). For more information, see FIG 2.

The contrast ratio is valued with operating condition of LGD's standard BLU

2. Response time is the time required for the display to transit from any gray to white (Rise Time, Tr_R) and from any gray to black (Decay time, Tr_D). For additional information see the FIG. 3.

※ G to G_{BW} Spec stands for average value of all measured points.

Photo Detector : RD-80S / Field : 2 °

The response time is valued with operating condition of LGD's standard BLU

3. G to G $_\sigma$ is Variation of Gray to Gray response time composing a picture

$$\text{G to G } (\sigma) = \sqrt{\frac{\Sigma(Xi - u)^2}{N}}$$

Xi = Individual Data
u = Data average
N : The number of Data

4. The value of transmittance should be extracted using the standard light source of D65

5. The value of color coordinates should be extracted using the standard light source of D65

6. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD module surface. For more information, see the FIG. 4.

7. Gray scale specification

Gamma Value is approximately 2.2. For more information, see the Table 10.

Table 10. GRAY SCALE SPECIFICATION

Gray Level	Luminance [%] (Typ)
L0	0.09 (TBD)
L63	0.27
L127	1.04
L191	2.49
L255	4.68
L319	7.66
L383	11.5
L447	16.1
L511	21.6
L575	28.1
L639	35.4
L703	43.7
L767	53.0
L831	63.2
L895	74.5
L959	86.7
L1023	100

Measuring point for Contrast Ratio

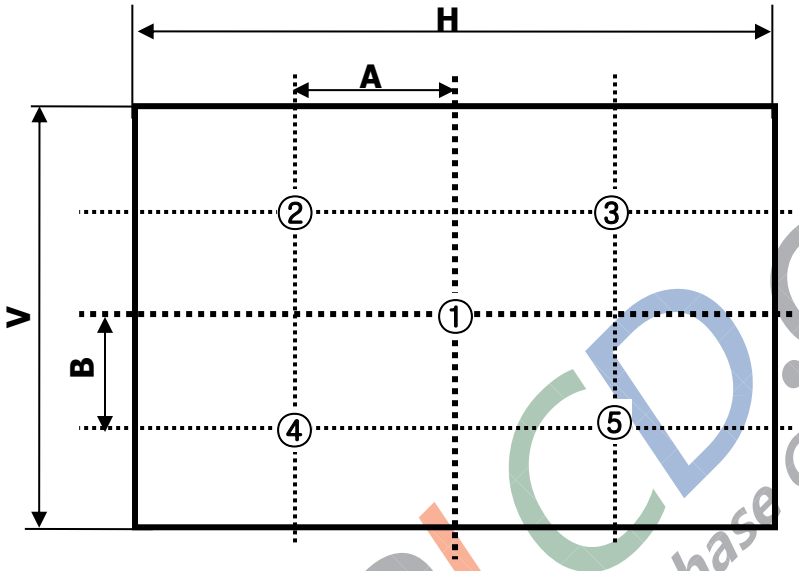


FIG. 2 Points for Contrast Ratio Measure

Response time is defined as the following figure and shall be measured by switching the input signal for "Gray(N)" and "Black or White".

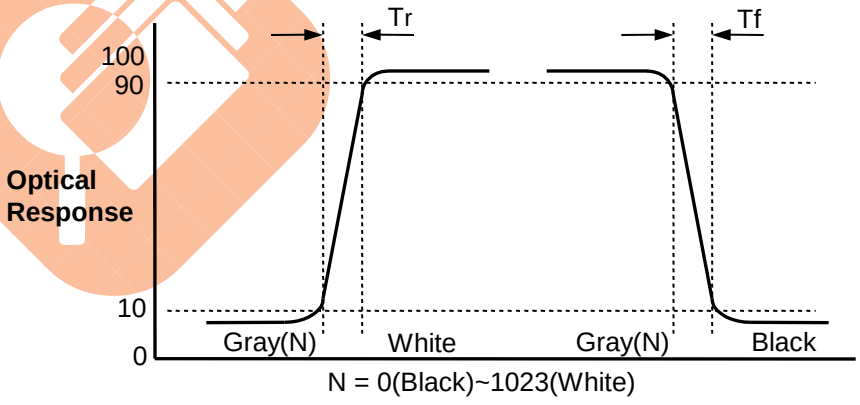


FIG. 3 Response Time

Dimension of viewing angle range

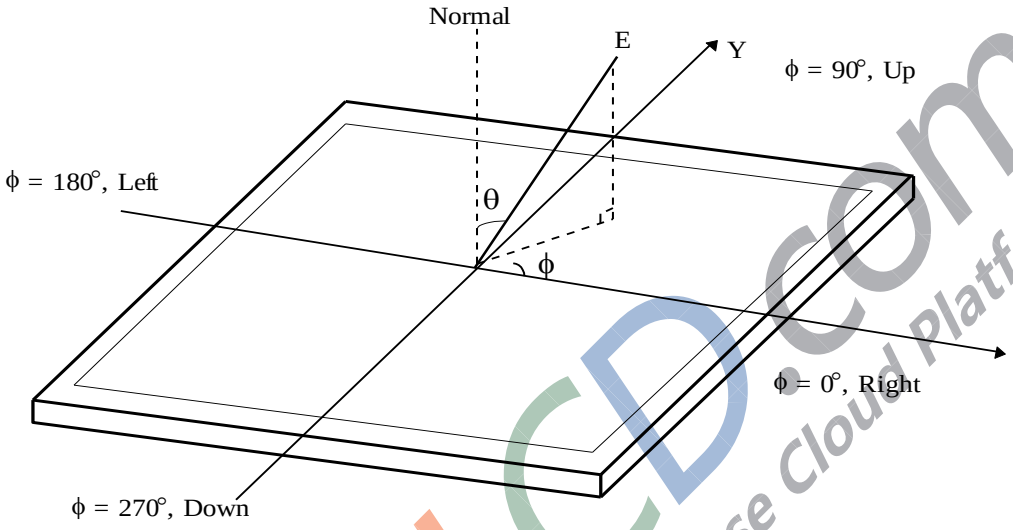


FIG. 4 Viewing Angle

5. Mechanical Characteristics

Table 11 provides general mechanical characteristics.

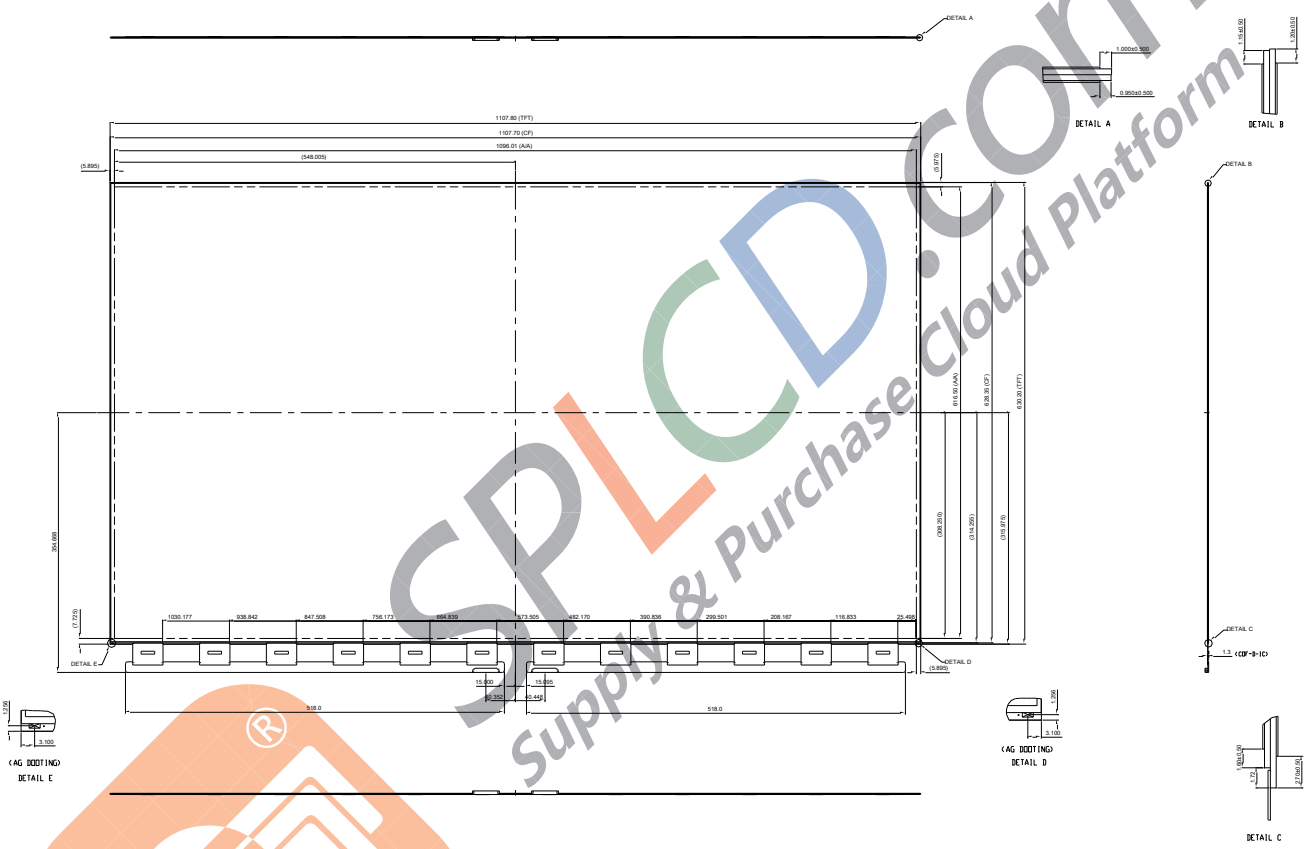
Table 11. MECHANICAL CHARACTERISTICS

Item	Value	
Outline Dimension (Only Glass)	Horizontal	1107.8 mm
	Vertical	630.2 mm
	Depth	1.3 mm
Active Display Area	Horizontal	1096.01 mm
	Vertical	616.51 mm
Weight	2.1Kg (Typ.)	
Surface Treatment	Hard coating(2H), Anti-glare low reflection treatment of the front polarizer (Haze 3%(Typ.))	

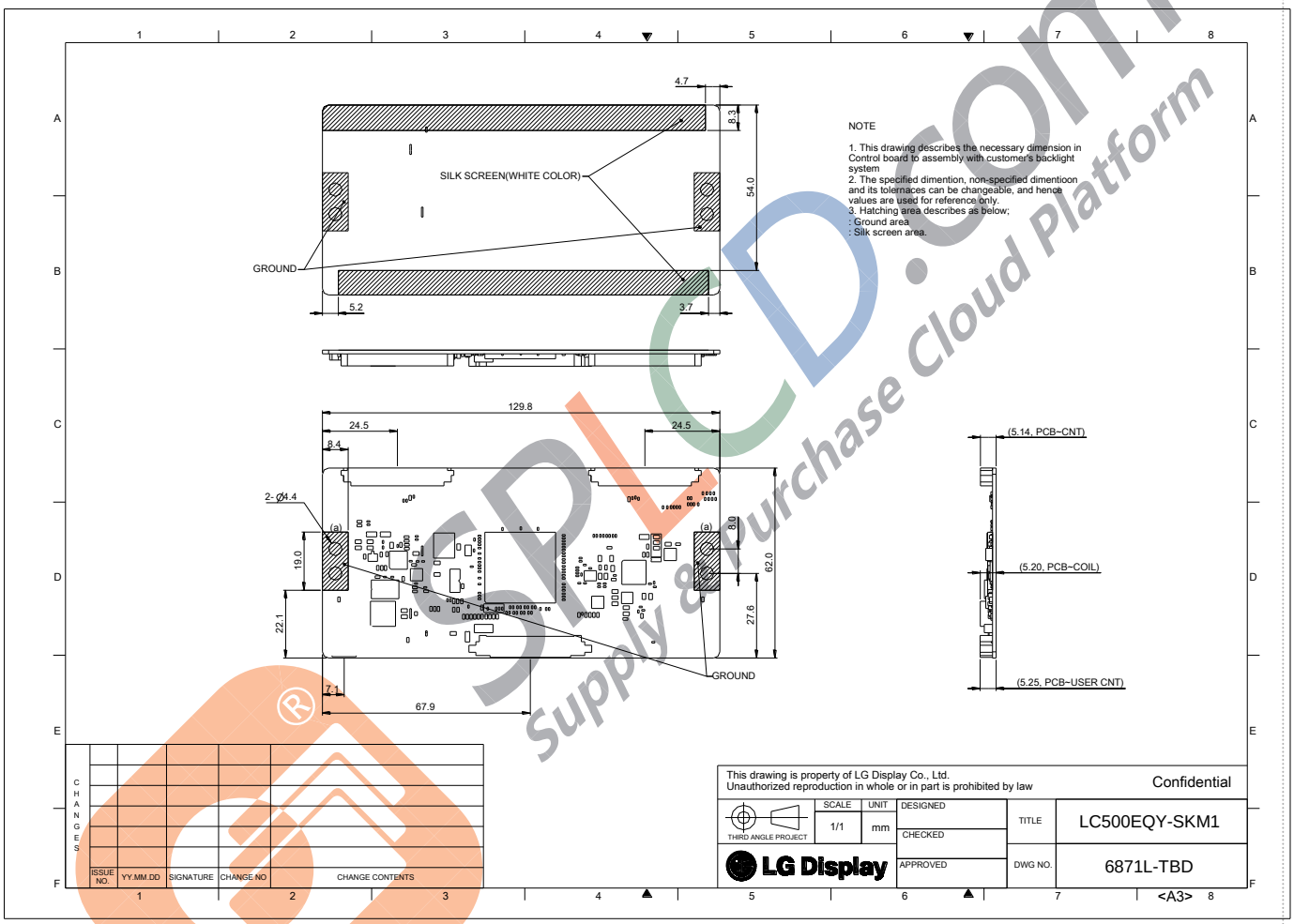
Note : Please refer to a mechanic drawing in terms of tolerance at the next page.

6. Mechanical Dimension

6-1. Board Assembly Dimension



6-2. Control Board Assembly Dimension



Date	Version

7. Reliability

Table 12. ENVIRONMENT TEST CONDITION

No.	Test Item	Condition
1	High temperature storage test	Ta= 60°C 90% 240h
2	Low temperature storage test	Ta= -20°C 240h
3	High temperature operation test	Ta= 50°C 50%RH 500h
4	Low temperature operation test	Ta= 0°C 500h
5	Humidity condition Operation	Ta= 40 °C ,90%RH
6	Altitude operating storage / shipment	0 - 16,400 ft 0 - 40,000 ft

Note : Before and after Reliability test, LCM should be operated with normal function.

8. International Standards

8-1. Safety

a) UL 60065, Underwriters Laboratories Inc.
Audio, Video and Similar Electronic Apparatus - Safety Requirements.

b) CAN/CSA C22.2 No.60065:03, Canadian Standards Association.
Audio, Video and Similar Electronic Apparatus - Safety Requirements.

c) IEC 60065, The International Electrotechnical Commission (IEC).
Audio, Video and Similar Electronic Apparatus - Safety Requirements.

8-2. Environment

a) RoHS, Directive 2011/65/EU of the European Parliament and of the council of 8 June 2011

9. Packing

9-1. Information of B/Ass'y Label

a) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M

A,B,C : SIZE(INCH)
D : YEAR
E : MONTH
F ~ M : SERIAL NO.

notes

1. YEAR

Year	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Mark	A	B	C	D	E	F	G	H	J	K

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	3	4	5	6	7	8	9	A	B	C

b) Location of Lot Mark

Serial NO. is printed on the label. The label is attached to the front side of the Left Source PCB.
This is subject to change without prior notice.

9-2. Packing Form

a) Package quantity in one Pallet : 144 pcs

b) Pallet Size : 1400mm(W) X 900mm(D) X 1200mm(H)

10. Precautions

Please pay attention to the followings when you use this TFT LCD module.

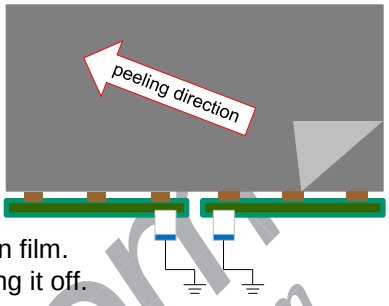
10-1. Handling Precautions

(1) Please attach the surface transparent protective film to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
(2) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(3) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
(4) After removing the protective film, when the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzine.
Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
(5) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(6) Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly. Panel ground path should be connected to metal ground.
(7) Please make sure to avoid external forces applied to the Source PCB and D-IC during the process of handling or assembling the TV set. If not, it causes panel damage or malfunction.
(8) Panel and BLU should be protected from the static electricity. If not, it causes IC damage.
(9) Do not pull or fold the source D-IC which connect the source PCB and the panel.
(10) Panel(board ass'y) should be put on the BLU structure precisely to avoid mechanical impact.
(11) FFC Cable should be connected between System board and Source PCB correctly.
(12) Mechanical structure for backlight system should be designed for sustaining board ass'y safely.
(13) Surface temperature of the Source D-IC should be controlled under 100℃ with TV Set status. If not, problems such as IC damage or decrease of lifetime could occur.

10-2. Operating Precautions

(1) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(2) Brightness depends on the temperature. (In lower temperature, it becomes lower.) And in lower temperature, Stable time(required time that brightness is stable after turned on) becomes longer
(3) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(4) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(5) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.

10-3. Protection Film



(1) Please keep attaching the protection film before assembly.
(2) Please peel off the protection film slowly.
(3) Please peel off the protection film just like shown in the Fig.1
(4) Ionized air should be blown over during the peeling.
(5) Source PCB should be connected to the ground when peel off the protection film.
(6) The protection film should not be contacted to the source D-IC during peeling it off.

< Fig. 1 >

10-4. Storage Precautions

When storing modules as spares for a long time, the following precautions are necessary.

(1) Temperature : 5 ~ 40 ℃
(2) Humidity : 35 ~ 75 %RH
(3) Period : 6 months
(4) Control of ventilation and temperature is necessary.
(5) Please make sure to protect the product from strong light exposure, water or moisture. Be careful for condensation.
(6) Please keep the modules at a circumstance shown below Fig. 2

< Fig. 2 >

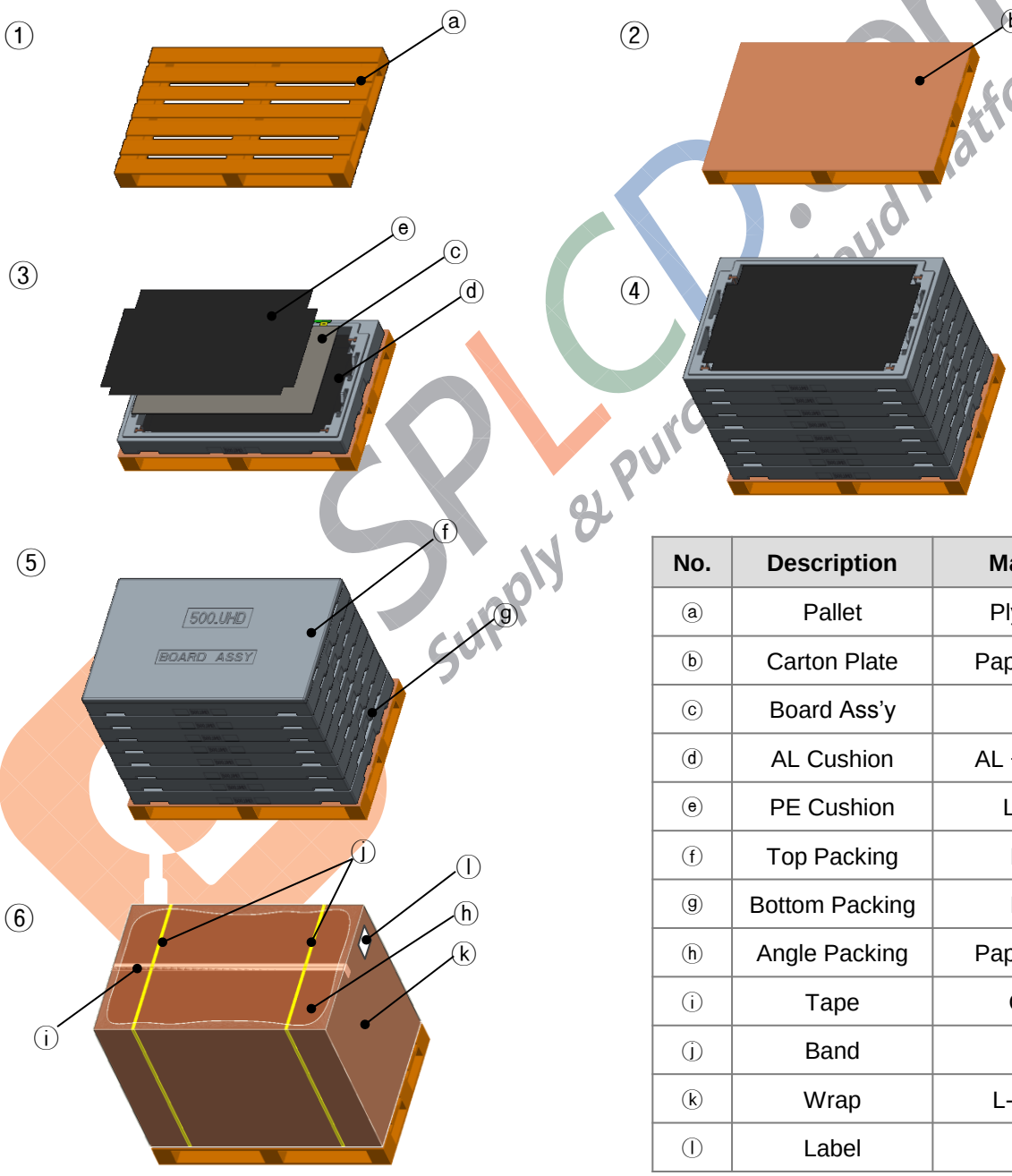
10-5. Packing Precautions

Product assembled into module should be stored in the Al-bag(cover case).

APPENDIX- Ⅰ -1

■ Pallet Ass'y

a) B/Ass'y Qty + PE Sheet / Box : 18pcs + 19pcs
b) B/Ass'y Qty / Pallet : 144pcs
c) Box Qty / Pallet : 8Box



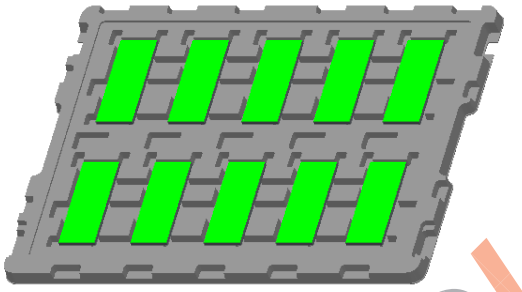
No.	Description	Material
ⓐ	Pallet	Plywood
ⓑ	Carton Plate	Paper(SW)
ⓒ	Board Ass'y	-
ⓓ	AL Cushion	AL + LDPE
ⓔ	PE Cushion	LDPE
ⓕ	Top Packing	EPS
ⓖ	Bottom Packing	EPS
ⓗ	Angle Packing	Paper(SW)
ⓘ	Tape	OPP
ⓙ	Band	PP
ⓚ	Wrap	L-LDPE
ⓛ	Label	PP

APPENDIX- Ⅰ - 2

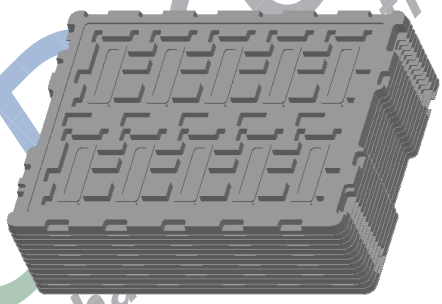
■ Control PCB Packing Ass'y

a) Control PCB Qty / Box : 144 pcs
b) Tray Qty / Box : 16Tray (Uppermost Tray Is empty)
c) Tray Size : 466 X 353 X 16
d) Box Size : 468 X 355 X 202

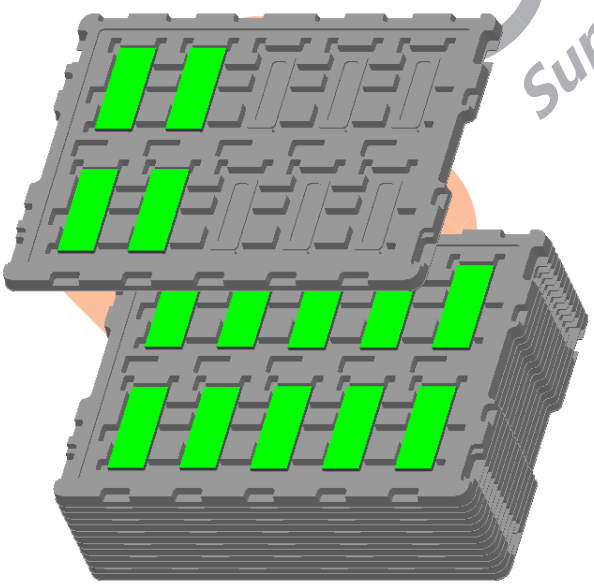
[10pcs/Tray]



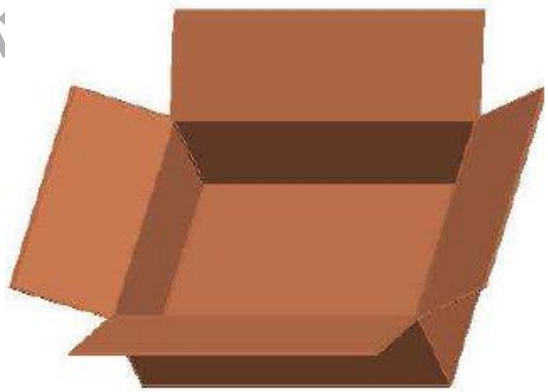
[15Tray+Empty Tray]



[10pcs/14Tray+4pcs/1tray]



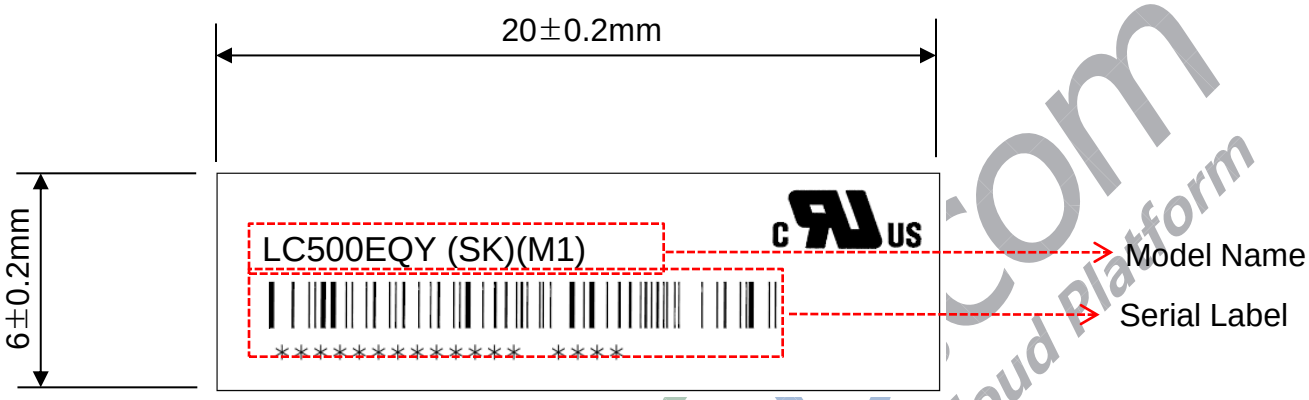
[Inserting into Box]



No.	Description	Material
1	PCB Packing Ass'y	-
2	Tray	PET
3	Box	SWR4

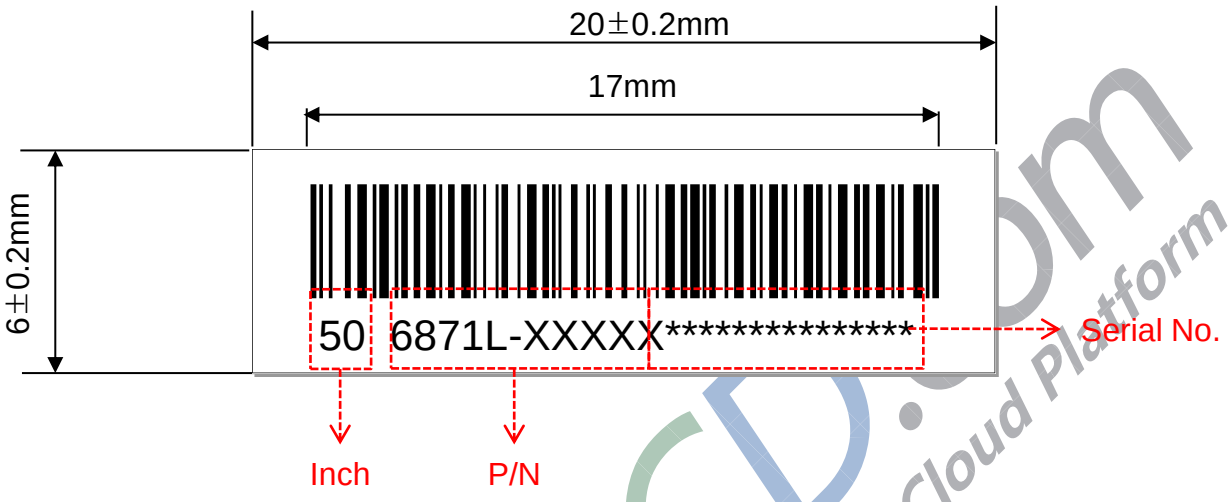
APPENDIX- II -1

■ Serial Label



■ Serial No. (See CAS page 22 for more information)

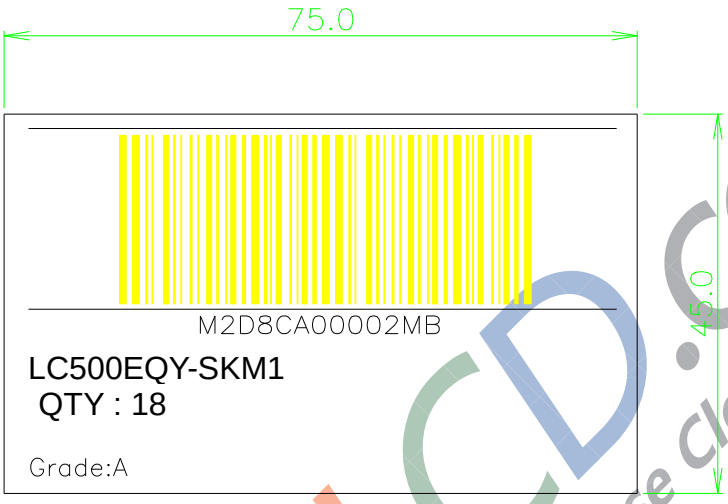
■ Control PCB Label



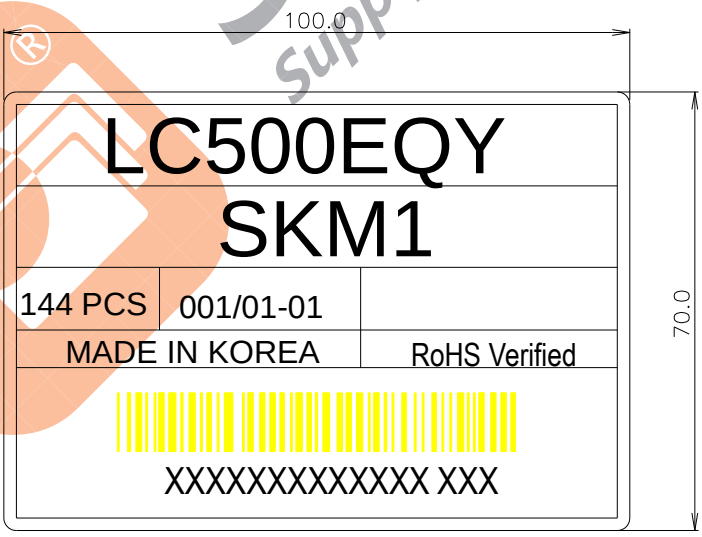
■ Control PCB Box Label

 # APPENDIX- II -2

■ BOX Label

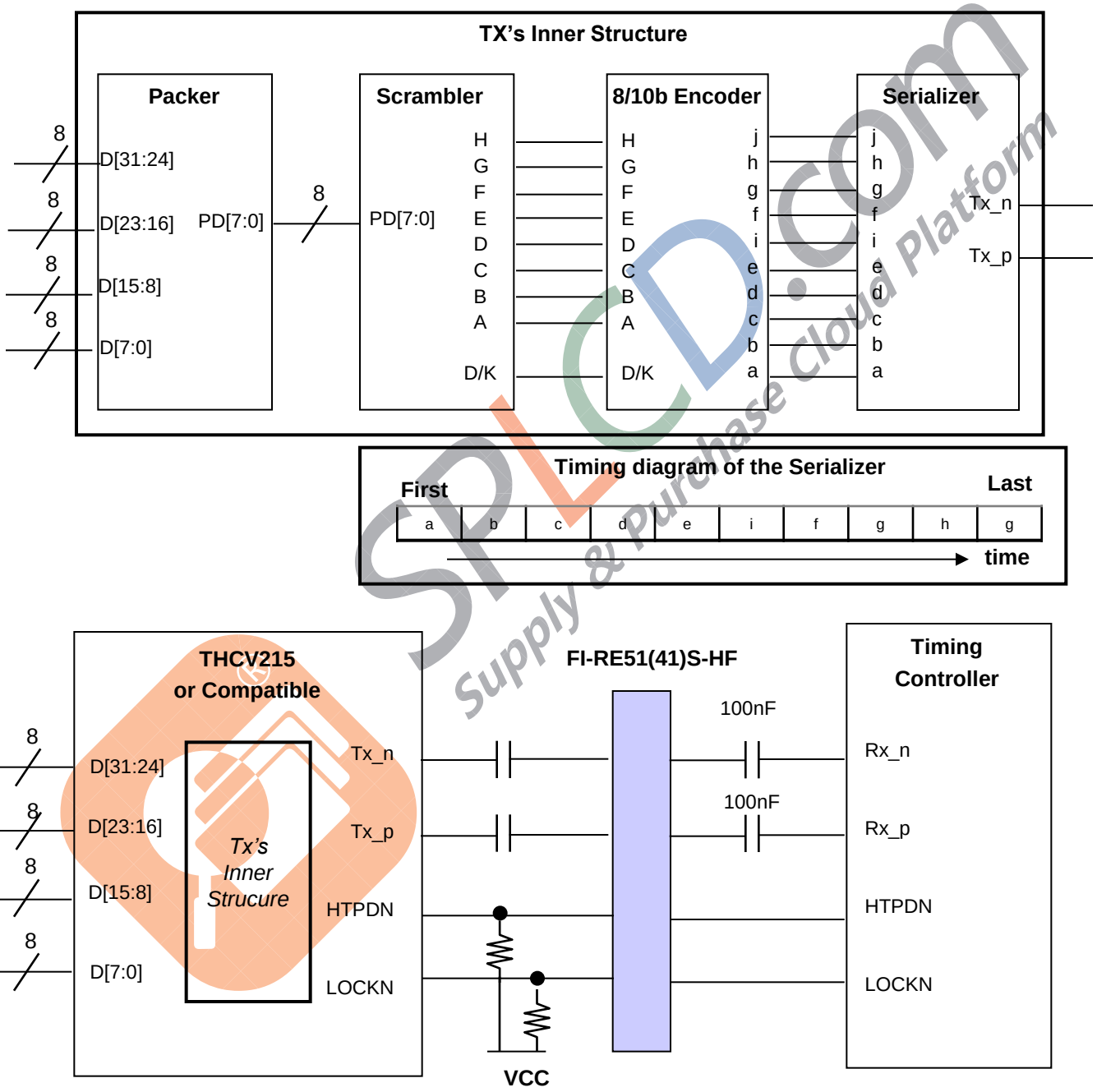


■ Pallet Label



APPENDIX- III

■ Required signal assignment for Flat Link (Thine : THCV215) Transmitter

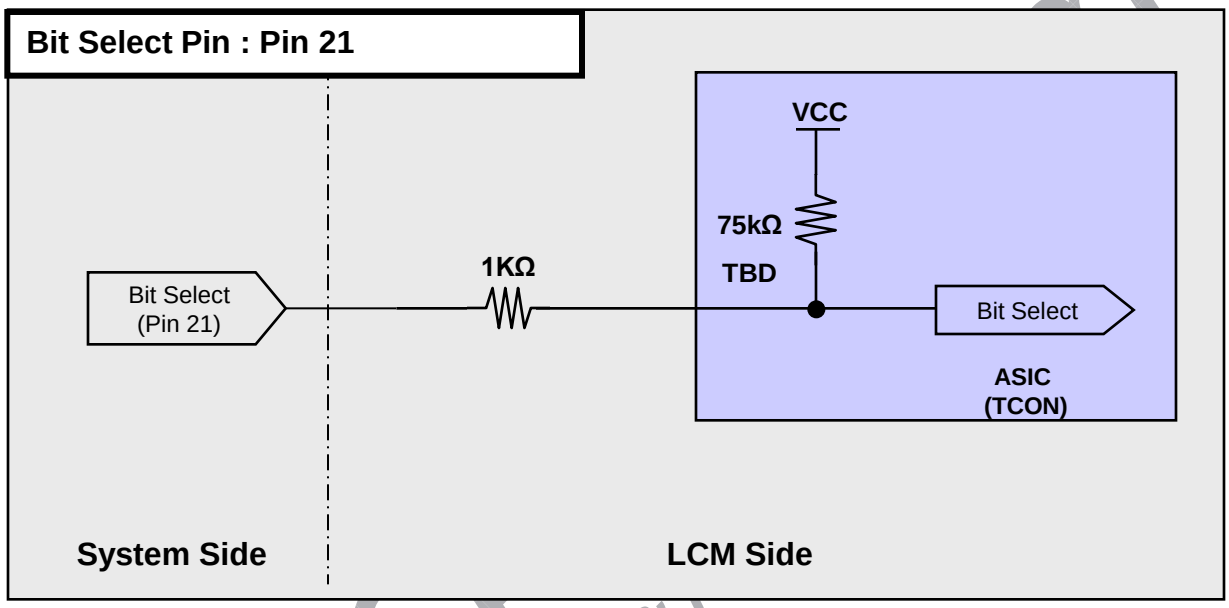


notes: 1. The LCD module uses a 100 nF capacitor on positive and negative lines of each receiver input.
2. Refer to Vx1 Transmitter Data Sheet for detail descriptions. (THCV215 or Compatible)
3. About Module connector pin configuration, Please refer to the Page 6.

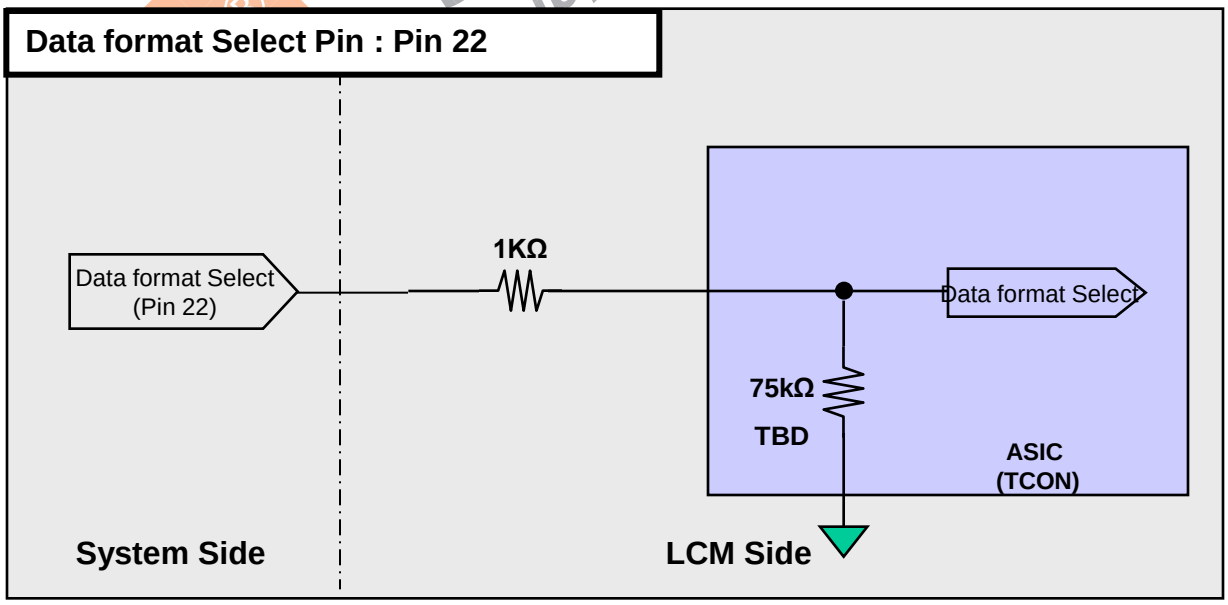
APPENDIX- Ⅳ-1

■ Option Pin Circuit Block Diagram

3) Circuit Block Diagram of Bit Selection pin



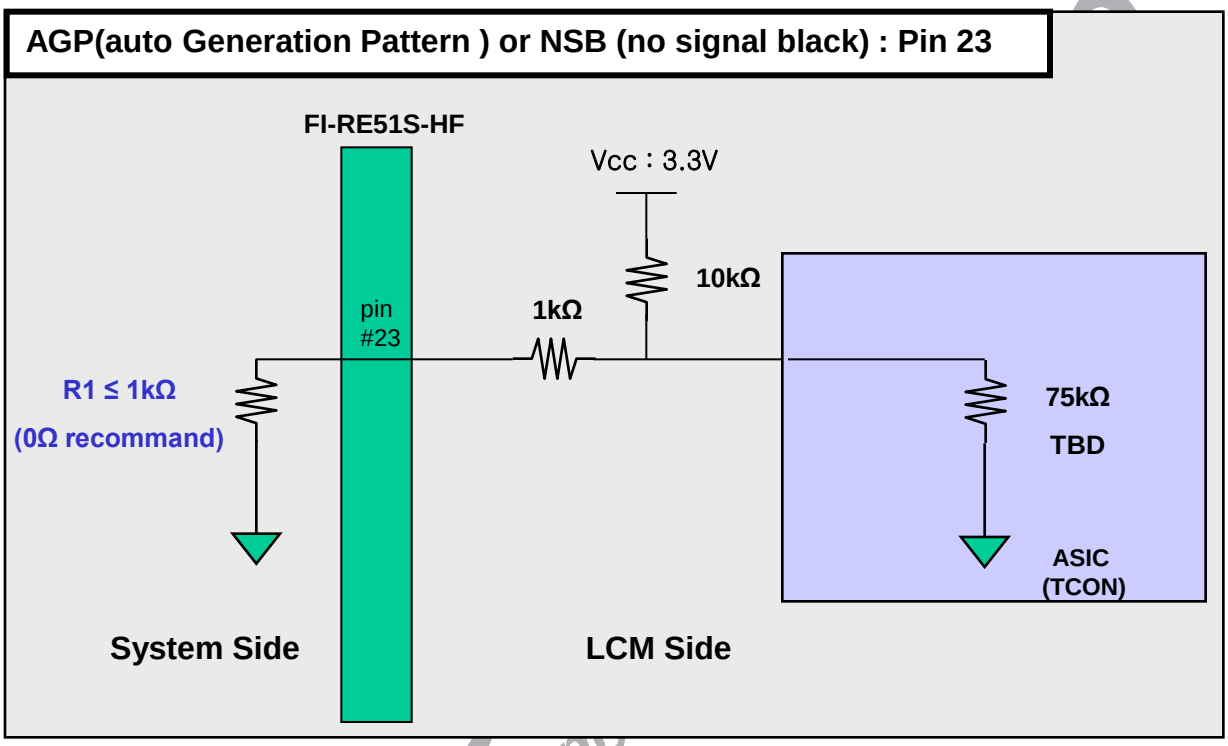
4) Circuit Block Diagram of Data format Selection pin



APPENDIX- Ⅳ-2

■ Option Pin Circuit Block Diagram

5) Circuit Block Diagram of AGP Selection pin

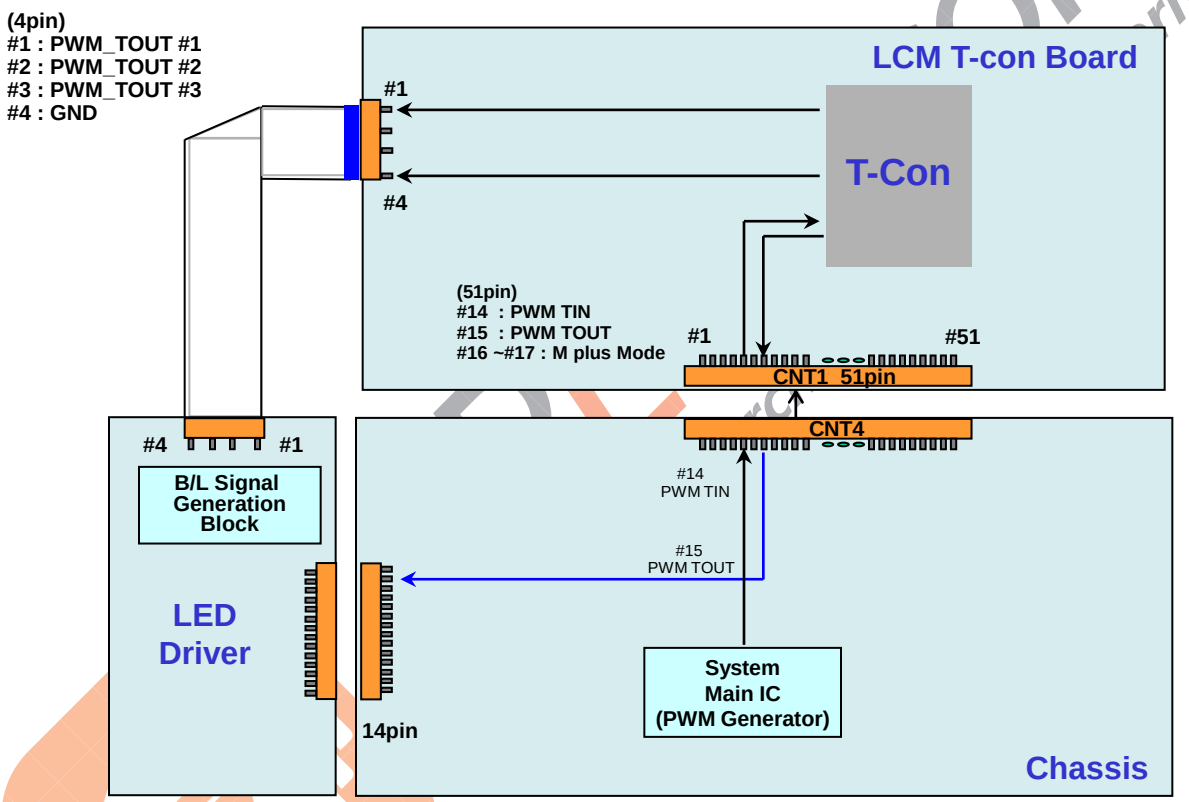


APPENDIX-V

■ Scanning Design Guide

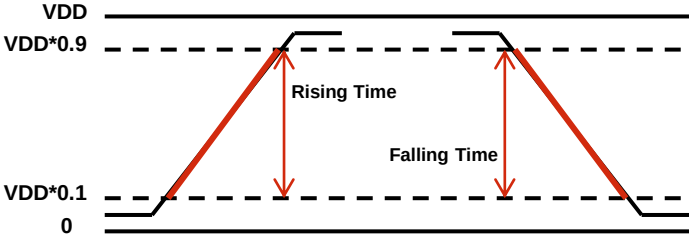
◇ When Mplus Enable is “L", PWM TOUT = System Dimming.
PWM TOUT signals are synchronized with V-Sync Freq. of System in T-Con Board.
#15 PWM TOUT Pin must be connected to LED Driver, In case of non-Scanning mode.

◇ LCD Connector(CN4): FN100-Z04B-C20 (manufactured by UJU Electronics)



◇ PWM Specification (VDD = 3.3V)
1. PWM High Voltage Range : 2.5V~3.6V
2. PWM Low Voltage Range : 0.0V~0.7V

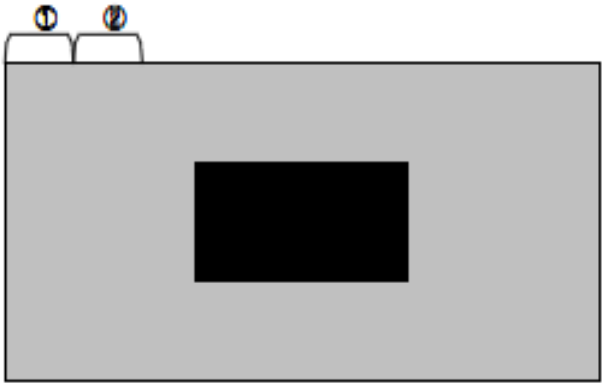
EXTVBR-B Frequency	100 Hz for PAL 120 Hz for NTSC
Rising Time	MAX 10.0 μs
Falling Time	MAX 10.0 μs



APPENDIX- VI

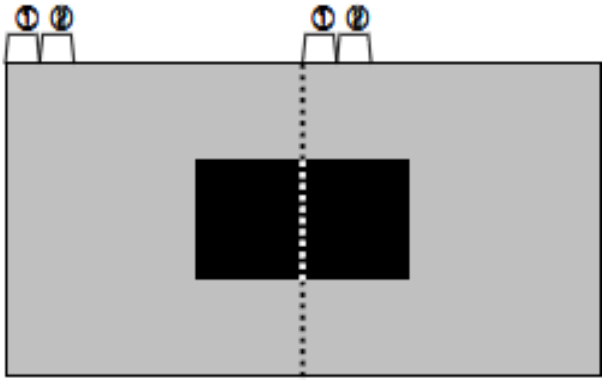
■ Input mode of pixel data

Mode 1 : Non-Division



Lane	1st Data	2nd Data	Data#
Lane0	1	9	3833
Lane1	2	10	3834
Lane2	3	11	3835
Lane3	4	12	3836
Lane4	5	13	3837
Lane5	6	14	3838
Lane6	7	15	3839
Lane7	8	16	3840

Mode 2 : 2 Division

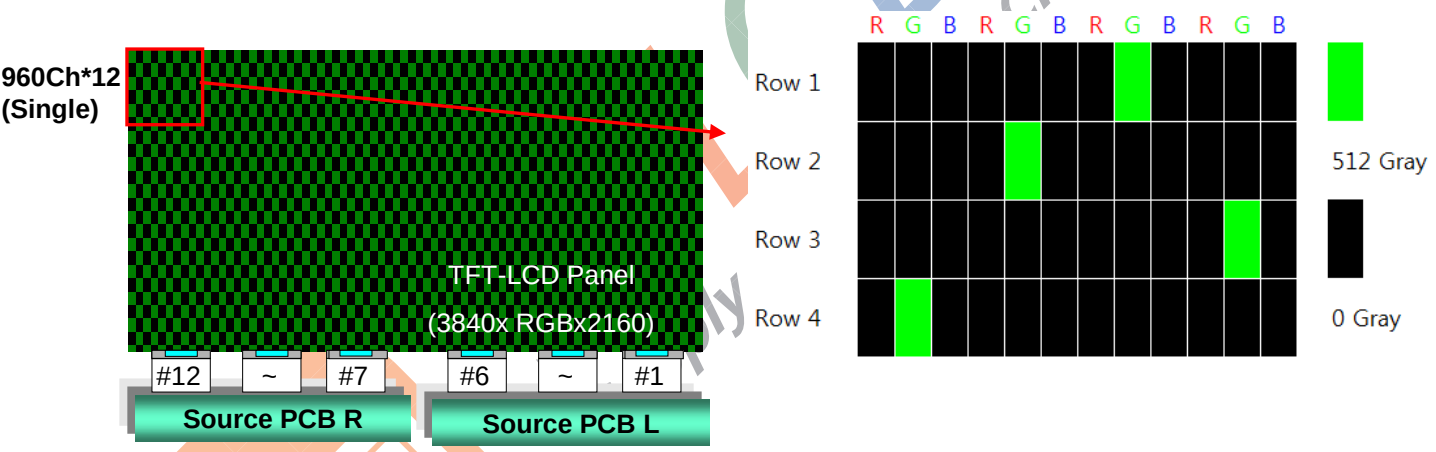


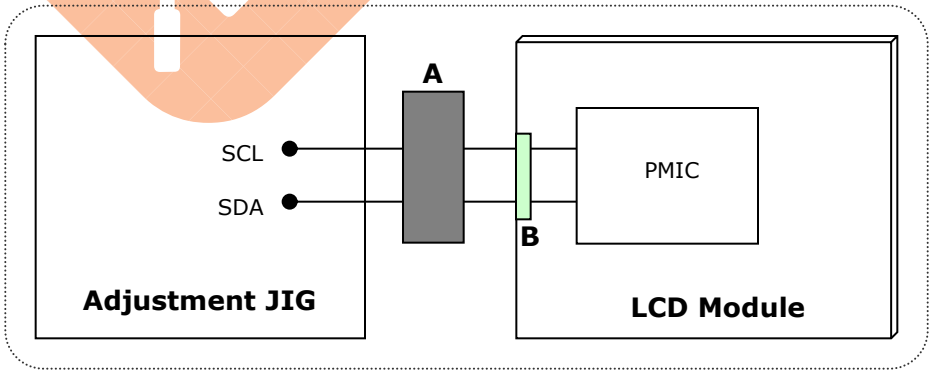
Lane	1st Data	2nd Data	Data#
Lane0	1	5	1917
Lane1	2	6	1918
Lane2	3	7	1919
Lane3	4	8	1920
Lane4	1921	1925	3837
Lane5	1922	1926	3838
Lane6	1923	1927	3839
Lane7	1924	1928	3840

APPENDIX-VII-1

■ Flicker Adjustment

Parameter	Unit	Min	Typ	Max	Note
Inversion Method	-	V2Dot Inversion			
Adjust Pattern / Gray Level	-	V2Dot Full Flicker / 512Gray			
Position	-	Center			
Voltage range	V	4.9V (TBD)	5.4V (TBD)	5.9V (TBD)	





A : Pull-up Resistors (If it is necessary)

B : I2C Connector (Refer to Appendix IX)

APPENDIX-VII-2

Vcom Adjustment

MODULE 51 Pin CNT(CN1) PIN CONFIGURATION

Pin No	Description	Note
1~15	-	
18	SDA	
19	SCL	
20	NC	
21~22	-	
23		
24~51	-	

LC500EQY-SKM1 Control PCB Assembly uses Richtek PWM IC(RT6923).
PWM IC (Slave) Address is 40h (01000000), Vcom Register address is 0x16.

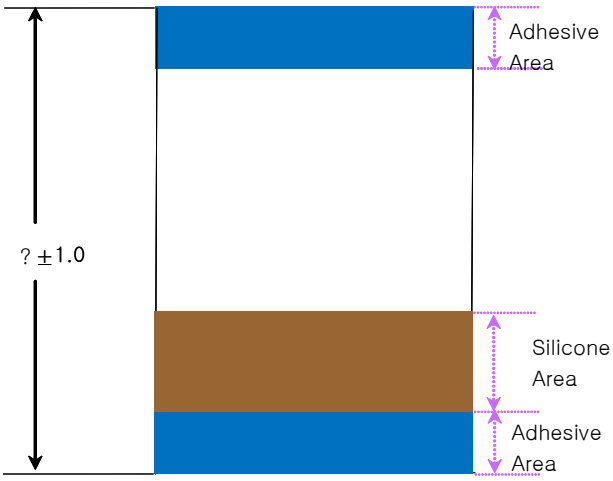
If you need detailed information, Please refer to Richtek PWM IC(RT6923) Data Sheet or contact with Richtek company.

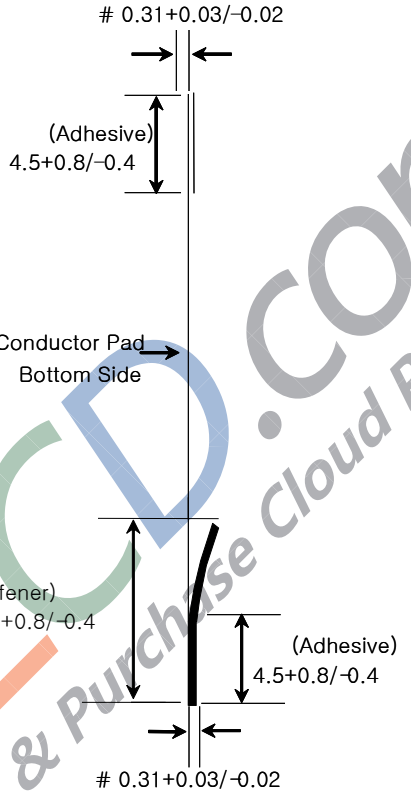
APPENDIX- VIII

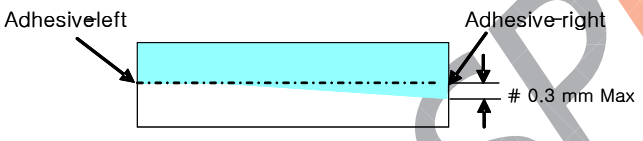
■ The reference method of BL dimming

It is recommended to use synchronous V-sync frequency to prevent waterfall
(Vsync * 2 =P-Dim Frequency)

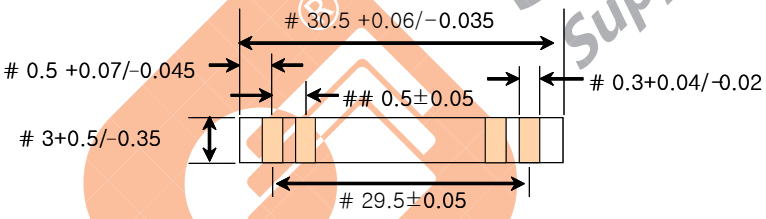
APPENDIX-IX







< Pad Detail- 60Pin >



◈ Note

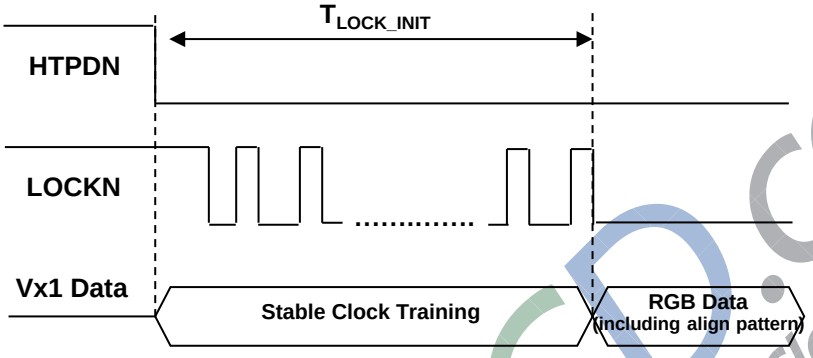
- Pad : GOLD Plating
- # ≥ Cpk 1.0
- ## ≥ Cpk 1.33
- Stiffener color : Sky Blue
- H-F
- Dimensions unit : mm

- Material List

APPLICATION	STANDARD	MATERIAL	REFERENCE
1. CONDUCTOR	GOLD PLATED COPPER WIRE	1. 99.99% COPPER 2. GOLD PLATED	1. Tolerance - THICKNESS: ±0.01 - WIDTH: +0.04 -0.02 2. ELOGATION(%) : 10 MORE THAN 3. TENSION : (KGF) 0.2 MORE THAN 4. GOLD THICKNESS : 0.05 μm MIN *MAKER : TAIHAN ELECTRIC plating process : 3 MICRON/SUNEUN
2. INSULATION	POLYESTER FILM (PET/PET)	1. POLYESTER BASE FILM : 0.025 mm 2. POLYESTER HOTMELT ADHESIVE : 0.035 mm TOTAL THICKNESS : 0.060 mm	UL VW-1 FLAME Width : 120mm Length : 500M UNIT : ROLL * MAKER : SHINCHANG HOTMELT/ COSMOAMT
3. SUPPORTING TAPE	POLYESTER FILM	1. POLYESTER BASE FILM : 0.188 mm 2. POLYESTER HOTMELT ADHESIVE : 0.027 mm TOTAL THICKNESS : 0.215 mm	Width : 20.5mm Length : 250M Unit : ROLL *MAKER : SUNGSHIN Trading/ COSMOAMT
4. SILICON TAPE (BROWN)		TOTAL THICKNESS : 0.065 mm	*MAKER : DAEHYUN ST

APPENDIX- X-1

■ Vx1 Initialization Characteristics

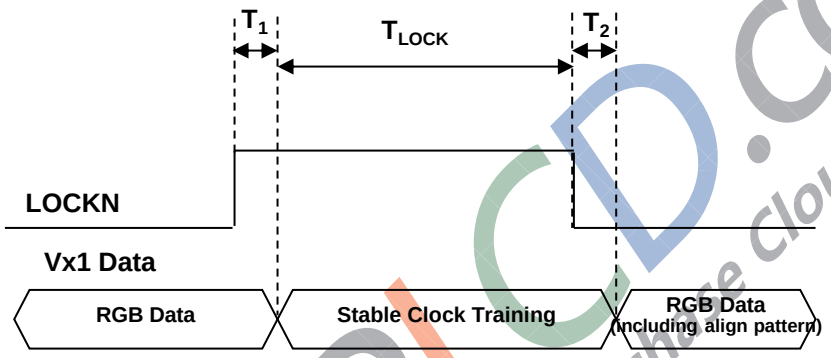


1) UHD60Hz T-Con

Characteristics	Symbol	Min	Typ	Max	Unit
Initial CDR lock time (From Stable CDR training to CDR lock)	T_{LOCK_INT}	0		310	ms

APPENDIX- X-2

■ Vx1 Lock Timing In Normal Operation



Characteristics	Symbol	Min	Typ	Max	Unit
CDR lock time from stable clock training pattern to LOCKN “Low” in normal operation	T_{LOCK}			2	ms
Latency from LOCKN “High” to clock training pattern	T_1			100	us
Latency from clock “Low” to normal RGB Data	T_2			100	us

※ Vx1 Rx should get clock training pattern in T_1

※ Vx1 Rx should get RGB Data (including align pattern) in T_2