

LC550MUT
Liquid Crystal Display

Product Specification

SPECIFICATION FOR APPROVAL

() Preliminary Specification

() Final Specification

Title	55.0" WUXGA TFT LCD
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BUYER	LGE
LCD MODEL	LC550MUT-SCA1
SET MODEL	

SUPPLIER	LG Display Co., Ltd.
*MODEL	LC550MUT
SUFFIX	SCA1

*When you obtain standard approval,
please use the above model name without suffix

APPROVED BY	SIGNATURE	DATE
/		
/		
/		

Please return 1 copy for your confirmation with
your signature and comments.

APPROVED BY	SIGNATURE	DATE
- /Team Leader		
REVIEWED BY		
- / Project Leader		
PREPARED BY		
- / Engineer		

TV Product Development Dept.
LG Display Co., Ltd.

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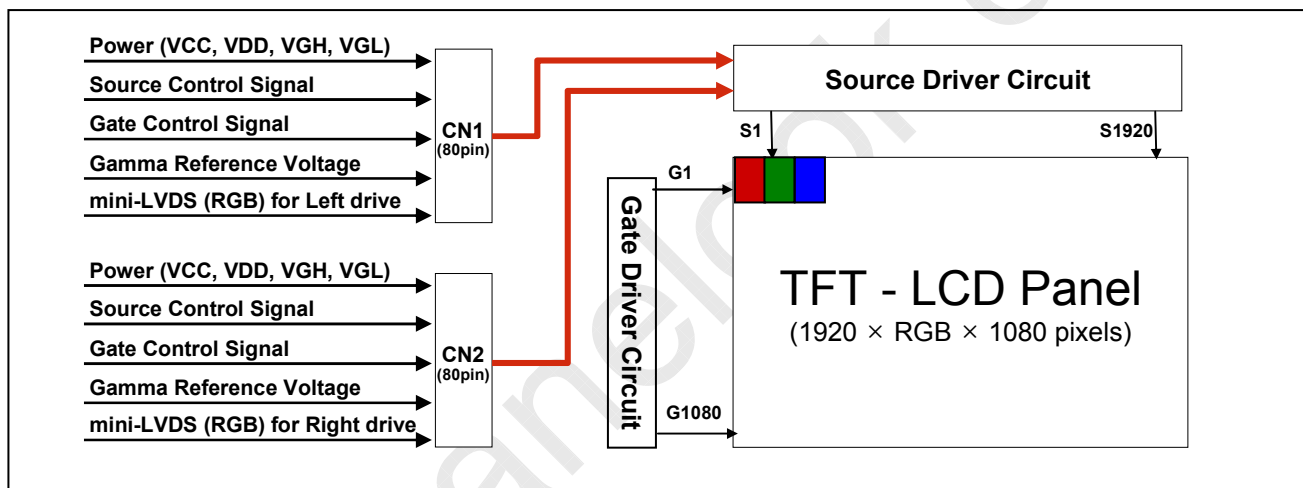
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1. General Description

The **LC550MUT** is a Color Active Matrix Liquid Crystal Display with an integral Source PCB and the nine of Gate Drive IC (GD-IC) at each side. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive display type which is operating in the normally black mode. It has a 54.64 inch diagonally measured active display area with WUXGA resolution progressive mode (1080 vertical by 1920 horizontal pixel array).

Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arrayed in vertical stripes. Gray scale or the luminance of the sub-pixel color is determined with a 8-bit gray scale signal for each dot. Therefore, it can present a palette of more than 16.7M colors.

It is intended to support LCD TV, PCTV where high brightness, super wide viewing angle, high color gamut, high color depth and fast response time are important.



General Features

Active Screen Size	54.64 inches(1387.8mm) diagonal
Outline Dimension	1220.8 (H) x 693.8 (V) x1.94 (D) (Typ.)
Pixel Pitch	0.630 mm x 0.630 mm
Pixel Format	1920 horiz. by 1080 vert. Pixels, RGB stripe arrangement
Color Depth	8-bit, 16.7 M colors
Drive IC Data Interface	Source D-IC : 8-bit mini-LVDS, and control signals TTL Gate D-IC : Line on Glass (LOG) Through Source D-IC
Viewing Angle (CR>10)	Viewing angle free (R/L 178 (Min.), U/D 178 (Min.))
Power Consumption	14.04[W] with LGE T-con
Weight	3.4kg(Typ)
Display Mode	Transmissive mode, Normally black
Surface Treatment	Hard coating(3H), Anti-glare treatment of front polarizer

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2. Absolute Maximum Ratings

The following items are maximum values which, if exceeded, may cause faulty operation or damage to the LCD module.

Table 1. ABSOLUTE MAXIMUM RATINGS

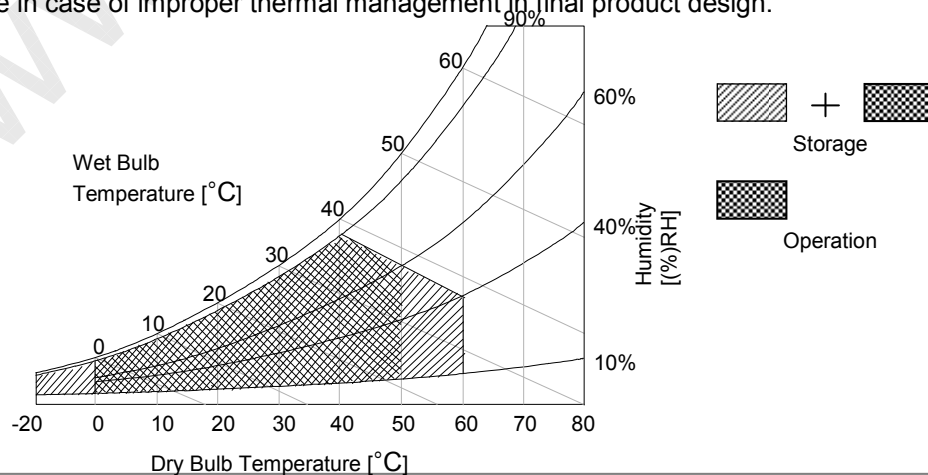
Parameter	Symbol	Value		Unit	Note
		Min	Max		
Logic Power Voltage	VCC	-0.5	+4.0	V _{DC}	1
Gate High Voltage	VGH	+18.0	+30.0	V _{DC}	
Gate Low Voltage	VGL	-8.0	-4.0	V _{DC}	
Source D-IC Analog Voltage	VDD	-0.3	+18.0	V _{DC}	
Gamma Ref. Voltage (Upper)	VGMH	$\frac{1}{2}VDD-0.5$	$VDD+0.5$	V _{DC}	
Gamma Ref. Voltage (Low)	VGML	-0.3	$\frac{1}{2}VDD+0.5$	V _{DC}	
Panel Front Temperature	T _{SUR}	-	+68	°C	4
Operating Temperature	T _{OP}	0	+50	°C	2,3
Storage Temperature	T _{ST}	-20	+60	°C	
Operating Ambient Humidity	H _{OP}	10	90	%RH	
Storage Humidity	H _{ST}	10	90	%RH	

Note: 1. Ambient temperature condition ($T_a = 25 \pm 2^\circ\text{C}$)

2. Temperature and relative humidity range are shown in the figure below. Wet bulb temperature should be Max 39 °C and no condensation of water.

3. Gravity mura can be guaranteed below 40 °C condition.

4. The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 68 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 68 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.





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3. Electrical Specifications

3-1. Electrical Characteristics

It requires several power inputs. The VCC is the basic power of LCD Driving power sequence, Which is used to logic power voltage of Source D-IC and Gate D-IC.

Table 2. ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Note
Logic Power Voltage	VCC	-	3.0	3.3	3.6	V _{DC}	
Logic High Level Input Voltage	V _{IH}		2.7		VCC	V _{DC}	
Logic Low Level Input Voltage	V _{IL}		0		0.6	V _{DC}	
Source D-IC Analog Voltage	VDD	-	15.8	16	16.2	V _{DC}	
Half Source D-IC Analog Voltage	H_VDD	-	7.9	8.0	8.1	V _{DC}	
Gamma Reference Voltage	V _{GMH}	(GMA1 ~ GMA9)	½*VDD		VDD-0.2		
	V _{GML}	(GMA10 ~ GMA18)	0.2		½*VDD		
Common Voltage	V _{com}	-		6.13		V	
Mini-LVDS Clock frequency	CLK	3.0V≤VCC ≤3.6V			312	MHz	
mini-LVDS input Voltage (Center)	V _{IB}	Mini-LVDS Clock and Data	0.7 + (V _{ID} /2)		(VCC-1.2) – V _{ID} / 2	V	5
mini-LVDS input Voltage Distortion (Center)	ΔV _{IB}				0.8	V	
mini-LVDS differential Voltage range	V _{ID}		150		800	mV	
mini-LVDS differential Voltage range Dip	ΔV _{ID}		25		800	mV	
Gate High Voltage	V _{GH}		27.7	28.0	28.3	V _{DC}	
Gate Low Voltage	V _{GL}		-5.5	-5.0	-5.1	V _{DC}	
Gate High Modulation Voltage	V _{GHM}			28		V	
Total Power Current	I _{LCD}	-		1170		mA	2
Total Power Consumption	P _{LCD}	-		14.04		Watt	2

- Note:
1. The specified current and power consumption are under the V_{LCD}=12V., 25 ± 2°C, f_v=120Hz condition whereas mosaic pattern(8 x 6) is displayed and f_v is the frame frequency.
 2. The specified current and power consumption are measured with LGE T-con.
 3. All of the typical gate voltage should be controlled within 1% voltage level
 4. Ripple voltage level is recommended under 10%
 5. In case of mini-LVDS signal spec, refer to Fig 2 for the more detail.
 6. Logic Level Input Signal : SOE,POL,GSP,H_CONV,OPT_N
 7. HVDD Voltage level is half of VDD and it should be between Gamma9 and Gamma10

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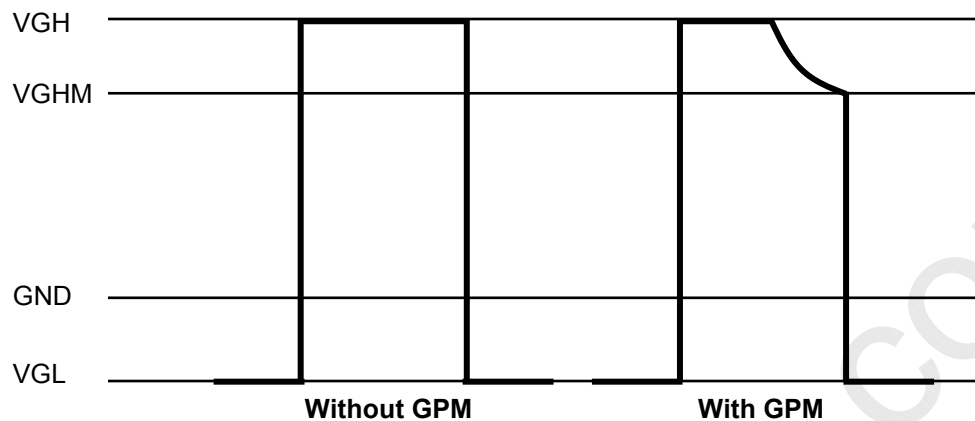


FIG. 1 Gate Output Wave form without GPM and with GPM

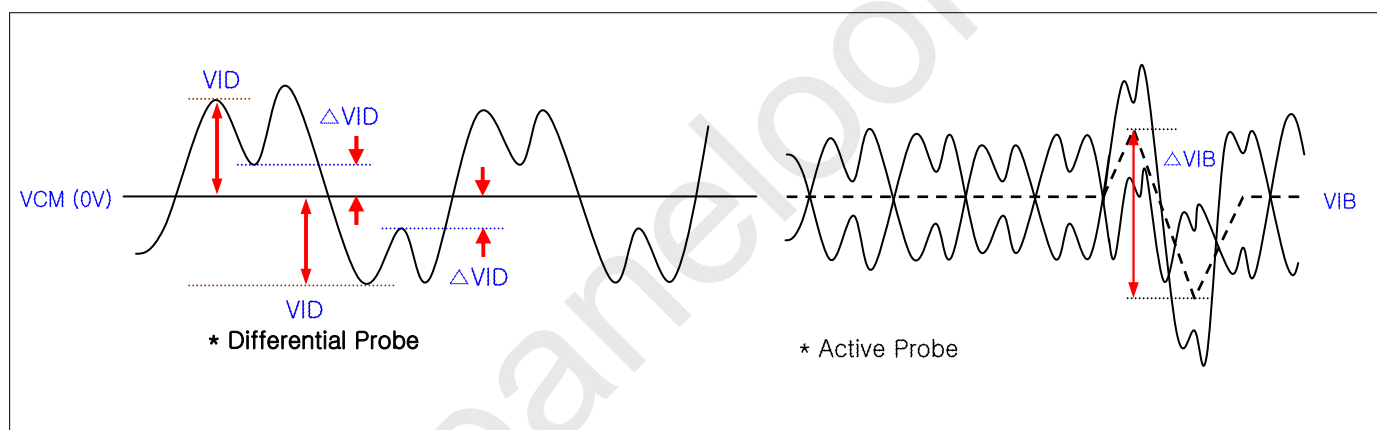


FIG. 2 Description of VID, Δ VIB, Δ VID

* Source PCB

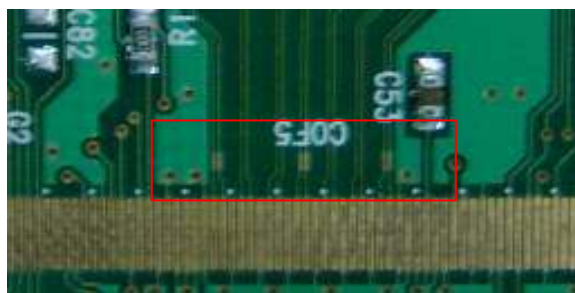


FIG. 3 Measure point

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3-2. Interface Connections

This LCD module employs two 80pin connector of interface connection, Each 80 pin connectors are used for the module electronics.

3-2-1. LCD Module

- LCD Connector : TF06L-80S-0.5SH (Manufactured by HIROSE or Equivalent)

Table 4-1. Source PCB CONNECTOR(CN5) PIN CONFIGURATION

No	Symbol	Description	No	Symbol	Description
1	GND	Ground	41	SOE	SOURCE OUTPUT ENABLE
2	LLV0 +	Left Mini LVDS Receiver Signal(0+)	42	GND	Ground
3	LLV0 -	Left Mini LVDS Receiver Signal(0-)	43	GMA 1	GAMMA VOLTAGE 1
4	LLV1 +	Left Mini LVDS Receiver Signal(1+)	44	GMA 2	N.C
5	LLV1 -	Left Mini LVDS Receiver Signal(1-)	45	GMA 3	GAMMA VOLTAGE 3
6	LLV2 +	Left Mini LVDS Receiver Signal(2+)	46	GMA 4	GAMMA VOLTAGE 4
7	LLV2 -	Left Mini LVDS Receiver Signal(2-)	47	GMA 5	GAMMA VOLTAGE 5
8	GND	Ground	48	GMA 6	GAMMA VOLTAGE 6
9	LLVCLK+	Left Mini LVDS Receiver Clock(+)	49	GMA 7	N.C
10	LLVCLK-	Left Mini LVDS Receiver Clock(-)	50	GMA 9	GAMMA VOLTAGE 9
11	GND	Ground	51	GMA 10	GAMMA VOLTAGE 10
12	LLV3 +	Left Mini LVDS Receiver Signal(3+)	52	GMA 12	N.C
13	LLV3 -	Left Mini LVDS Receiver Signal(3-)	53	GMA 13	GAMMA VOLTAGE 13
14	LLV4 +	Left Mini LVDS Receiver Signal(4+)	54	GMA 14	GAMMA VOLTAGE 14
15	LLV4 -	Left Mini LVDS Receiver Signal(4-)	55	GMA 15	GAMMA VOLTAGE 15
16	LLV5 +	Left Mini LVDS Receiver Signal(5+)	56	GMA 16	GAMMA VOLTAGE 16
17	LLV5 -	Left Mini LVDS Receiver Signal(5-)	57	GMA 17	N.C
18	GND	Ground	58	GMA 18	GAMMA VOLTAGE 18
19	LRV0 +	Left Mini LVDS Receiver Signal(0+)	59	GND	Ground
20	LRV0 -	Left Mini LVDS Receiver Signal(0-)	60	GND	Ground
21	LRV1 +	Left Mini LVDS Receiver Signal(1+)	61	Z_OUT	LTD OUTPUT
22	LRV1 -	Left Mini LVDS Receiver Signal(1-)	62	GND	Ground
23	LRV2 +	Left Mini LVDS Receiver Signal(2+)	63	VCOML_OUT	LEFT VCOM OUTPUT
24	LRV2 -	Left Mini LVDS Receiver Signal(2-)	64	VCOML_FB	LEFT VCOM Feedback
25	GND	Ground	65	GND	Ground
26	LRVCLK+	Left Mini LVDS Receiver Clock(+)	66	VGH	Gate High Voltage
27	LRVCLK-	Left Mini LVDS Receiver Clock(-)	67	GND	Ground
28	GND	Ground	68	GSC	GATE SHIFT CLOCK
29	LRV3 +	Left Mini LVDS Receiver Signal(3+)	69	GOE	GATE OUTPUT ENABLE
30	LRV3 -	Left Mini LVDS Receiver Signal(3-)	70	GND	Ground
31	LRV4 +	Left Mini LVDS Receiver Signal(4+)	71	VGL	Gate Low Voltage
32	LRV4 -	Left Mini LVDS Receiver Signal(4-)	72	GND	Ground
33	LRV5 +	Left Mini LVDS Receiver Signal(5+)	73	HVDD	DRIVER POWER SUPPLY VOLTAGE
34	LRV5 -	Left Mini LVDS Receiver Signal(5-)	74	HVDD	DRIVER POWER SUPPLY VOLTAGE
35	GND	Ground	75	GND	Ground
36	OPT_N	N.C	76	VCC	LOGIC POWER SUPPLY VOLTAGE
37	H_CONV	HORIZONTAL 2 DOT INVERSION SIGNAL	77	VCC	LOGIC POWER SUPPLY VOLTAGE
38	GSP	GATE START PULSE	78	GND	Ground
39	POL	POLARITY OUTPUT SIGNAL	79	VDD	DRIVER POWER SUPPLY VOLTAGE
40	GND	Ground	80	VDD	DRIVER POWER SUPPLY VOLTAGE

Notes : 1. More detail Information refer to application notes.

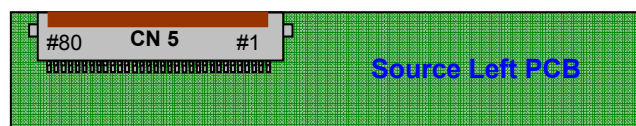
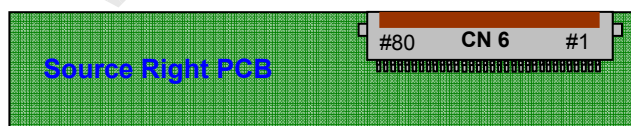
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Table 4-2. Source PCB CONNECTOR (CN6) PIN CONFIGURATION

No	Symbol	Description	No	Symbol	Description
1	VDD	DRIVER POWER SUPPLY VOLTAGE	41	POL	POLARITY OUTPUT SIGNAL
2	VDD	DRIVER POWER SUPPLY VOLTAGE	42	GND	Ground
3	GND	Ground	43	SOE	SOURCE OUTPUT ENBLE
4	VCC	LOGIC POWER SUPPLY VOLTAGE	44	H_CONV	HORIZONTAL 2 DOT INVERSION SIGNAL
5	VCC	LOGIC POWER SUPPLY VOLTAGE	45	OPT_N	N.C
6	GND	Ground	46	GND	Ground
7	HVDD	DRIVER POWER SUPPLY VOLTAGE	47	RLV0 +	Right Mini LVDS Receiver Signal(0+)
8	HVDD	DRIVER POWER SUPPLY VOLTAGE	48	RLV0 -	Right Mini LVDS Receiver Signal(0-)
9	GND	Ground	49	RLV1 +	Right Mini LVDS Receiver Signal(1+)
10	OPT_P	N.C	50	RLV1 -	Right Mini LVDS Receiver Signal(1-)
11	VGL	Gate Low Voltage	51	RLV2 +	Right Mini LVDS Receiver Signal(2+)
12	GND	Ground	52	RLV2 -	Right Mini LVDS Receiver Signal(2-)
13	GOE	GATE OUTPUT ENABLE	53	GND	Ground
14	GSC	GATE SHIFT CLOCK	54	RLVCLK+	Right Mini LVDS Receiver Clock(+)
15	GND	Ground	55	RLVCLK-	Right Mini LVDS Receiver Clock(-)
16	VGH	Gate High Voltage	56	GND	Ground
17	GND	Ground	57	RLV3 +	Right Mini LVDS Receiver Signal(3+)
18	VCOMR_FB	RIGHT VCOM OUTPUT	58	RLV3 -	Right Mini LVDS Receiver Signal(3-)
19	VCOMR_OUT	RIGHT VCOM Feedback	59	RLV4 +	Right Mini LVDS Receiver Signal(4+)
20	GND	Ground	60	RLV4 -	Right Mini LVDS Receiver Signal(4-)
21	Z_OUT	LDT OUTPUT	61	RLV5 +	Right Mini LVDS Receiver Signal(5+)
22	GND	Ground	62	RLV5 -	Right Mini LVDS Receiver Signal(5-)
23	GMA 1	GAMMA VOLTAGE 1	63	GND	Ground
24	GMA 2	N.C	64	RRV0 +	Right Mini LVDS Receiver Signal(0+)
25	GMA 3	GAMMA VOLTAGE 3	65	RRV0 -	Right Mini LVDS Receiver Signal(0-)
26	GMA 4	GAMMA VOLTAGE 4	66	RRV1 +	Right Mini LVDS Receiver Signal(1+)
27	GMA 5	GAMMA VOLTAGE 5	67	RRV1 -	Right Mini LVDS Receiver Signal(1-)
28	GMA 6	GAMMA VOLTAGE 6	68	RRV2 +	Right Mini LVDS Receiver Signal(2+)
29	GMA 7	N.C	69	RRV2 -	Right Mini LVDS Receiver Signal(2-)
30	GMA 9	GAMMA VOLTAGE 9	70	GND	Ground
31	GMA 10	GAMMA VOLTAGE 10	71	RRVCLK+	Right Mini LVDS Receiver Clock(+)
32	GMA 12	N.C	72	RRVCLK-	Right Mini LVDS Receiver Clock(-)
33	GMA 13	GAMMA VOLTAGE 13	73	GND	Ground
34	GMA 14	GAMMA VOLTAGE 14	74	RRV3 +	Right Mini LVDS Receiver Signal(3+)
35	GMA 15	GAMMA VOLTAGE 15	75	RRV3 -	Right Mini LVDS Receiver Signal(3-)
36	GMA 16	GAMMA VOLTAGE 16	76	RRV4 +	Right Mini LVDS Receiver Signal(4+)
37	GMA 17	N.C	77	RRV4 -	Right Mini LVDS Receiver Signal(4-)
38	GMA 18	GAMMA VOLTAGE 18	78	RRV5 +	Right Mini LVDS Receiver Signal(5+)
39	Ground	Ground	79	RRV5 -	Right Mini LVDS Receiver Signal(5-)
40	GSP	GATE START PULSE	80	GND	Ground

Notes : 1. More detail Information refer to application notes.



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3-3. Signal Timing Specifications

Table 6. Timing Requirements

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Mini Clock pulse period	T ₁		3.2	3.4		ns	1
Mini Clock pulse low period	T ₂		1.6	-	-	ns	
Mini Clock pulse high period	T ₃		1.6	-	-	ns	
Mini Data setup time	T ₆		0.55	-	-	ns	
Mini Data hold time	T ₇		0.55	-	-	ns	
Reset low to SOE rising time	T ₈		0	-	-	ns	
SOE to Reset input time	T ₉		200	-	-	ns	
Receiver off to SOE timing	T ₁₀		10	-	-	CLK cycle	
POL signal to SOE setup time	T ₁₁		-5	-	-	ns	
POL signal to SOE hold time	T ₁₂		6	-	-	ns	
Reset High Period	T ₁₃		3			CLK cycle	
SOE signal GSP setup time	T ₁₄		100			ns	
SOE signal GSP Hold time	T ₁₅		100			ns	
SOE signal Pulse Width	T ₁₆		200			ns	

- Note :
- mini-LVDS timing measure conditions
: 268MHz < Clock Frequency < 312MHz, 150mV < VID < 800mV @ 3.0 < VCC < 3.3
 - Setup time and hold time should be satisfied at the same time

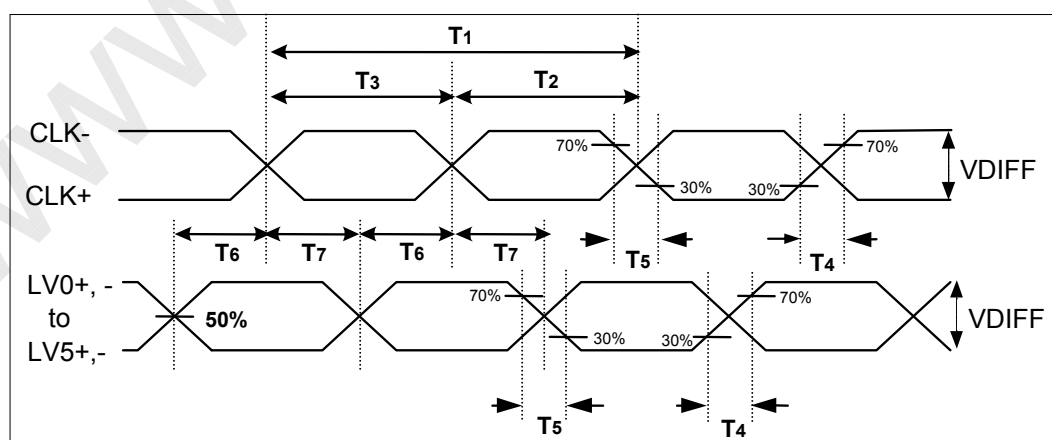


FIG 4. Source D-IC Input Data Latch Timing Waveform

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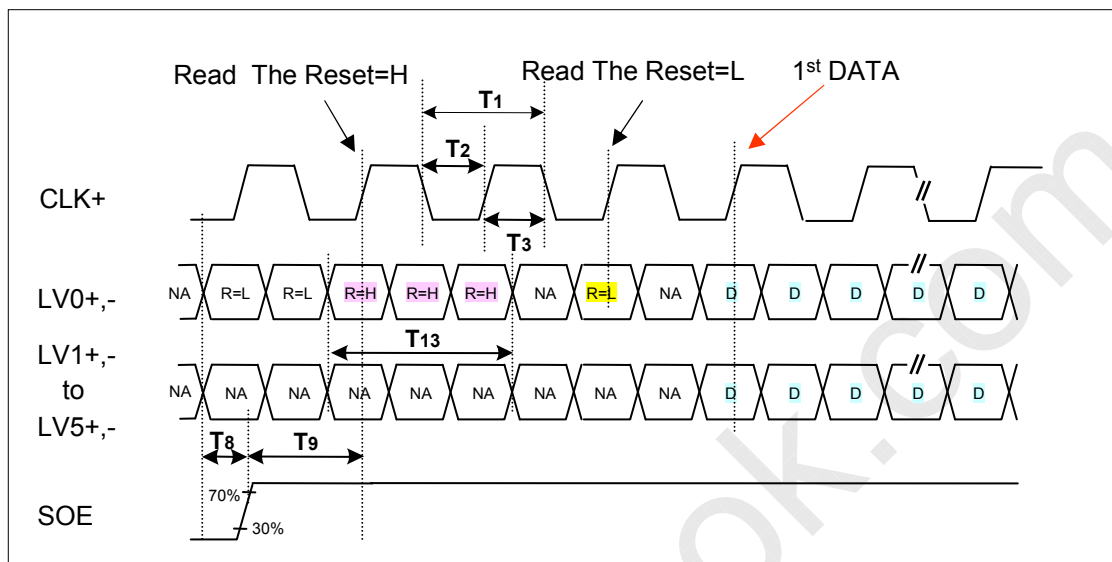
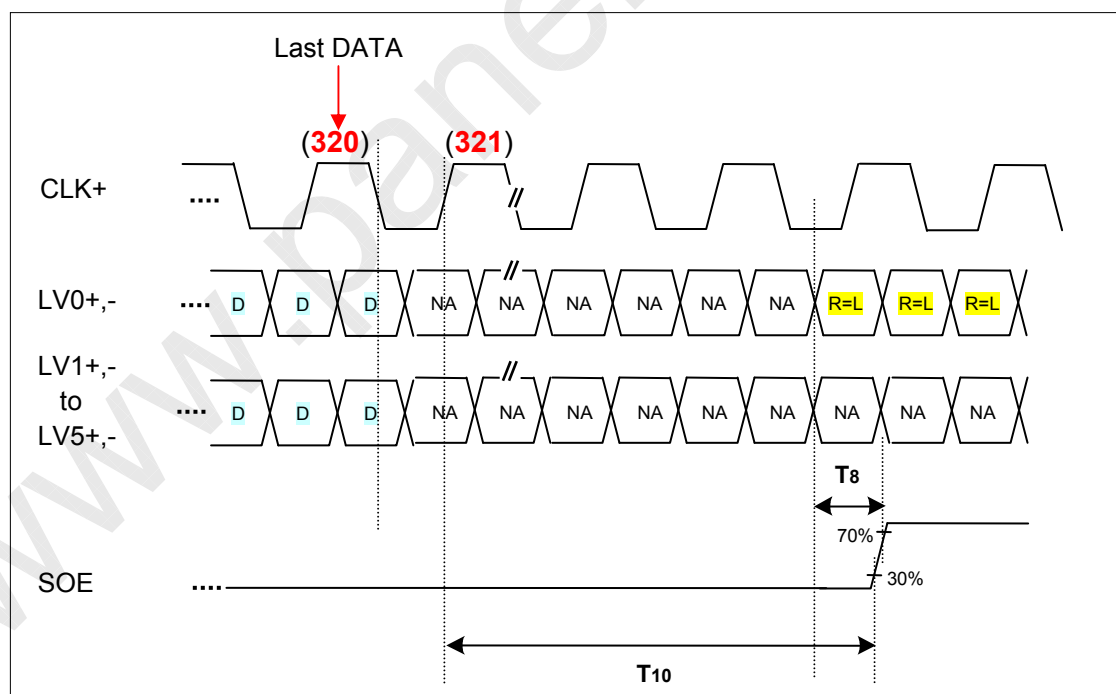
FIG 5-1. Input Data Timing for 1st Source D-IC Chip

FIG 5-2. Last Data Latch to SOE Timing

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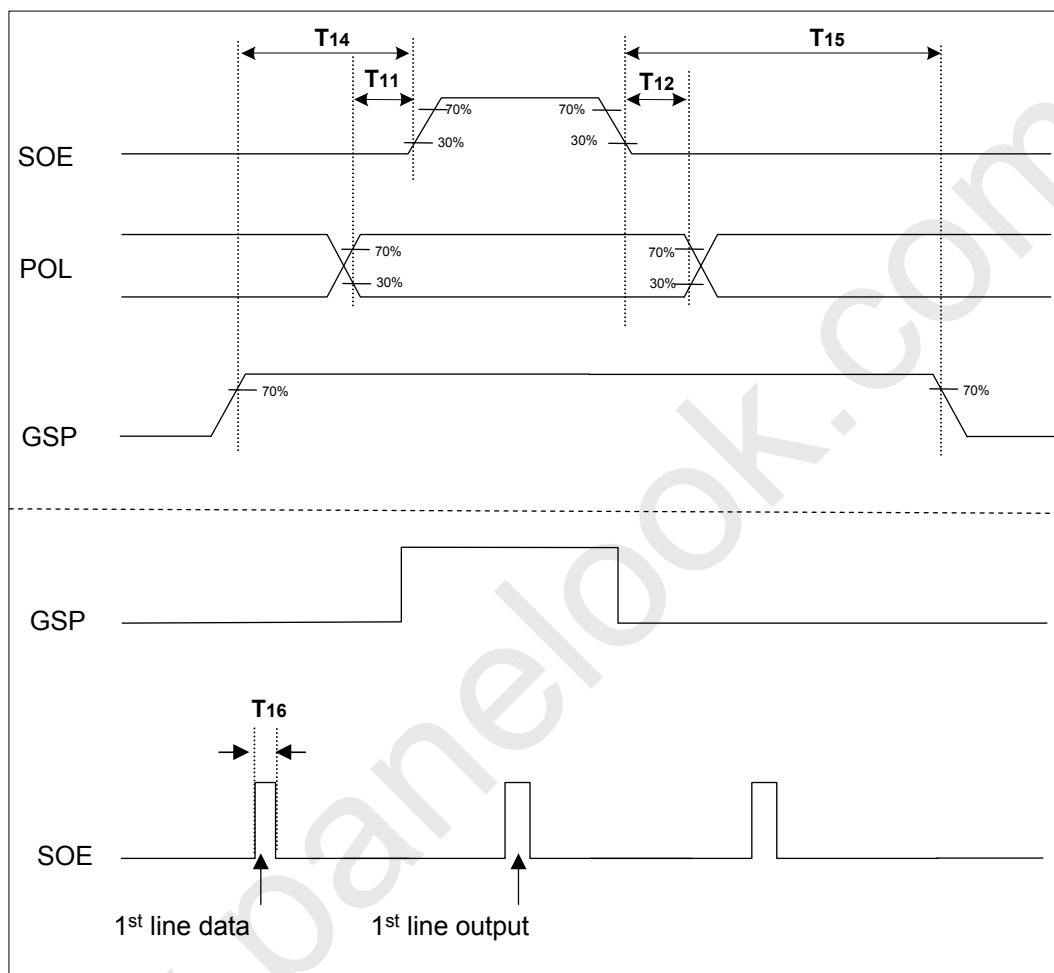


FIG 6. POL, GSP and SOE Timing Waveform

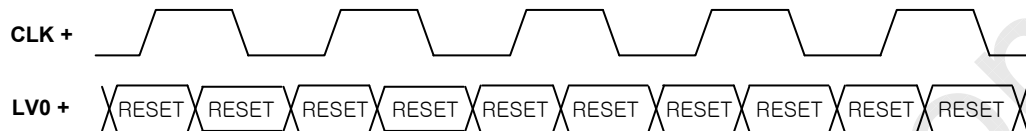
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3-4. Data Mapping and Timing

Display data and control signal (RESET) are input to **LV0** to **LV5**.

3-4-1. Control signal input mode



3-4-2. Display data input mode

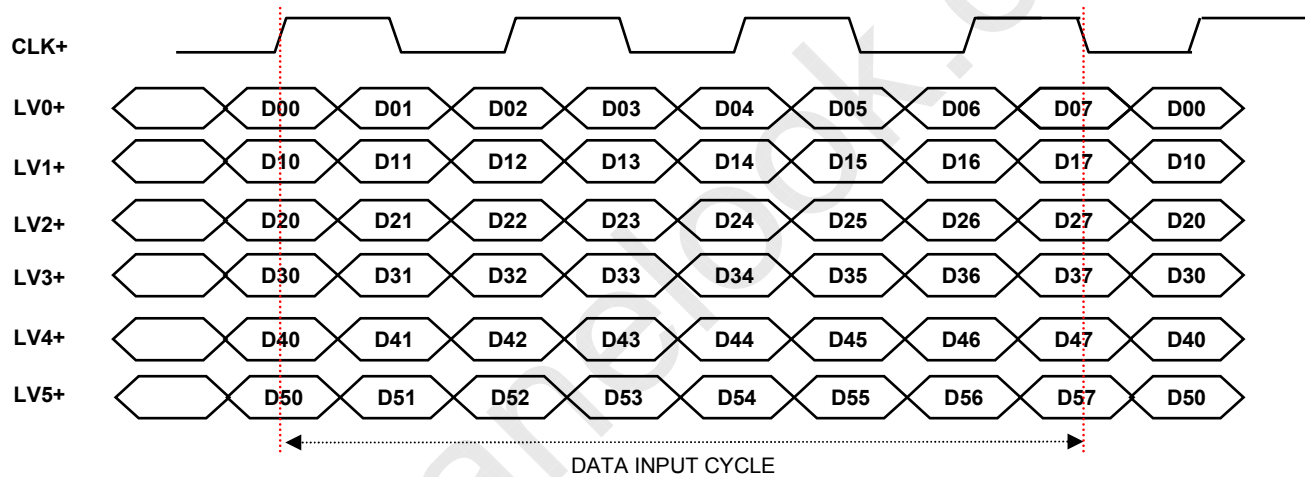


Fig. 7 Mini-LVDS Data

Note : 1. For data mapping, please refer to panel pixel structure Fig.8

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3-5. Panel Pixel Structure

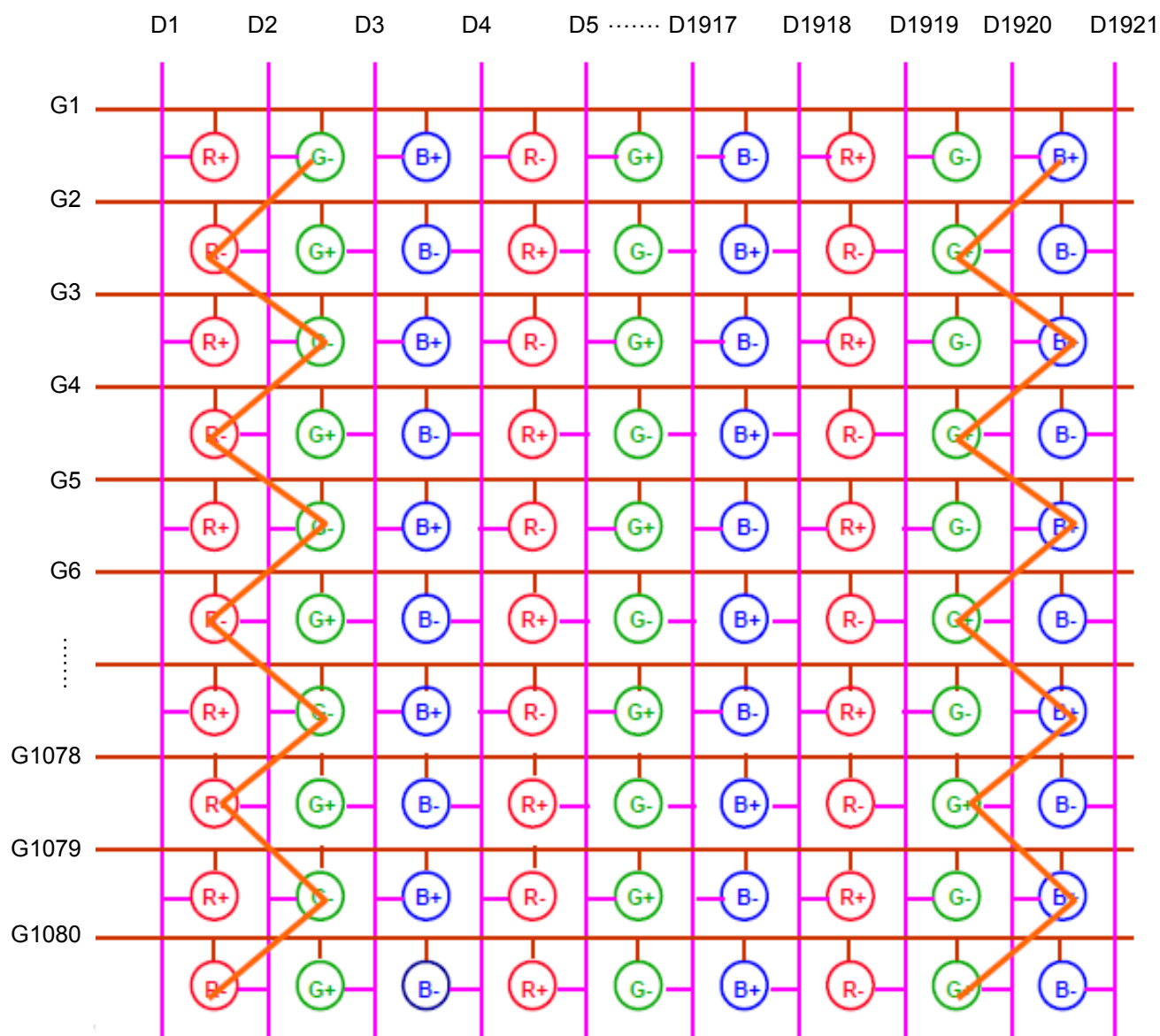


FIG. 8 Panel Pixel Structure

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3-6. Power Sequence

3-6-1. LCD Driving circuit

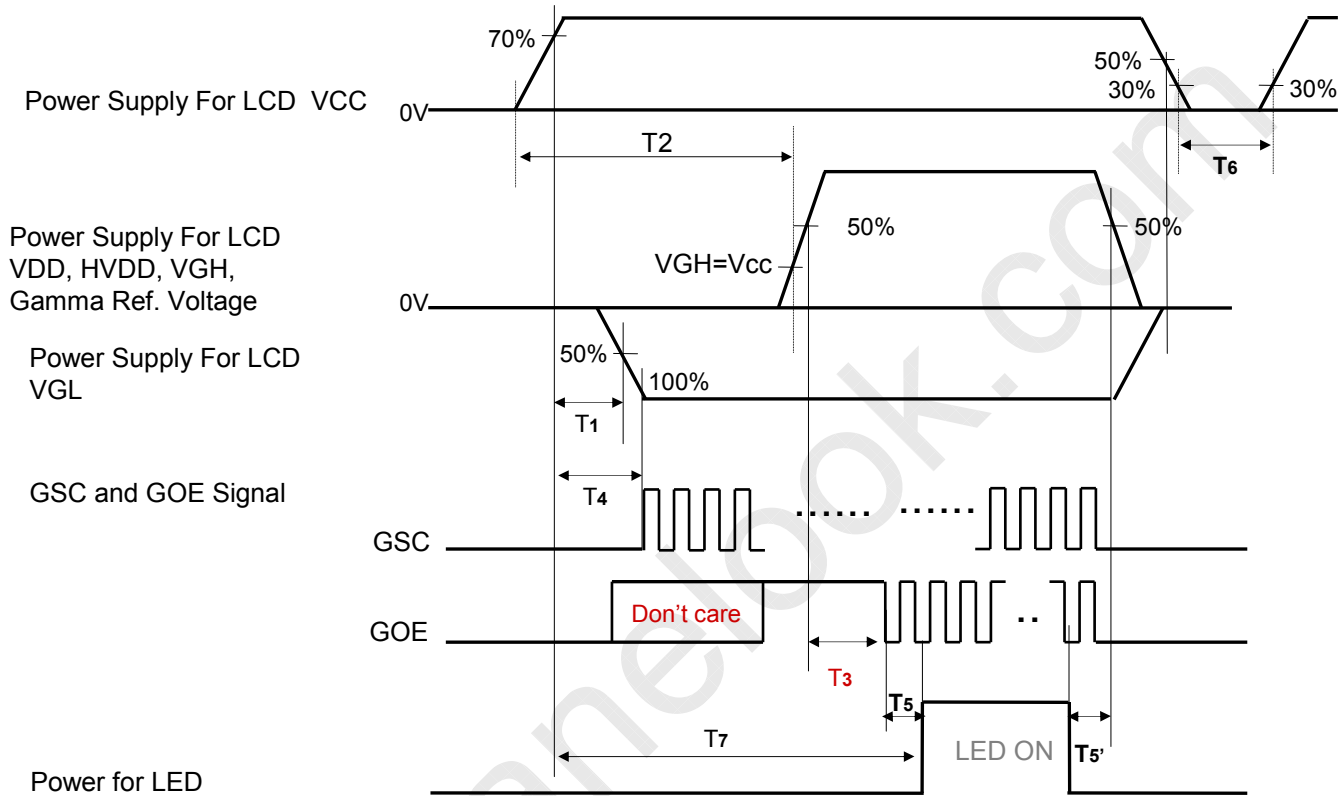


Table 7. POWER SEQUENCE

Ta= 25±2°C, fv=240Hz, Dclk=74.25MHz

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	0.5		-	ms	
T2	0.01		-	ms	
T3	5		-	ms	
T4	0		T2	ms	
T5 / T5'	500		-	ms	
T6	2		-	sec	
T7	0.5		-	s	

Note : 1. Power sequence for Source D-IC must follow the Case1 & 2.

※ Please refer to Appendix V for more details.

2. The Gate D-IC power on sequence must be VCC, VGL, logic input & VGH.

3. The 1st start of GSC is located between VGL and VGH.

4. GOE rising is before GSC.

5. Power off sequence order is reverse of power on sequence.

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4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable in a dark environment at $25\pm 2^{\circ}\text{C}$. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and θ equal to 0° .

FIG. 1 shows additional information concerning the measurement equipment and method.

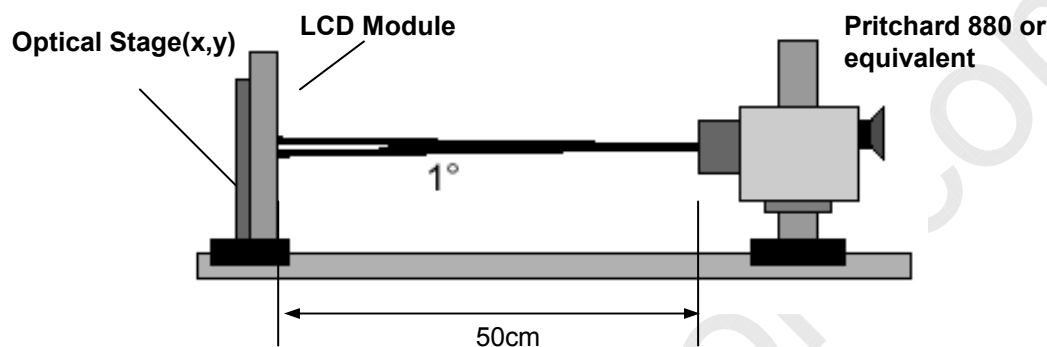


FIG. 1 Optical Characteristic Measurement Equipment and Method

Table 2. OPTICAL CHARACTERISTICS

 $T_a = 25\pm 2^{\circ}\text{C}$, VDD,VGH,VGL=typ., $f_v=240\text{Hz}$, Dclk=297MHz

Parameter		Symbol	Value			Unit	Note
			Min	Typ	Max		
Contrast Ratio		CR		1400(TBD)	-		
Response Time	Rising	Tr		5(TBD)			2
	Falling	Tf		5(TBD)		ms	2
Color Coordinates [CIE1931]	RED	Rx	Typ -0.03	0.651 (TBD)	Typ +0.03		With only color filter glass
		Ry		0.334 (TBD)			
	GREEN	Gx		0.312 (TBD)			
		Gy		0.598 (TBD)			
	BLUE	Bx		0.150 (TBD)			
		By		0.068 (TBD)			
Viewing Angle (CR>10)							
	x axis, right($\phi=0^{\circ}$)	θ_r	89	-	-	degree	3
	x axis, left ($\phi=180^{\circ}$)	θ_l	89	-	-		
	y axis, up ($\phi=90^{\circ}$)	θ_u	89	-	-		
	y axis, down ($\phi=270^{\circ}$)	θ_d	89	-	-		
Gray Scale			-	-	-		4

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Notes :1. Contrast Ratio(CR) is defined mathematically as :

$$CR = \frac{\text{Surface Luminance at position n with all white pixels}}{\text{Surface Luminance at position n with all black pixels}}$$

n = the Position number(1, 2, 3, 4, 5). For more information, see FIG 2.

2. Response time is the time required for the display to transition from G(0) to G(255) (Rise Time, Tr_R) and from G(0) to G(255) (Decay Time, Tr_D). For additional information see the FIG. 3.
3. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD module surface. For more information, see the FIG. 4.
4. Gray scale specification
Gamma Value is approximately 2.2. For more information, see the Table 3.

Table 3. GRAY SCALE SPECIFICATION

Gray Level	Luminance [%] (Typ.)		Gray Level	Gamma Ref.
L0	0.07	Positive Voltage	L0	Gamma9
L63	0.27			
L127	1.04		L63	Gamma6
L191	2.49		L127	Gamma5
L255	4.68		L191	Gamma4
L319	7.66		L223	Gamma3
L383	11.5		L255	Gamma1
L447	16.1			
L511	21.6	Negative Voltage	L255	Gamma18
L575	28.1		L223	Gamma16
L639	35.4		L191	Gamma15
L703	43.7		L127	Gamma14
L767	53.0		L63	Gamma13
L831	63.2			
L895	74.5			
L959	86.7		L0	Gamma10
L1023	100			

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Measuring point for surface luminance & measuring point for luminance variation.

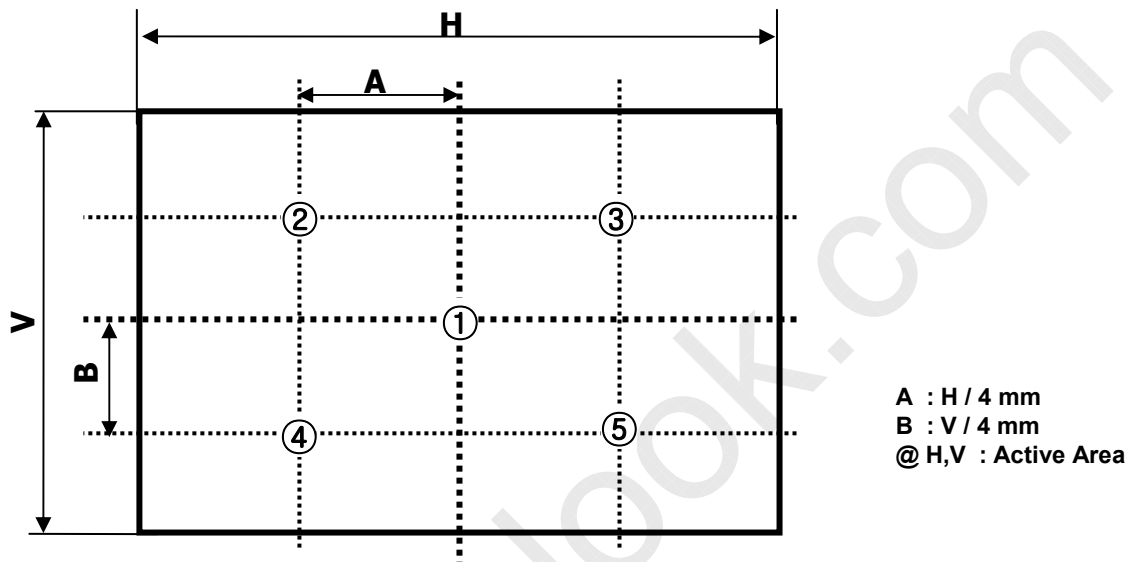


FIG. 9 5 Points for Luminance Measure

Response time is defined as the following figure and shall be measured by switching the input signal for "Gray(0)" and "Gray(255)".

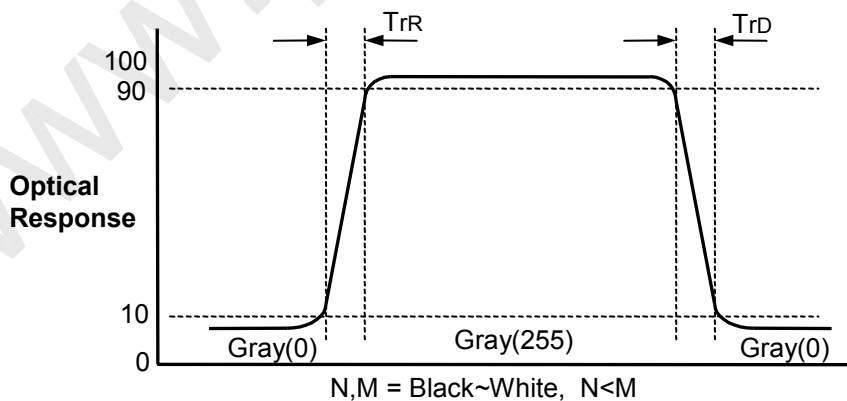


FIG. 10 Response Time

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Dimension of viewing angle range

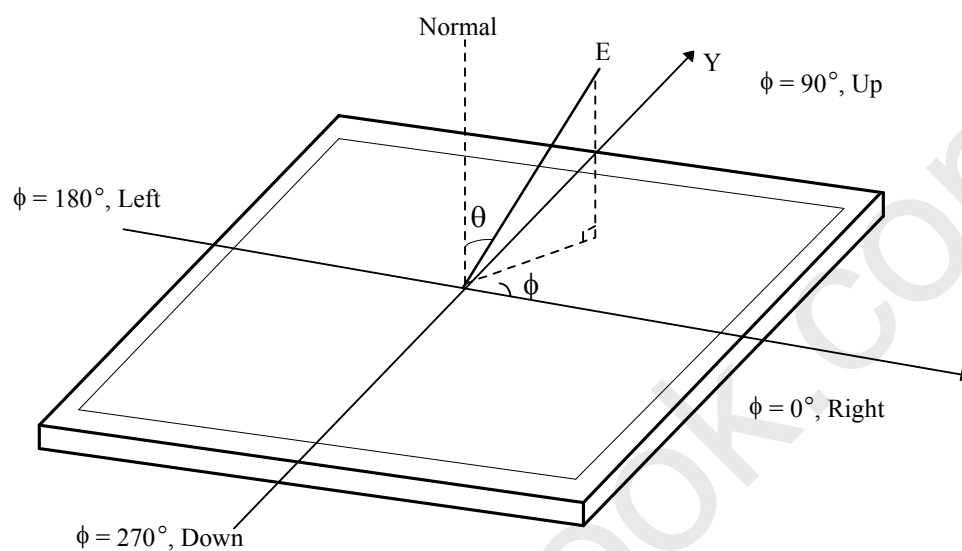


FIG. 11 Viewing Angle

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5. Mechanical Characteristics

Table 10 provides general mechanical characteristics.

Table 10. MECHANICAL CHARACTERISTICS

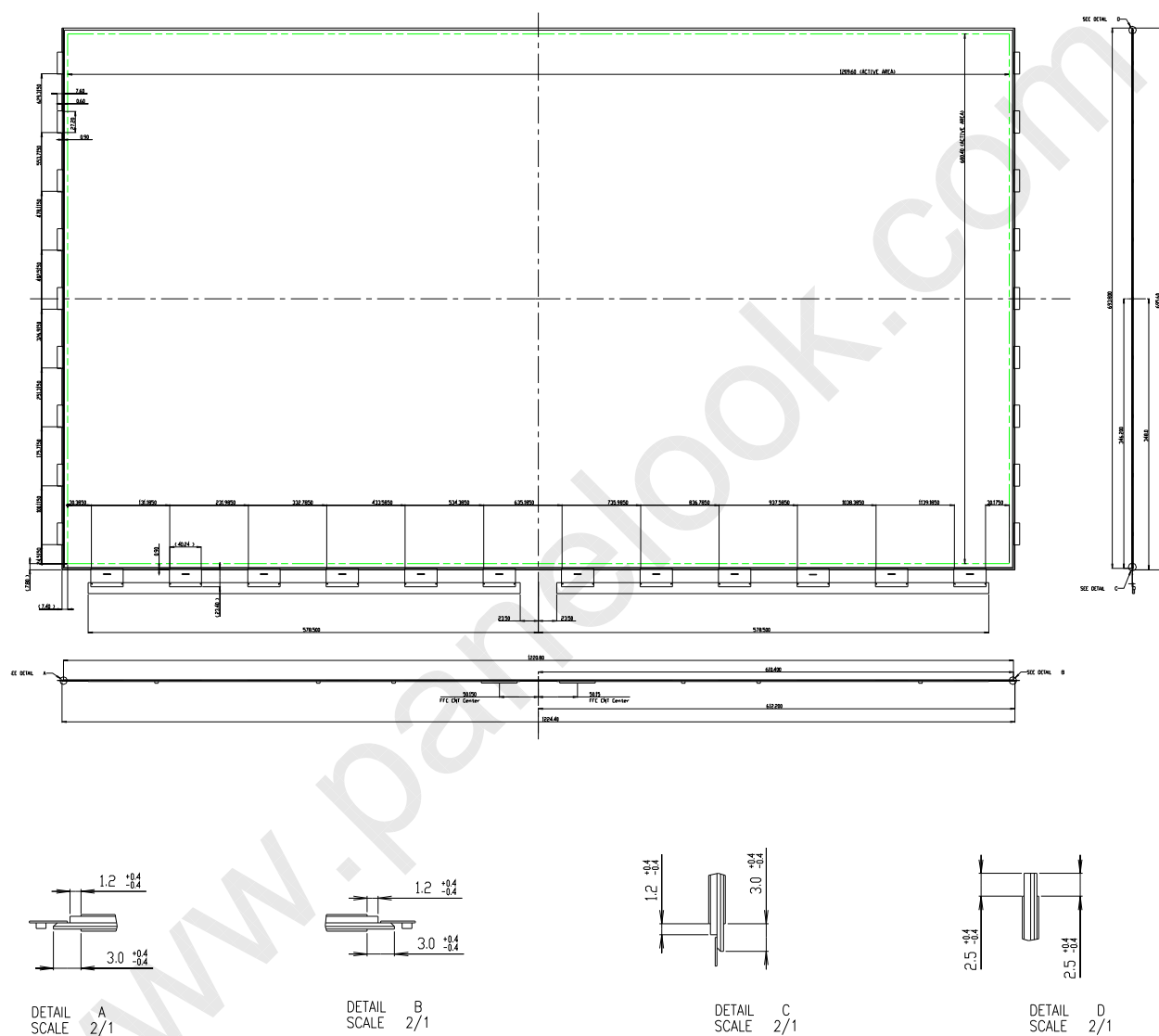
Item	Value	
Outline Dimension (Only Glass)	Horizontal	1220.8 mm
	Vertical	693.8 mm
	Thickness	1.94 mm
Bezel Area	Horizontal	1220.8 mm
	Vertical	693.8 mm
Active Display Area	Horizontal	1209.6 mm
	Vertical	680.4 mm
Weight	3.4Kg (Typ.)	

Note : Please refer to a mechanic drawing in terms of tolerance at the next page.

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<FRONT VIEW>



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6. Reliability

Table 11. ENVIRONMENT TEST CONDITION

No.	Test Item	Condition
1	High temperature storage test	Ta= 60°C 240h
2	Low temperature storage test	Ta= -20°C 240h
3	High temperature operation test	Ta= 50°C 50%RH 240h
4	Low temperature operation test	Ta= 0°C 240h
5	Humidity condition Operation	Ta= 40 °C ,90%RH
6	Altitude operating storage / shipment	0 - 15,000 ft 0 - 40,000 ft



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7. International Standards

7-1. Environment

- a) RoHS, Directive 2002/95/EC of the European Parliament and of the council of 27 January 2003



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8. Packing

8-1. Packing Form

- a) Package quantity in one Pallet : 70 pcs
- b) Pallet Size :1400 mm(L) X 900 mm(W) X 1105 mm(H)

Product Specification

9. Precautions

Please pay attention to the followings when you use this TFT LCD panel.

9-1. Assembly Precautions

- (1) Please attach the surface transparent protective plate to the surface in order to protect the polarizer.
Transparent protective plate should have sufficient strength in order to resist external force.
- (2) You should adopt radiation structure to satisfy the temperature specification.
- (3) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
- (4) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth. (Some cosmetics are detrimental to the polarizer.)
- (5) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer
- (6) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
- (7) Board ass'y should be put on the mold frame properly.
- (8) FFC Cable should be connected between System board and Source PCB correctly.
- (9) Mechanical structure for backlight system should be designed for sustaining board ass'y safely.

9-2. Operating Precautions

- (1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
 $V = \pm 200\text{mV}$ (Over and under shoot voltage)
- (2) Response time depends on the temperature. (In lower temperature, it becomes longer.)
- (3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time (required time that brightness is stable after turned on) becomes longer
- (4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
- (5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
- (6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.
- (7) Please do not give any mechanical and/or electrical impact to board ass'y. Otherwise, it can't be operated its full characteristics perfectly.



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9-3. Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly. Panel ground path should be connected to metal ground.

9-4. Precautions for Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

9-5. Storage

When storing the board ass'y as spares for a long time, the following precautions are necessary.

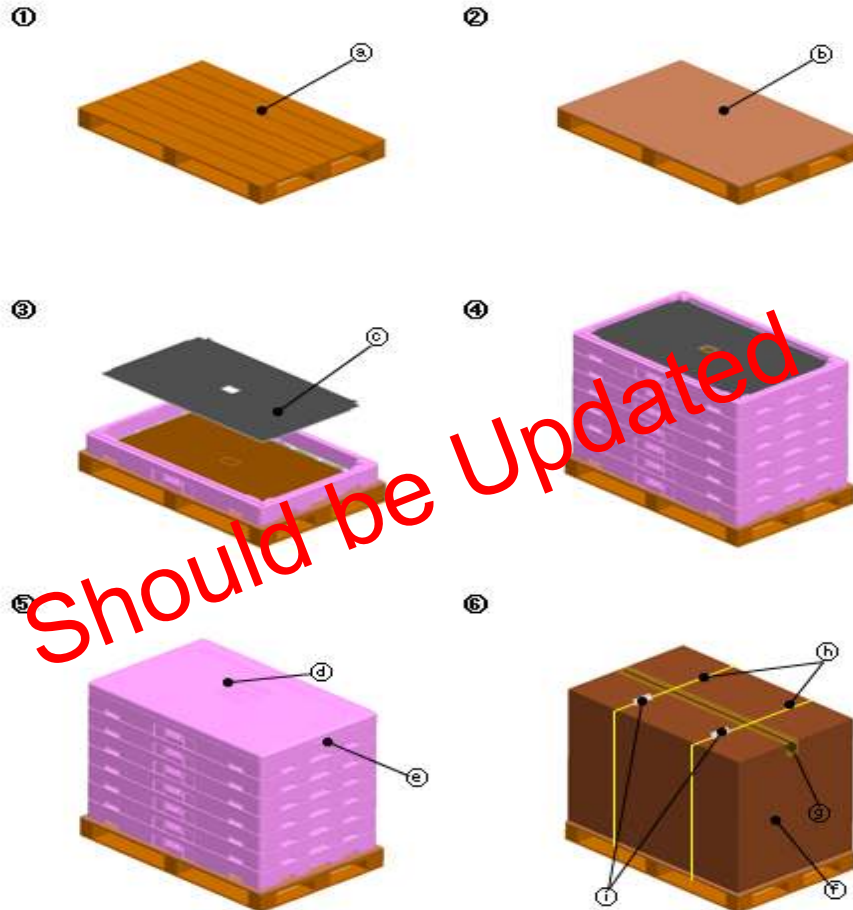
- (1) Store them in a dark place. Do not expose the board ass'y to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
- (2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

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APPENDIX- I

■ Pallet Ass'y



No.	Description	Material
(a)	Pallet	Plywood
(b)	Carton Plate	Single Wall
(c)	PE Sheet	Carbon
(d)	Top Packing	EPP
(e)	Bottom Packing	EPP
(f)	Angle Packing	Single Wall
(g)	Tape	OPP
(h)	Band	PP
(i)	Clip	Steel

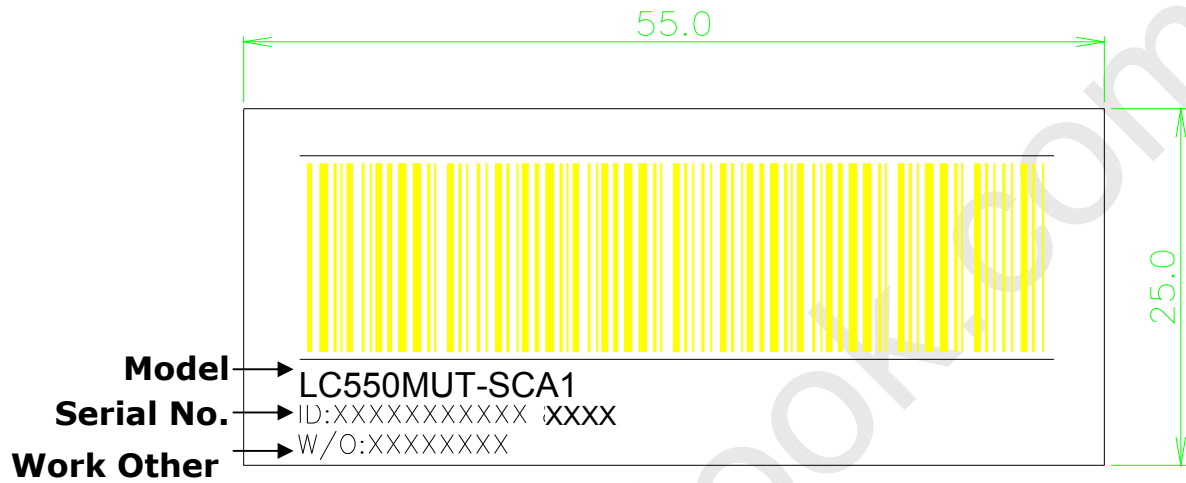


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APPENDIX- II

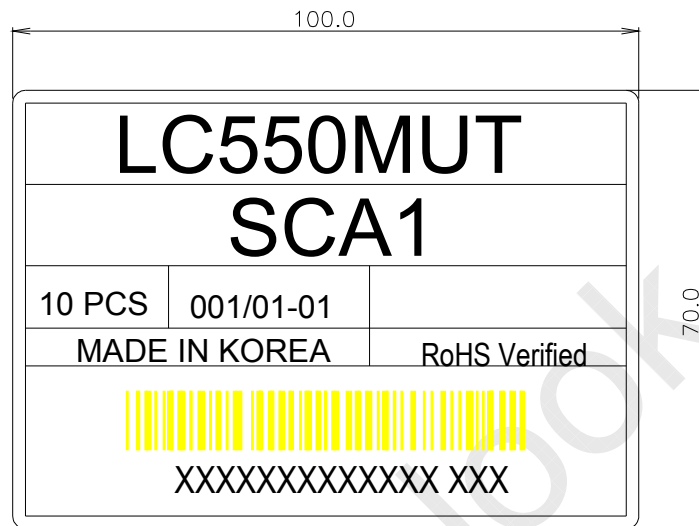
■ Serial Label



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APPENDIX- III

■ Pallet Label

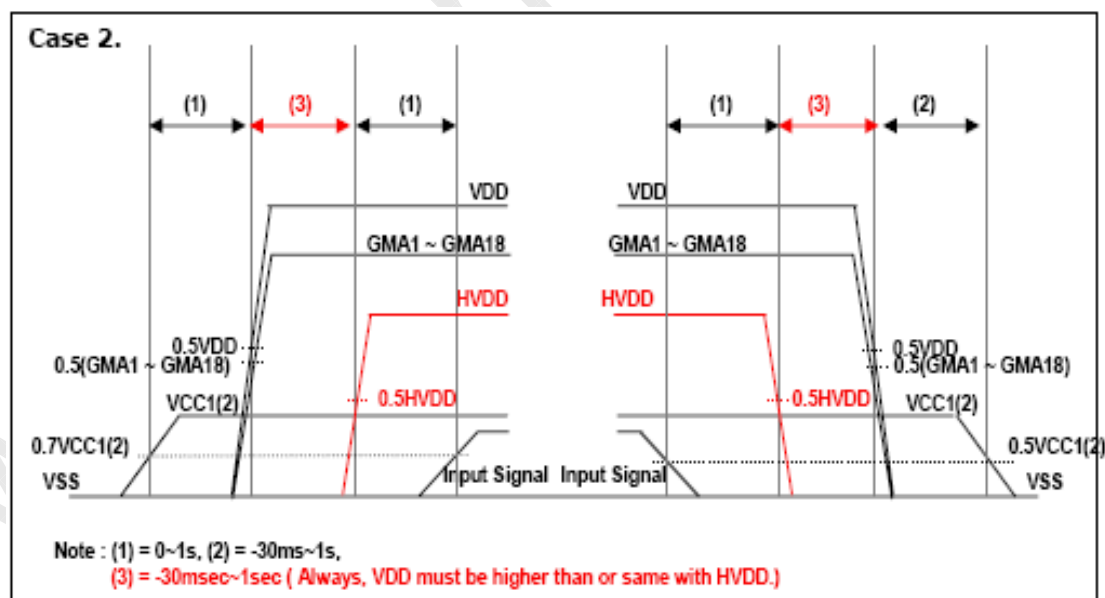
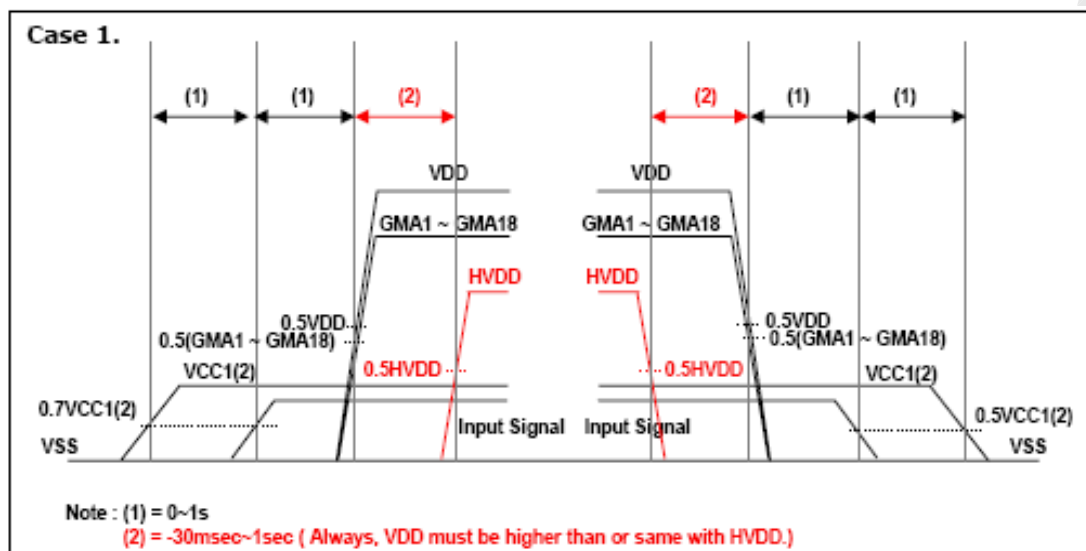


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APPENDIX- IV

■ LC550MUT-SCA1-Source D-IC Power Sequence



- Input Signal : SOE,POL,GSP,H_CONV,OPT_N