



SANYO Semiconductors

DATA SHEET

LC587508A

LC587506A

LC587504A

ROM (8K/6K/4K × 16 bits), RAM (512 × 4 bits), LCD driver
4-bit 1-chip Microcomputers

Overview

The LC587508A/06A/04A are CMOS 4-bit microcontrollers that, centering around a low-voltage-operable CPU, incorporate on a single-chip a number of features including 8K/6K/4K × 16 bits of ROM, 512 × 4 bits of RAM, stack-dedicated RAM (8 levels), 8-bit AD (4CH), 8-bit timer (2 channels) (1 channel can be used as an event counter), 8-bit synchronous serial interface, alarm signal generator circuit, remote control carrier generator circuit, LCD controller and driver, and powerful standby function (power saving feature). They are upward-compatible versions of the LC587408A, extended with reinforced I/O port and segment driver capabilities.

Functions

- Mobile devices with LCD display capabilities (optimum for mobile device applications that require battery-driven low power operation).
- Control and LCD display of and for portable CDs, timers, and health monitoring instruments.
- Remote control for CDs, VCRs, tuners, etc.

Features

■ROM

- LC587508A (8192 × 16 bits)
- LC587506A (6144 × 16 bits)
- LC587504A (4096 × 16 bits)

■RAM

- LC587508A (512 × 4 bits)
- LC587506A (512 × 4 bits)
- LC587504A (512 × 4 bits)

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SANYO Electric Co.,Ltd. Semiconductor Company

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

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■ Instruction Cycle Time

(all instructions except table lookup instructions execute in one cycle)

- LCD voltage step-up option (1.5V power supply/Ag battery, etc.)

Cycle Time	Supply Voltage	System Clock Oscillation Source	Oscillation Frequency
20μs	1.35 to 1.75V	RC oscillator	200kHz
122μs	1.35 to 1.75V	Xtal (crystal) oscillator	32.768kHz

- LCD voltage step-down option (3.0V power supply/Li battery, etc.)

Cycle Time	Supply Voltage	System Clock Oscillation Source	Oscillation Frequency
1μs	4.5 to 5.5V	CF (ceramic) oscillator	4MHz
4μs	2.5 to 5.5V	CF (ceramic) oscillator	1MHz
10μs	2.5 to 5.5V	CF (ceramic) oscillator	400kHz
122μs	2.0 to 5.5V	Xtal (crystal) oscillator	32.768kHz

* It must be noted when using an LCD, that the lower limit of the system operating voltage becomes higher in accordance with the LCD's bias specifications.

■ Ports

Input-only pins

- Port S (4 pins)
- INT pin (1 pin)

Input/output pins

- Port K (4 pins)

The output type is fixed to "CMOS".

- Port M (4 pins)

The output type can be programmed to "CMOS" or "Pch" on a port basis.

(The M4 pin is configured as a signal input pin when timer 2 is set in the event counter mode).

- Port SO (4 pins)

The output type can be programmed to "CMOS" or "Nch" on a port basis. The three pins SO1, SO2, and SO3 are also used for the serial interface (2-pin serial communication is also possible).

- Port P (4 pins)

The output type can be programmed to "CMOS" or "Pch" on a port basis.

- Port A (4 pins)

The output type can be programmed to "CMOS" or "Pch" on a port basis.

Output-only pins

- Port N (4 pins)

The N3 pin is also used as the remote controller carrier output pin. The N4 pin is also used as the alarm output pin.

LCD driver pins

- Common pin (4 pins)
- Segment pin (35 pins)

Each segment pin incorporates dedicated memory (segment memory) for holding output data. Its output type can be changed under program control from "LCD driver output" to a general-purpose output type (CMOS, Pch, or Nch).

■ Variety of LCD Drive Modes

LCD Drive Mode	No. of Drivable Segments	Required Common Pins
1/3 bias, 1/4 duty	140 segments	COM1 to COM4
1/3 bias, 1/3 duty	105 segments	COM1 to COM3
1/2 bias, 1/4 duty	140 segments	COM1 to COM4
1/2 bias, 1/3 duty	105 segments	COM1 to COM3
DUPLEX	70 segments	COM1 and COM2
STATIC	35 segments	COM1

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■ Timers

Timer 1

- 6-bit prescaler + 8-bit programmable reload timer
(The prescaler is shared by timer 1, timer 2, and serial interface).
- Supports programmable generation of the remote controller carrier signal.

Timer 2

- 6-bit prescaler + 8-bit programmable timer
(The prescaler is shared by timer 1, timer 2, and serial interface).
- Can serve as an event counter.

Base timer (available when the 32.768kHz Xtal oscillation source is selected)

- Allows two signals (125ms/500ms or 250ms/1000ms) to be selected out of four reference signals using a mask option and programming, so that the base timer is flexible with the application.

■ Standby Function

HALT mode

- The microcontroller halts execution of instructions in the HALT mode. The oscillation circuits, timers, the LCD controller and driver, and serial interface continue processing. A program that contains no unnecessary loop and makes effective use of this HALT mode could realize low-power operation.
- The conditions for resetting the HALT mode can be defined under program control. The following sources can reset the HALT mode:
 - (1) Change in the level of the signal at the INT pin (1 source)
 - (2) Timer 1 (1 source)
 - (3) Timer 2 (1 source)
 - (4) Base timer (1 source)
 - (5) Change in the level of the signal at the serial interface or SO4 pin (either one source)
 - (6) Change in the level of the signal at port S or K defined by the SSW instruction (8 sources)
 - (7) Reset signal

HOLD mode

- The complete standby mode in which all oscillation circuits are stopped.
- The conditions for resetting the HOLD mode can be defined under program control. The following sources can reset the HOLD mode:
 - (1) Change in the level of the signal at the INT pin (1 source)
 - (2) Timer 2 event counter mode (1 source)
 - (3) Change in the level of the signal at the serial interface or SO4 pin (either one source)
 - (4) Change in the level of the signal at port S or K defined by the SSW instruction (8 sources)
 - (5) Reset signal

■ Interrupt Function (5-source 4-vector addresses)

- (1) Change in the level of the signal at the INT pin (1 source)
- (2) Timer 1 (1 source)
- (3) Timer 2 (1 source)
- (4) Change in the level of the signal at the serial interface or SO4 pin (either one source)

■ Watchdog Timer

The watchdog timer is of a 16-bit counter type. It can be reset by a combination of two passing points so that it is flexible with the application.

Sample watchdog timer operating times

- | | |
|--|-----------------|
| When Xtal oscillation is selected (32.768kHz, 1- or 2-oscillator mode) : | 2000ms (max.) |
| When CF oscillation is selected (1MHz, 1 oscillation) : | 65.536ms (max.) |

■ Subroutine Stack

The LC587508A/06A/04A series microcontrollers incorporate 8 levels of stack-dedicated RAM that is shared by the interrupt handler and subroutines. Consequently, no data memory is consumed to save the contents of the program counter.

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■Number of Instructions

The LC587508A/06A/04A series microcontrollers are provided with 130 easy-to-use instructions including accumulator manipulation, register-to-memory transfer, arithmetic and logical operations, flag manipulation, I/O port manipulation, and a variety of conditional branch instructions.

■Oscillation Circuits (3 Circuits)

1-oscillation mode ----- One of CF, RC, and Xtal oscillators

2-oscillation mode ----- CF + Xtal oscillators or RC oscillator + Xtal oscillators

CF (ceramic) oscillation circuit

- Fast mode system clock
- 400kHz to 4MHz

RC (resistor & capacitor) oscillation circuit

- Fast mode system clock
- 200kHz to 800kHz (depends on the power requirements)
- 2-pin oscillation

Xtal (crystal) oscillation circuit

- Slow mode system clock
- 32.768kHz, 65.536kHz

■Packaging

- QIP80E (flat package) <Under development>
- Chip

1.5V Supply Voltage Version

Absolute Maximum Ratings at $V_{SS} = 0V$, $T_a = 25^{\circ}C \pm 2^{\circ}C$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Maximum supply voltage	V_{DD}		-0.3		+6.5	V
	V_{DD1}		-0.3		+6.5	V
	V_{DD2}		-0.3		+6.5	V
Maximum input voltage	V_{I-1}	Permitted by designated circuit, XTIN and CFIN	Up to the voltage to be generated			
	V_{I-1}	S1-S4, K1-K4, P1-P4, SO1-SO4, RES, INT, TST (Ports K, P, M, and SO are in input mode.)	-0.3		$V_{DD}+0.3$	V
Maximum output voltage	V_{O-1}	Permitted by designated circuit, XTOUT, CFOUT	Up to the voltage to be generated			
	V_{O-1}	K1-K4, P1-P4, SO1-SO4, N1-N4, CUP1, CUP2, SEG1-SEG35, COM1-COM4 (Ports K, P, M, and SO are in output mode.)	-0.3		$V_{DD}+0.3$	V
	V_{O-3}	Open drain version N1-N4 (Nch)	-0.3		+12	V
Output pin current	I_{O-1}	Per 1 pin, N1-N4	0		+10	mA
	I_{O-2}		-10		0	mA
	I_{O-3}	Per 1 pin, K1-K4, P1-P4, M1-M4, SO1-SO4	0		+1	mA
	I_{O-4}		-1		0	mA
	ΣI_{O-1} ΣI_{O-2}	Total pin current (K1-4, P1-4, M1-4, SO1-SO4, N1-N4, SEG1-SEG35)	-20		20	mA mA
Power dissipation	P_D max	QIP80E flat package			300	mW
Operating ambient temperature	T_{opr}		-30		+70	$^{\circ}C$
Storage ambient temperature	T_{stg}		-55		+125	$^{\circ}C$

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Allowable Operating Range at $V_{SS} = 0V$, $T_a = -30^{\circ}C$ to $+70^{\circ}C$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	No LCD version: $V_{DD2} = V_{DD} \times 2$, $V_{DD1} = V_{DD}$	1.35		1.75	V
		1/1 bias version: $V_{DD2} = V_{DD} \times 2$, $V_{DD1} = V_{DD}$	1.35		1.75	V
		1/2 bias version: $V_{DD2} = V_{DD} \times 2$, $V_{DD1} = V_{DD}$	1.35		1.75	V
		1/3 bias version: $V_{DD2} = V_{DD} \times 3$, $V_{DD1} = V_{DD} \times 2$	1.35		1.75	V
High-level input voltage	V_{IH1}	S1-S4, K1-K4, P1-P4, M1-M4, SO1-SO4, A1-A4, INT	$0.7V_{DD}$		V_{DD}	V
	V_{IH2}	RES pin	$0.75V_{DD}$		V_{DD}	V
	V_{IH3}	CFIN pin	$0.75V_{DD}$		V_{DD}	V
Low-level input voltage	V_{IL1}	S1-S4, K1-K4, P1-P4, M1-M4, SO1-SO4, A1-A4, INT	0		$0.3V_{DD}$	V
	V_{IL2}	RES pin	0		$0.25V_{DD}$	V
	V_{IL3}	CFIN pin	0		$0.25V_{DD}$	V
Operating frequency	fopr1	$V_{DD} = 1.35V$ to $1.75V$ 32kHz XTIN/XTOUT crystal oscillator	32		33	kHz
	fopr2	$V_{DD} = 1.35V$ to $1.75V$ 65kHz XTIN/XTOUT crystal oscillator	60		70	kHz
	fopr3	$V_{DD} = 1.35V$ to $1.75V$ RC version		200		kHz
	fopr4	$V_{DD} = 1.35V$ to $1.75V$ SO1/SO3 pins(serial mode) Rising and falling edges of input signal/clock waveform $\leq 10\mu s$	DC		200	kHz

*** Note:**

The recommended operating range and electrical characteristics listed above are measured for the test LSI devices that are incorporated in the QIP80E package.

The specifications for the chip version of this LSI are basically identical to those for the QIP80E package version of this LSI except that the some characteristics of the chip version of the LSI differ depending on the board on which the chip is mounted, the bonding pressure, and the molding resin used. Consequently, the recommended operating range and electrical characteristics for the chip version of this LSI are defined at an operating ambient temperature (T_a) of $25^{\circ}C \pm 2^{\circ}C$.

Electrical Characteristics at $V_{DD} = 1.55V$, $V_{SS} = 0V$, $T_a = -30$ to $+70^{\circ}C$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input resistance	R_{IN1A}	$V_{IN} = 0.2V_{DD}$ Low-level hold T_r *1	200	300	400	k Ω
	R_{IN1B}	$V_{IN} = V_{DD}$ Pull-down resistance *1	200	300	400	k Ω
	R_{IN1C}	$V_{IN} = 0.8V_{DD}$ High-level hold T_r *1	200	300	400	k Ω
	R_{IN1D}	$V_{IN} = V_{SS}$ Pull-up resistance *1	200	300	400	k Ω
	R_{IN2A}	$V_{IN} = 0.2V_{DD}$ INT low-level hold T_r	200	300	400	k Ω
	R_{IN2B}	$V_{IN} = V_{DD}$ INT pull-down resistance	60		220	k Ω
	R_{IN2C}	$V_{IN} = 0.8V_{DD}$ INT high-level hold T_r	200	300	400	k Ω
	R_{IN2D}	$V_{IN} = V_{SS}$ INT pull-up resistance	60		220	k Ω
	R_{IN3}	$V_{IN} = V_{DD}$ RES pull-down resistance	20		300	k Ω
	R_{IN4}	$V_{IN} = V_{SS}$ RES pull-up resistance	20		300	k Ω
	R_{IN5}	$V_{IN} = V_{DD}$ TST pin pull-down resistance	20		300	k Ω
High-level output voltage	V_{OH-1}	$V_{DD} = 1.35V/I_{OH} = -500\mu A$	$V_{DD}-0.65$			V
Low-level output voltage	V_{OL-1}	$V_{DD} = 1.35V/I_{OL} = 500\mu A$ * N1-N4			0.65	V
	V_{OH-2} V_{OL-2}	$V_{DD} = 1.35V/I_{OH} = -100\mu A$ $V_{DD} = 1.35V/I_{OL} = 100\mu A$ * K1-K4, P1-P4, M1-M4, SO1-SO4, A1-A4 (Ports K, P, M, SO, and A are in output mode.)	$V_{DD}-0.2$		0.2	V V
Off output leakage current	$ I_{OFF} $	$V_{OH} = 10.5V$ N1-N4 (open version)			1.0	μA
Segment port output impedance • CMOS output port type						
High-level output voltage	V_{OH-3}	$I_{OH} = -50\mu A$ Seg1 to 35	$V_{DD}-0.2$			V
Low-level output voltage	V_{OL-3}	$I_{OL} = 50\mu A$			0.2	V
Segment port output impedance • Pch-open drain output type						
Off output leakage current	$ I_{OFF} $	$V_{OL} = V_{SS}$			1.0	μA
Segment port output impedance • Nch-open drain output type						
Off output leakage current	$ I_{OFF} $	$V_{OH} = V_{DD}$			1.0	μA

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Segment port output impedance • Static type						
High-level output voltage	V_{OH-4}	$I_{OH} = -10\mu A$ Seg1 to Seg35	$V_{DD2-0.2}$			V
Low-level output voltage	V_{OL-4}	$I_{OL} = 10\mu A$			0.2	V
High-level output voltage	V_{OH-5}	$I_{OH} = -100\mu A$ COM1	$V_{DD2-0.2}$			V
Low-level output voltage	V_{OL-5}	$I_{OL} = 100\mu A$			0.2	V
Segment port output impedance • 1/2 bias type						
High-level output voltage	V_{OH-4}	$I_{OH} = -10\mu A$ Seg1 to Seg35	$V_{DD2-0.2}$			V
Low-level output voltage	V_{OL-4}	$I_{OL} = 10\mu A$			0.2	V
High-level output voltage	V_{OH-5}	$I_{OH} = -100\mu A$ COM1-COM4	$V_{DD2-0.2}$			V
M-level output voltage	V_{OM}	$I_{OH} = -100\mu A$	$V_{DD-0.2}$			V
Low-level output voltage		$I_{OL} = 100\mu A$			$V_{DD+0.2}$	V
	V_{OL-5}	$I_{OL} = 100\mu A$			0.2	V
Segment port output impedance • 1/3 bias type						
High-level output voltage	V_{OH-4}	$I_{OH} = -10\mu A$ Seg1 to Seg35	$V_{DD2-0.2}$			V
M-level output voltage	V_{OM1-1}	$I_{OH} = -10\mu A$	$V_{DD1-0.2}$			V
		$I_{OL} = 10\mu A$			$V_{DD1+0.2}$	V
	V_{OM1-2}	$I_{OH} = -10\mu A$	$V_{DD-0.2}$			V
		$I_{OL} = 10\mu A$			$V_{DD+0.2}$	V
Low-level output voltage	V_{OL-4}	$I_{OL} = 10\mu A$			0.2	V
High-level output voltage	V_{OH-6}	$I_{OH} = -100\mu A$ COM1-COM4	$V_{DD2-0.2}$			V
M-level output voltage	V_{OM2-1}	$I_{OH} = -100\mu A$	$V_{DD1-0.2}$			V
		$I_{OL} = 100\mu A$			$V_{DD1+0.2}$	V
	V_{OM2-2}	$I_{OH} = -100\mu A$	$V_{DD-0.2}$			V
		$I_{OL} = 100\mu A$			$V_{DD+0.2}$	V
Low-level output voltage	V_{OL-6}	$I_{OL} = 100\mu A$			0.2	V

Electrical Characteristics at $V_{DD} = 1.55V$, $V_{SS} = 0V$, $T_a = -30$ to $+70^\circ C$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Power supply leakage current	ILEK-1	$V_{DD} = 3.0V$ $T_a = 25^\circ C$	-1.0		1.0	μA
Input leakage current	IOFF	$V_{DD} = 3.0V$ $T_a = 25^\circ C$ $V_{IN} = V_{DD}/2$ S1-S4, K1-K4, P1-P4, M1-M4, SO1-SO4, A1-A4 (input mode)	-1.0		1.0	μA
Output voltage 1	V_{DD1-1} V_{DD2-1}	$V_{DD} = 1.5V$, 1/1 bias, $f_{opr} = 32.768kHz$ V_{DD1} : OPEN/ $V_{DD2-V_{SS}}$: $0.1\mu F$ CUP1-CUP2: $0.1\mu F$	1.35 2.85	1.5 3.0	1.65 3.15	V V
Output voltage 2	V_{DD1-2} V_{DD2-2}	$V_{DD} = 1.5V$, 1/2 bias, $f_{opr} = 32.768kHz$ V_{DD1} : OPEN/ $V_{DD2-V_{SS}}$: $0.1\mu F$ CUP1-CUP2: $0.1\mu F$	1.35 2.85	1.5 3.0	1.65 3.15	V V
Output voltage 3	V_{DD1-3} V_{DD2-3}	$V_{DD} = 1.5V$, 1/3 bias, $f_{opr} = 32.768kHz$ $V_{DD1-V_{SS}}$: $0.1\mu F$ / $V_{DD2-V_{SS}}$: $0.1\mu F$ CUP1-CUP2: $0.1\mu F$	2.85 4.35	3.0 4.5	3.15 4.65	V V
Supply current 1	$ I_{DD} _{1-1}$	$V_{DD} = 1.55V$ $T_a = 25^\circ C$ Xtal 32kHz version (Cd and Rd built in) $C_g = 30pF$, $C_l = 31K\Omega$ in HALT mode, LCD = 1/3 bias, 32Hz		1.5	4.0	μA

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3.0V Supply Voltage Version

Absolute Maximum Ratings at $V_{SS} = 0V$, $T_a = 25^\circ C \pm 2^\circ C$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Maximum supply voltage	V_{DD}		-0.3		+6.5	V
	V_{DD1}		-0.3		V_{DD}	V
	V_{DD2}		-0.3		V_{DD}	V
Maximum input voltage	V_{I-1}	Permitted by designated circuit, XTIN and CFIN	Up to the voltage to be generated			
	V_{I-2}	S1-4, K1-4, P1-P4, SO1-SO4, RES, INT, TST (Ports K, P, M, and SO are in input mode.)	-0.3		$V_{DD}+0.3$	V
Maximum output voltage	V_{O-1}	Permitted by designated circuit, XTOUT and CFOUT	Up to the voltage to be generated			
	V_{O-2}	K1-4, P1-P4, SO1-SO4, N1-N4, CUP1, CUP2, SEG1-SEG35, COM1-COM4 (Ports K, P, M, and SO are in output mode.)	-0.3		$V_{DD}+0.3$	V
	V_{O-3}	Open-drain version N1-N4 (Nch)	-0.3		+12	V
Output pin current	I_{O-1}	Per pin, N1-4	0		+10	mA
	I_{O-2}		-10		0	mA
	I_{O-3}	Per pin, K1-K4, P1-P4, M1-M4, SO1-SO4	0		+1	mA
	I_{O-4}		-1		0	mA
	ΣI_{O-1}	Total pin current (K1-K4, P1-P4, M1-M4, SO1-SO4, N1-N4, SEG1- SEG35)			20	mA
ΣI_{O-2}	-20				mA	
Power dissipation	P_D max	QIP80E flat package			300	mW
Operating ambient temp.	T_{opr}		-30		+70	$^\circ C$
Storage ambient temp.	T_{stg}		-55		+125	$^\circ C$

Allowable Operating Range at $V_{SS} = 0V$, $T_a = -30^\circ C$ to $+70^\circ C$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	No LCD version: $V_{DD2} = V_{DD1} = V_{DD}$	2.00		5.50	V
		1/1 bias version: $V_{DD2} = V_{DD1} = V_{DD}$	2.00		5.50	V
		1/2 bias version: $V_{DD2} = V_{DD1} = V_{DD}/2$	3.00		5.50	V
		1/3 bias version: $V_{DD2} = V_{DD}/3$ $V_{DD1} = 2 \times V_{DD}/3$	3.00		5.50	V
High-level input voltage	V_{IH1}	S1-S4, K1-K4, P1-P4, M1-M4, SO1-SO4, A1-A4, INT	$0.7V_{DD}$		V_{DD}	V
	V_{IH2}	RES pin	$0.75V_{DD}$		V_{DD}	V
	V_{IH3}	CFIN pin	$0.75V_{DD}$		V_{DD}	V
Low-level input voltage	V_{IL1}	S1-S4, K1-K4, P1-P4, M1-M4, SO1-SO4, A1-A4, INT	0		$0.3V_{DD}$	V
	V_{IL2}	RES pin	0		$0.25V_{DD}$	V
	V_{IL3}	CFIN pin	0		$0.25V_{DD}$	V
Operating freq.	fopr1	$V_{DD} = 2.0V$ to $5.5V$ 32kHz XTIN/XTOUT crystal oscillator	32		33	kHz
	fopr2	$V_{DD} = 2.2V$ to $5.5V$ 65kHz XTIN/XTOUT crystal oscillator	60		70	kHz
	fopr3	$V_{DD} = 2.2V$ to $5.5V$ CFIN/CFOUT CF version	390		810	kHz
	fopr4	$V_{DD} = 2.8V$ to $5.5V$ CFIN/CFOUT CF version	390		4200	kHz
	fopr5	$V_{DD} = 3.0V$ to $5.5V$ SO1/SO3 pin (serial mode) Rising and falling edges of input signal/clock waveform $\leq 10\mu s$	DC		200	kHz

*** Note:**

The recommended operating range and electrical characteristics listed above are measured for the test LSI devices that are incorporated in the QIP80E package.

The specifications for the chip version of this LSI are basically identical to those for the QIP80E package version of this LSI except that the some characteristics of the chip version of the LSI differ depending on the board on which the chip is mounted, the bonding pressure, and the molding resin used. Consequently, the recommended operating range and electrical characteristics for the chip version of this LSI are defined at an operating ambient temperature (T_a) of $25^\circ C \pm 2^\circ C$.

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Electrical Characteristics at $V_{DD} = 4.5V$, $V_{SS} = 0V$, $T_a = -30$ to $+70^\circ C$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input resistance	R_{IN1A}	$V_{IN} = 0.2V_{DD}$ Low-level hold T_r *1	200	400	500	k Ω
	R_{IN1B}	$V_{IN} = V_{DD}$ Pull-down resistance *1	200	300	400	k Ω
	R_{IN1C}	$V_{IN} = 0.8V_{DD}$ High-level hold T_r *1	200	400	500	k Ω
	R_{IN1D}	$V_{IN} = V_{SS}$ Pull-up resistance *1	200	300	400	k Ω
	R_{IN2A}	$V_{IN} = 0.2V_{DD}$ INT low-level hold T_r	200	400	500	k Ω
	R_{IN2B}	$V_{IN} = V_{DD}$ INT pull-down resistance	60		220	k Ω
	R_{IN2C}	$V_{IN} = 0.8V_{DD}$ INT high-level hold T_r	200	400	500	k Ω
	R_{IN2D}	$V_{IN} = V_{SS}$ INT pull-up resistance	60		220	k Ω
	R_{IN3}	$V_{IN} = V_{DD}$ RES pull-down resistance	20		300	k Ω
	R_{IN4}	$V_{IN} = V_{SS}$ RES pull-up resistance	20		300	k Ω
R_{IN5}	$V_{IN} = V_{DD}$ TST pin pull-down resistance	20		300	k Ω	
High-level output voltage	V_{OH-1}	$V_{DD} = 3.0V/I_{OH} = -5mA$	$V_{DD}-0.5$			V
Low-level output voltage	V_{OL-1}	$V_{DD} = 3.0V/I_{OL} = 5mA$ * N1-N4			0.5	V
	V_{OH-2}	$V_{DD} = 3.0V/I_{OH} = -1mA$	$V_{DD}-0.5$			V
	V_{OL-2}	$V_{DD} = 3.0V/I_{OL} = 1mA$ * K1-K4, P1-P4, M1-M4, SO1-SO4, A1-A4 (Ports K, P, M, SO, and A are in output mode.)			0.5	V
Off output leakage current	$ I_{OFF} $	$V_{OH} = 10.5V$ N1-N4 (open version)			1.0	μA
Segment port output impedance • CMOS output type						
High-level output voltage	V_{OH-3}	$I_{OH} = -50\mu A$ Seg1 to Seg35	$V_{DD}-0.2$			V
Low-level output voltage	V_{OL-3}	$I_{OL} = 50\mu A$			0.2	V
Segment port output impedance • Pch-open drain output type						
Off output leakage current	$ I_{OFF} $	$V_{OL} = V_{SS}$			1.0	μA
Segment port output impedance • Nch-open drain output type						
Off output leakage current	$ I_{OFF} $	$V_{OH} = V_{DD}$			1.0	μA
Segment port output impedance • Static type						
High-level output voltage	V_{OH-4}	$I_{OH} = -10\mu A$ Seg1 to Seg35	$V_{DD}-0.2$			V
Low-level output voltage	V_{OL-4}	$I_{OL} = 10\mu A$			0.2	V
High-level output voltage	V_{OH-5}	$I_{OH} = -100\mu A$ COM1	$V_{DD}-0.2$			V
Low-level output voltage	V_{OL-5}	$I_{OL} = 100\mu A$			0.2	V
Segment port output impedance • 1/2 bias type						
High-level output voltage	V_{OH-4}	$I_{OH} = -10\mu A$ Seg1 to Seg35	$V_{DD}-0.2$			V
Low-level output voltage	V_{OL-4}	$I_{OL} = 10\mu A$			0.2	V
High-level output voltage	V_{OH-5}	$I_{OH} = -100\mu A$ COM1-COM4	$V_{DD}-0.2$			V
M-level output voltage	V_{OM}	$I_{OH} = -100\mu A$	$V_{DD}1-0.2$			V
Low-level output voltage		$I_{OL} = 100\mu A$			$V_{DD}1+0.2$	V
	V_{OL-5}	$I_{OL} = 100\mu A$			0.2	V
Segment port output impedance • 1/3 bias type						
High-level output voltage	V_{OH-4}	$I_{OH} = -10\mu A$ Seg1 to Seg35	$V_{DD}-0.2$			V
M-level output voltage	V_{OM1-1}	$I_{OH} = -10\mu A$	$V_{DD}1-0.2$			V
		$I_{OL} = 10\mu A$			$V_{DD}1+0.2$	V
	V_{OM1-2}	$I_{OH} = -10\mu A$	$V_{DD}2-0.2$			V
		$I_{OL} = 10\mu A$			$V_{DD}2+0.2$	V
Low-level output voltage	V_{OL-4}	$I_{OL} = 10\mu A$			0.2	V
High-level output voltage	V_{OH-6}	$I_{OH} = -100\mu A$ COM1-COM4	$V_{DD}-0.2$			V
M-level output voltage	V_{OM2-1}	$I_{OH} = -100\mu A$	$V_{DD}1-0.2$			V
		$I_{OL} = 100\mu A$			$V_{DD}1+0.2$	V
	V_{OM2-2}	$I_{OH} = -100\mu A$	$V_{DD}2-0.2$			V
		$I_{OL} = 100\mu A$			$V_{DD}2+0.2$	V
Low-level output voltage	V_{OL-6}	$I_{OL} = 100\mu A$			0.2	V

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Electrical Characteristics at $V_{DD} = 4.5V$, $V_{SS} = 0V$, $T_a = -30$ to $+70^\circ C$

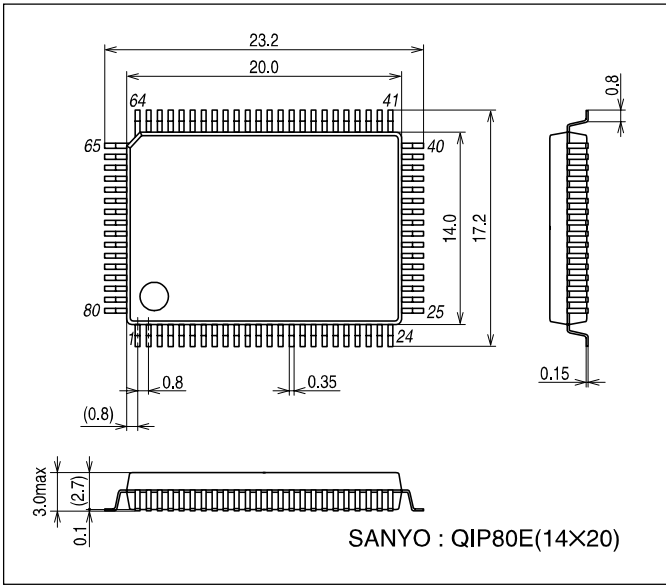
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Power leakage current	ILEK-1	$V_{DD} = 3.0V$ $T_a = 25^\circ C$	-1.0		1.0	μA
Input leakage current	IOFF	$V_{DD} = 6.0V$ $T_a = 25^\circ C$ $V_{IN} = V_{DD}/2$ S1-S4, K1-K4, P1-P4, M1-M4, SO1-SO4, A1-A4 (input mode)	-1.0		1.0	μA
Output voltage 1	V_{DD1-1} V_{DD2-1}	$V_{DD} = 3.0V$, 1/1 bias, $f_{opr} = 32.768kHz$ V_{DD1} : OPEN/ V_{DD2} : OPEN CUP1-CUP2: OPEN	2.8		V_{DD}	V
			2.8		V_{DD}	V
Output voltage 2	V_{DD1-2} V_{DD2-2}	$V_{DD} = 3.0V$, 1/2 bias, $f_{opr} = 32.768kHz$ V_{DD1} : OPEN/ V_{DD2} - V_{SS} : $0.1\mu F$ CUP1-CUP2: $0.1\mu F$	1.4	1.5	1.6	V
			1.4	1.5	1.6	V
Output voltage 3	V_{DD1-3} V_{DD2-3}	$V_{DD} = 3.0V$, 1/3 bias, $f_{opr} = 32.768kHz$ V_{DD1} - V_{SS} : $0.1\mu F$ / V_{DD2} - V_{SS} : $0.1\mu F$ CUP1-CUP2: $0.1\mu F$	1.9	2.0	2.1	V
			0.9	1.0	1.1	V
Supply current 1	$ I_{DD} 2-1$	$V_{DD} = 3.0V$ $T_a = 25^\circ C$ Xtal 32kHz version (Cd and Rd built in) $V_{DD} = 5.0V$ $T_a = 25^\circ C$ Xtal 32kHz version (Cd and Rd built in) $C_g = 30pF$, $C_I = 31k\Omega$ HALT mode, LCD = 1/3 bias, 32Hz		5.0	10.0	μA
				25.0	40.0	μA
Supply current 2	$ I_{DD} 2-2$	$V_{DD} = 3.0V$ $T_a = 25^\circ C$ CF 400kHz version $V_{DD} = 5.0V$ $T_a = 25^\circ C$ CF 400kHz version $C_{cg} = C_{cd} = 330pF$, HALT mode, LCD = 1/3 bias, 32Hz		150	200	μA
					550	μA
Supply current 3	$ I_{DD} 2-3$	$V_{DD} = 3.0V$ $T_a = 25^\circ C$ CF 4MHz version $V_{DD} = 5.0V$ $T_a = 25^\circ C$ CF 4MHz version $C_{cg} = C_{cd} = 33pF$, HALT mode, LCD = 1/3 bias, 32Hz		220	300	μA
					750	μA

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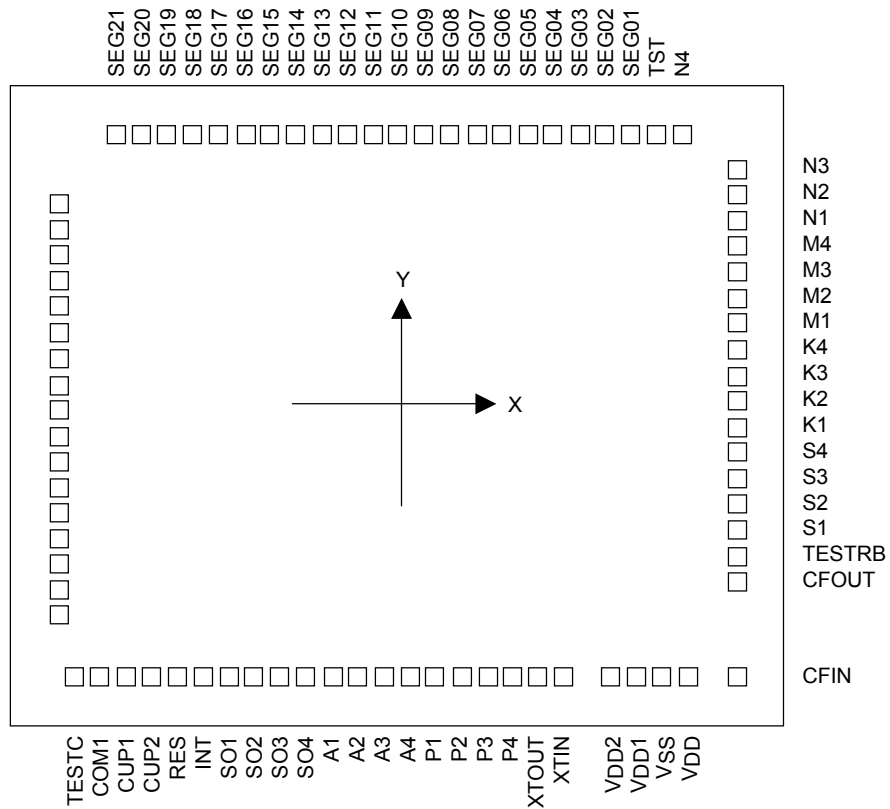
Package Dimensions

unit : mm

3174A



PAD Reference Diagram



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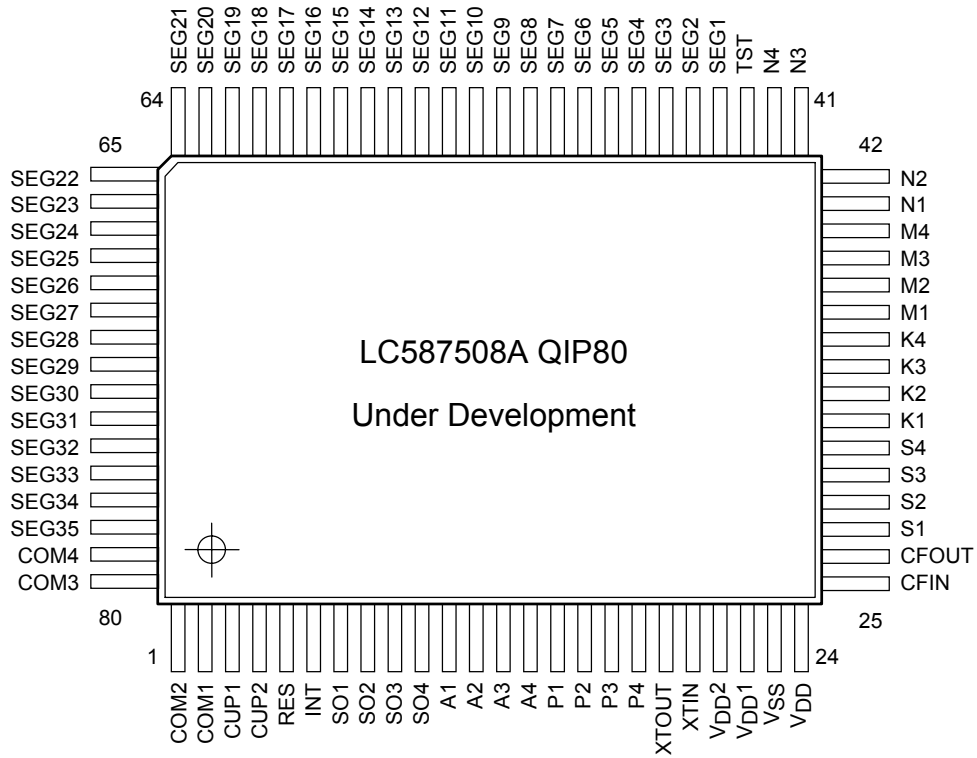
PAD Coordinate Values

NO	Pin Name	X Cord.	Y Cord.	NO	Pin Name	X Cord.	Y Cord.	NO	Pin Name	X Cord.	Y Cord.
1	V _{DD}	1405	-1318	31	SEG10	5	1318	61	COM1	-1445	-1318
2	CFIN	1643	-1315	32	SEG11	-120	1318	62	CUP1	-1320	-1318
3	CFOUT	1643	-850	33	SEG12	-245	1318	63	CUP2	-1195	-1318
4	TESTRB	1643	-725	34	SEG13	-370	1318	64	RES	-1070	-1318
5	S1	1643	-600	35	SEG14	-495	1318	65	INT	-945	-1318
6	S2	1643	-475	36	SEG15	-620	1318	66	SO1	-820	-1318
7	S3	1643	-350	37	SEG16	-745	1318	67	SO2	-695	-1318
8	S4	1643	-225	38	SEG17	-870	1318	68	SO3	-570	-1318
9	K1	1643	-100	39	SEG18	-995	1318	69	SO4	-445	-1318
10	K2	1643	25	40	SEG19	-1120	1318	70	A1	-320	-1318
11	K3	1643	150	41	SEG20	-1245	1318	71	A2	-195	-1318
12	K4	1643	275	42	SEG21	-1370	1318	72	A3	-70	-1318
13	M1	1643	400	43	SEG22	-1643	980	73	A4	55	-1318
14	M2	1643	525	44	SEG23	-1643	855	74	P1	180	-1318
15	M3	1643	650	45	SEG24	-1643	730	75	P2	305	-1318
16	M4	1643	775	46	SEG25	-1643	605	76	P3	430	-1318
17	N1	1643	900	47	SEG26	-1643	480	77	P4	555	-1318
18	N2	1643	1025	48	SEG27	-1643	355	78	XTOUT	680	-1318
19	N3	1643	1150	49	SEG28	-1643	230	79	XTIN	805	-1318
20	N4	1380	1318	50	SEG29	-1643	105	80	V _{DD2}	1030	-1318
21	TST	1255	1318	51	SEG30	-1643	-20	81	V _{DD1}	1155	-1318
22	SEG1	1130	1318	52	SEG31	-1643	-145	82	V _{SS}	1280	-1318
23	SEG2	1005	1318	53	SEG32	-1643	-270				
24	SEG3	880	1318	54	SEG33	-1643	-395				
25	SEG4	755	1318	55	SEG34	-1643	-520				
26	SEG5	630	1318	56	SEG35	-1643	-645				
27	SEG6	505	1318	57	COM4	-1643	-770				
28	SEG7	380	1318	58	COM3	-1643	-895				
29	SEG8	255	1318	59	COM2	-1643	-1020				
30	SEG9	130	1318	60	TESTC	-1570	-1318				

* TST, TESTRB, and TESTC PAD must be held open.

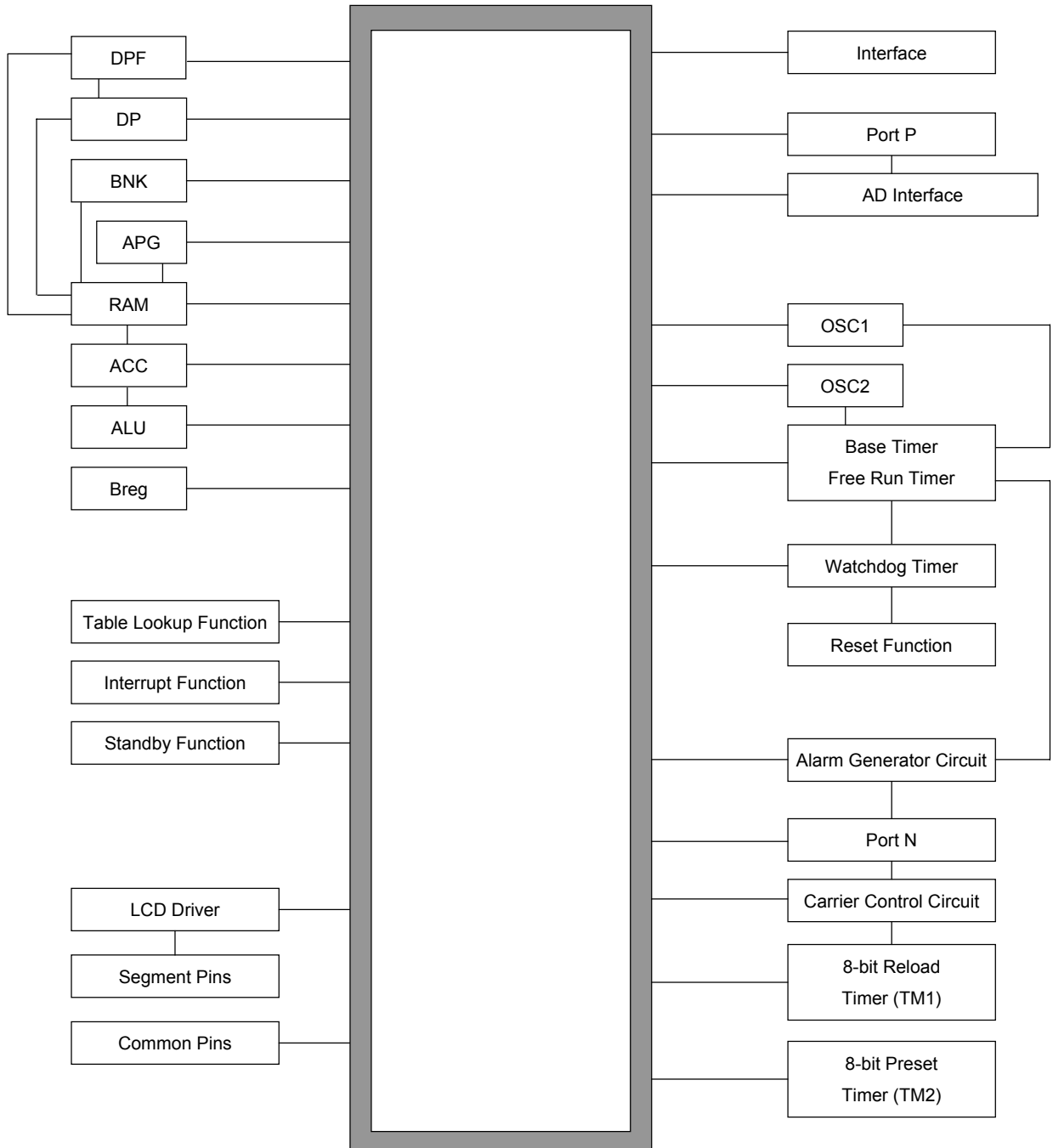
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Pin Layout



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System Block Diagram



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Mask Option Overview

The mask options make the microcontroller's hardware features conform with the application's specifications. The user can select mask options arbitrarily.

Oscillator circuit related options

- OSC1 SELECT-----Selects the OSC1 oscillation specifications to be applied to the application product.
1: EXT 2: RC 3: CF 4: NONUSED
- OSC1 PRE-DIV-----Selects the OSC1 system clock specifications.
1: OSC1/1 2: OSC1/2
- OSC1 WAIT TIME SELECT -----Selects the OSC1 release time.
1: 1/4K 2: 1/8K 3: 1/16K 4: 1/32K 5: 1/64K
- OSC2(Xtal) SELECT-----Selects the OSC2 oscillation specifications to be applied to the application product.
1: 2kHz 2: 5kHz 3: NONUSED
- OSC2(Xtal) CdRd SELECT-----Selects the OSC2 oscillation specifications.
1: USE 2: NONUSE

Other options

- RESISTOR SOURCE LEVEL-----Selects the pull-up or pull-down specifications.
1: PULL DOWN 2: PULL UP
- POWER SOURCE LEVEL -----Specifies the LCD voltage step-up or step-down circuit according to the power supply system selected.
1: $V_{DD} = 1.5V$ 2: $V_{DD} = 3.0V$
- RES PORT RESISTOR SELECT ---Selects the specifications for the RESET pin.
1: OPEN 2: PULL DOWN 3: PULL UP
- RES PORT LEVEL-----Selects the level of the reset signal.
1: L-LEVEL 2: H-LEVEL
- N PORT INITIAL LEVEL -----Selects the initial state of port N.
1: L-LEVEL 2: H-LEVEL
- N1 PORT-----Selects the output type of port N1.
1: N-CH 2: C-MOS
- N2 PORT-----Selects the output type of port N2.
1: N-CH 2: C-MOS
- N3 PORT-----Selects the output type of port N3.
1: N-CH 2: C-MOS
- N4 PORT-----Selects the output type of port N4.
1: N-CH 2: C-MOS

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Pin Function Chart

Pin Name	I/O	Function	Reset-time State
V _{SS}		Power supply (-) pin	
V _{DD}		Power supply (+) pin	
V _{DD1} V _{DD2}		<p>LCD drive power pin The external circuit control varies with the power requirements and LCD drive bias system.</p> <p>[1.5V power supply specifications]</p> <p>(1/1, 1/2 bias specifications) (1/3 bias specifications)</p> <p>[3.0V power supply specifications]</p> <p>(1/1 bias specifications) (1/2 bias specifications) (1/3 bias specifications)</p>	
CUP1 CUP2		<p>LCD drive pin The external circuit control varies with the LCD drive bias system.</p> <p>[1.5V power supply specification] Connect capacitor for 1/1, 1/2, and 1/3 bias systems.</p> <p>[3.0V power supply specifications] Connect capacitor for 1/2, 1/3 bias systems.</p>	
CFIN CFOUT	Input Output	OSC1 (fast mode) oscillator pin	
XTIN XTOUT	Input Output	OSC2 (slow mode) oscillator pin Xtal: 32kHz, 65kHz	
INT	Input	<p>1-bit input pin External interrupt pin The input type and interrupt level are determined by the program. (pull-up, pull-down, open) (rising edge, falling edge) Also available is the level hold function that prevents the pin from being floated.</p>	Interrupt acceptance: Disabled
S1 S2 S3 S4	Input Input Input Input	<p>4-bit input port Incorporate pull-up or pull-down resistors that can be controlled through the program on a port basis. Incorporate input change detector and chatter elimination circuits that can be controlled through the program in 1 bit units. The chatter elimination time varies with the oscillator specifications. 32.768kHz Xtal oscillator: 7.8ms or 1.95ms Also available is the level hold function that prevents the pin from being floated.</p>	Pull-up or -down resistor: ON (After reset: OFF)

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Pin Name	I/O	Function	Reset-time State
K1 K2 K3 K4	Input/output Input/output Input/output Input/output	4-bit input/output port Incorporate pull-up or pull-down resistors that can be controlled through the program on a port basis. Incorporate input change detector and chatter elimination circuits that can be controlled through the program on a port basis. The chatter elimination time varies with the oscillation specifications. 32.768kHz Xtal oscillator: 7.8ms or 1.95ms Output type: CMOS Also available is the "level hold function" that prevents the pin from being floated.	Input mode Pull-up or -down resistor: ON (After reset: OFF) Output latch data: High
SO1 SO2 SO3 SO4	Input/output Input/output Input/output Input/output	4-bit input/output port (also used by the serial interface) SO1: Serial input pin SO2: Serial output pin SO3: Serial clock pin 2-wire serial transmission is also possible. The SO4 pin can also be used as a halt reset or interrupt source pin when the serial function is not to be used. Incorporate pull-up or pull-down resistors that can be controlled through the program on a port basis. The output type can be controlled through the program on a port basis (CMOS/Nch). Also available is the "level hold function" that prevents the pin from being floated.	Input mode Pull-up or -down resistor: ON (After reset state is exited: OFF) 4-bit parallel mode Output latch data: High
M1 M2 M3 M4	Input/output Input/output Input/output Input/output	4-bit I/O port Incorporate pull-up or pull-down resistors that can be controlled through the program on a port basis. The output type can be controlled through the program on a port basis (CMOS/Pch). The M4 pin serves as a clock input pin when timer 2 is run in the event counter mode. Also available is the "level hold function" that prevents the pin from being floated.	Input mode Pull-up or -down resistor: ON (After reset state is exited: OFF) Output latch data: High
P1 P2 P3 P4	Input/output Input/output Input/output Input/output	4-bit I/O port Incorporate pull-up or pull-down resistors that can be controlled through the program on a port basis. The output type can be controlled through the program on a port basis (CMOS/Pch). Also available is the level hold function that prevents the pin from being floated.	Input mode Pull-up or -down resistor: ON (After reset state is exited: OFF) Output latch data: High
A1 A2 A3 A4	Input/output Input/output Input/output Input/output	4-bit I/O port Incorporate pull-up or pull-down resistors that can be controlled through the program on a port basis. The output type can be controlled through the program on a port basis (CMOS/Pch). Also available is the "level hold function" that prevents the pin from being floated.	Input mode Pull-up or -down resistor: ON (After reset state is exited: OFF) Output latch data: High
N1 N2 N3 N4	Output Output Output Output	4-bit output port The output type can be controlled through the program on a port basis (CMOS/Nch). These pins serve as a middle voltage withstand pin when output type is set to open-drain. The N3 pin is an output pin for generating the remote controller carrier signal. The N4 pin is an output pin for the alarm pulse signal.	The output level is determined by an option.
SEG01 to SEG35	Output Output	LCD panel segment drive pins Support 6 drive modes. Pins SEG01 to SEG16 can also be configured as general-purpose output pins (CMOS, Pch, Nch) through the program. The LCD drive and general-purpose output pins can be used in any combination.	
COM1 COM2 COM3 COM4	Output Output Output Output	LCD panel common electrode drive pins COM1 to COM4 are used according to the LCD drive duty mode. The LCD drive frequency (frame frequency) is determined under program control.	

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Pin Name	I/O	Function	Reset-time State
RES	Input	Input pin used to reset the microcontroller. 200 μ s or longer reset signal must be applied to this pin. The input type and reset level of this pin are determined with mask options.	
TST	Input	Test pin Must be connected to the V_{SS} pin (power supply-side).	

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