

**LC62F0164A**

16-Bit Single-Chip Microcontroller with On-Chip 64K-Word Flash EEPROM and 1K-Word RAM

Preliminary

Overview

The LC62F0164A single chip microcontroller integrates 64K words (128K bytes) of Flash EEPROM for program and data storage, 1K words (2K bytes) of internal RAM, 2 sets of timers (can be used as four timers), 2 channels of serial interfaces. The SANYO original high speed 16 bit CPU core (SNAIL) is used in the chip.

The LC62F0164A operates on 100 nS cycle time and most of instructions are one-word/one -cycle. The special architecture of the SNAIL core realizes both high speed operation and efficient code side. The instruction set of the SNAIL is simplified by disposing the instructions that are not frequently used. Simplified instruction set realized small core size like 8 bit microcontrollers and high speed operation like high performance 16 bit or 32 bit RISC chip. The SNAIL CPU core comprises high speed multiplier. The multiplier executes $16 \times 16 \rightarrow 32$ bits multiplication in two cycles.

The LC62F0164A has 1M bit Flash EEPROM for program and data storage. The contents of the Flash EEPROM can be written by three ways : parallel programming using EPROM programmer, on board programming using serial data input and data re-writing by program control. Using the data rewrite function by program control, the LC62F0164A can eliminate the external Flash EEPROM which is used in variety of applications.

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Features

- (1) High speed CPU core
 - 100nS cycle time (When Flash EEPROM is used)
 - Most instructions are one cycle/one word
 - Simple and efficient instructions
- (2) Integrated high speed multiplier
 - 16 × 16→32 bit
 - Two cycle pipelined
- (3) 1M bit Flash for program and data storage
 - The program and data area can freely be defined
 - On board rewrite function
 - Data rewrite function by program control
- (4) 1K word × 16 bits internal RAM (2K bytes)

(5) Ports

Port	# of pins	Input/Output	Other functions	Style	Flash control
P0	16	Input	External AD bus	With Pull-up resistor	
P1	16	Input/Output	External address bus	With Pull-up resistor	Data
P2	16	Input/Output		CMOS/N-ch OD With Pull-up resistor	Address
P3	15	Input/Output	Serial interface Counter input External bus control signals PWM output	CMOS/N-ch OD With Pull-up resistor	
	1	Input	READY signals		
P7	16	Input	External Interrupts AD converter	CMOS	Controls

(6) Timer - 2 sets (4 channels)

- Timer0 : Can be used as timer or pulse counter
 - 2 channels of 16 bit or one channel of 32 bit
 - Mode 0 : Two channels of 16 bit timers with programmable prescaler
 - Mode 1 : 16 bit timer with programmable prescaler + 16 bit pulse counter
 - Mode 2 : 32 bit timer with programmable prescaler
 - Mode 3 : 32 bit pulse counter
- Timer1 : Can be used as timer or PWM generator
 - 2 channels of 8 bit or one channel of 16 bit
 - Mode 0 : Two channels of 8 bit timers
 - Mode 1 : 8 bit timer + 8 bit PWM generator
 - Mode 2 : 16 bit timer
 - Mode 3 : Variable bit length PWM generator (9-16 bits)

(7) Serial Interface

- Two channels of 8 bit serial interface circuits
- Bit order switch function (LSB first or MSB first)
- 8 bit baud rate generator

(8) AD converter

- Eight channels of 10 bit AD converter

(9) External bus interface (under development)

2 external windows on data address space

- Programmable window address (512 address step)

- Programmable window size (512 words step)

Maximum of 32K words size each

- Independent control mode selection on each window

Two control mode : Multiplex or straight on each window

Wait state control (selectable from 2, 3, 4 or 5 waits)

External ready signal control

Automatic chip select signal generation

(10) Interrupts :

11 sources / 3 vectors

- 4 external interrupt INT0 / INT1 / INT2 / INT3

- 4 timer interrupts

- 2 serial interface interrupts

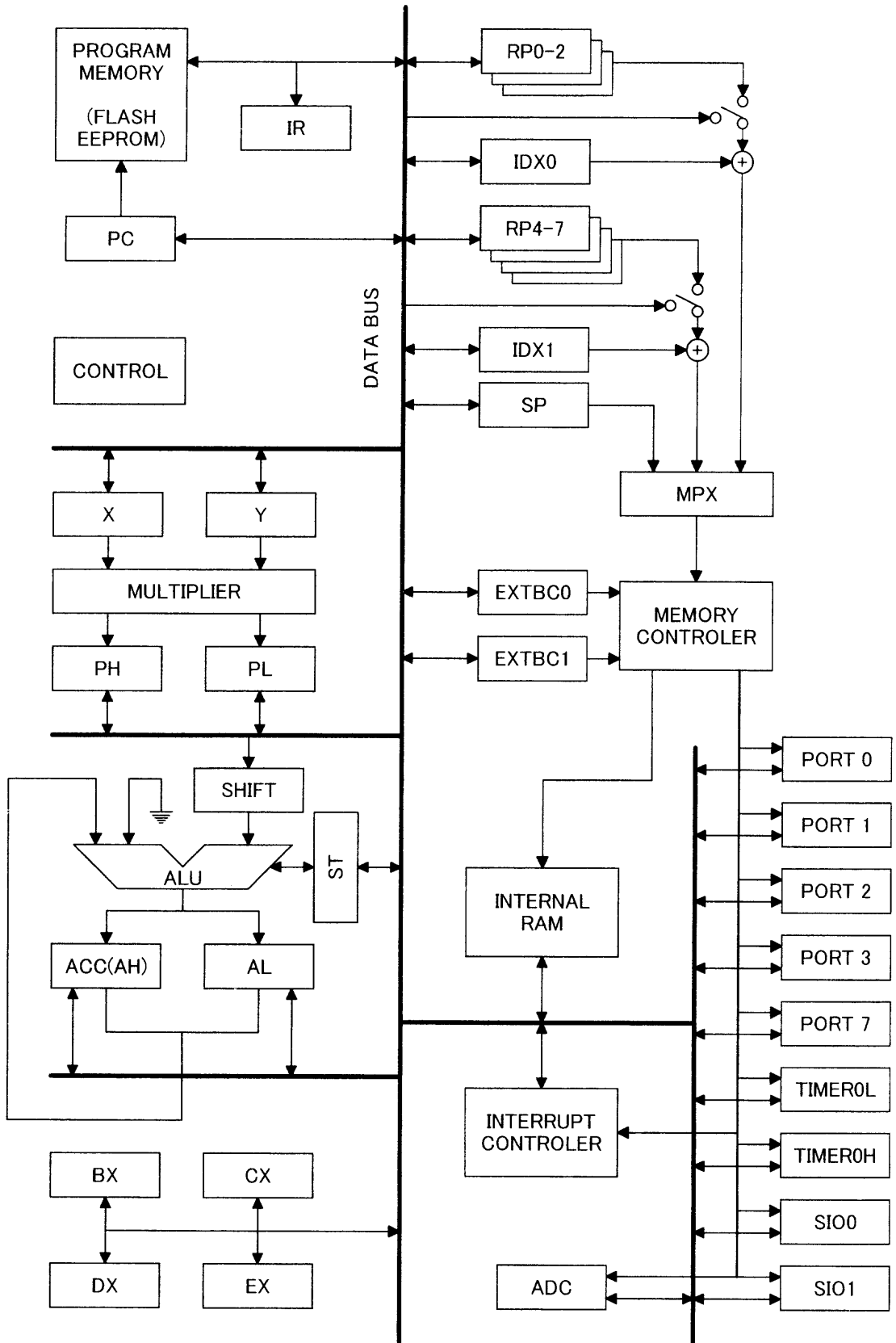
- 1 A/D converter

Programmable vector selection

Interrupt priority control function : Selectable from low/middle/high

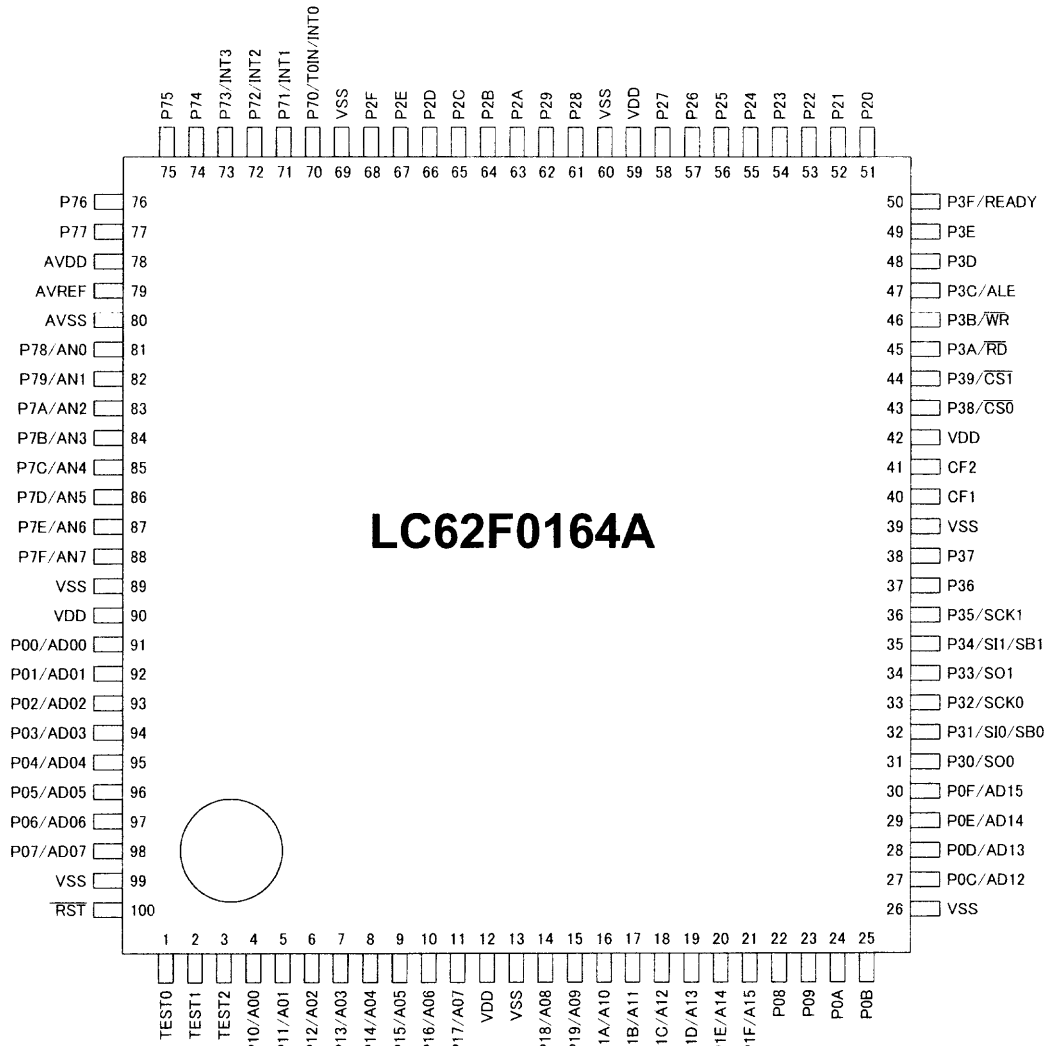
(11) SQFP-100 package

System Block Diagram



LC62F0164A

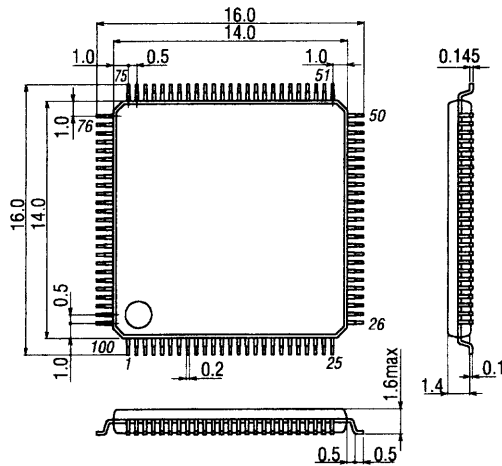
Pin Assignment



Package Dimension

(unit : mm)

3181B



SANYO : SQFP-100

1. Absolute Maximum Ratings at Ta=25°C, VSS1=VSS2=VSS3=VSS4=VSS5=VSS6=VSS7=AVSS=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings			unit
					min.	typ.	max.	
Supply voltage	VDDMAX	VDD1, VDD2, VDD3, VDD4 AVDD	VDD1=VDD2= VDD3=VDD4 =AVDD		-0.3		+6.5	V
Input voltage	VI	CF1, $\overline{\text{RST}}$, TEST 0-2 Ports 0,7, AVREF			-0.3		VDD+0.3	
Input/output voltage	VIO	Ports 1, 2, 3			-0.3		VDD+0.3	
High level output current	Peak output current	IOPH	Ports 1, 2, 3	•CMOS output •For each pin.		-15		mA
	Total output current	$\Sigma\text{IOAH}(1)$	Port 1	The total of all pins.		-30		
		$\Sigma\text{IOAH}(2)$	Port 2	The total of all pins.		-30		
		$\Sigma\text{IOAH}(3)$	Port 3	The total of all pins.		-30		
Low level output current	Peak output current	IOPL	Ports 1, 2, 3	For each pin.			15	
	Total output current	$\Sigma\text{IOAL}(1)$	Port 1	The total of all pins.			30	
		$\Sigma\text{IOAL}(2)$	Port 2	The total of all pins.			30	
		$\Sigma\text{IOAL}(3)$	Port 3	The total of all pins.			30	
Maximum power dissipation	Pdmax	SQFP100	Ta=0 to +50°C				350	mW
Operating temperature range	Topg				0		+50	°C
Storage temperature range	Tstg				-55		+125	

2. Recommended Operating Range at Ta=0 to +50°C, VSS1=VSS2=VSS3=VSS4=VSS5=VSS6=VSS7=AVSS=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD[V]	min.	typ.		max.
Operating supply voltage range	VDD	VDD1, VDD2, VDD3, VDD4 AVDD	$98\text{NS} \leq t_{\text{CYC}} \leq 102\text{NS}$		4.5		5.5	V
Input high voltage	V _{IH}	•Ports 0, 1, 2, 3, 7 • $\overline{\text{RST}}$		4.5 - 5.5	0.75VDD		VDD	
Input low voltage	V _{IL(1)}	•Ports 0, 1, 2, 3, 7 • $\overline{\text{RST}}$		4.5 - 5.5	VSS		0.25VDD	
	V _{IL(2)}	TEST 0, 1, 2		4.5 - 5.5	VSS		0.3VDD	
Operation cycle time	t _{CYC}			4.5 - 5.5	98		102	NS
Oscillation frequency range (Note 1)	F _{mCF}	CF1, CF2	20MHz ceramic resonator oscillation Refer to figure 1	4.5 - 5.5	19.6	20	20.4	MHz
	F _{sXtal}	CF1, CF2	20MHz crystal resonator oscillation Refer to figure 1	4.5 - 5.5		20		MHz
Oscillation stabilizing time period (Note 2)	T _{msCF}	CF1, CF2	20MHz ceramic resonator oscillation Refer to figure 3	4.5 - 5.5			5	ms
	T _{ssXtal}	CF1, CF2	20MHz crystal resonator oscillation Refer to figure 3	4.5 - 5.5			5	s

(Note 1) The oscillation constant is shown in Tables 1.

3. Electrical Characteristics at Ta=0 to +50°C, VSS1=VSS2=VSS3=VSS4=VSS5=VSS6=VSS7=AVSS=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD[V]	min.	typ.		max.
Input high current	I _{HH} (1)	•Ports 1, 2, 3	•Output disable •Pull-up resistor off •VIN=VDD (including off state leak current of output Tr.)	4.5 - 5.5			1	μA
	I _{HH} (2)	Port 0	•Pull-up resistor off •VIN=VDD	4.5 - 5.5			1	
	I _{HH} (3)	Port 7, \overline{RST}	VIN=VDD	4.5 - 5.5			1	
Input low current	I _{LL} (1)	Ports 1, 2, 3	•Output disable •Pull-up resistor off •VIN=VSS (including off state leak current of output Tr.)	4.5 - 5.5	-1			
	I _{LL} (2)	Port 0	•Pull-up resistor off •VIN=VSS	4.5 - 5.5	-1			
	I _{LL} (3)	Port 7, \overline{RST}	VIN=VSS	4.5 - 5.5	-1			
Output high current	VOH(1)	Port 1	IOH=-10mA	4.5 - 5.5	VDD-1.5			V
	VOH(2)	Ports 2, 3	IOH=-10mA CMOS output	4.5 - 5.5	VDD-1.5			
Output low current	VOL	Ports 1, 2, 3	IOL=10mA	4.5 - 5.5			1.5	V
Pull-up resistor	R _{pu}	Ports 0, 1, 2, 3	VIN=VSS	5.0	70	100	124	kΩ
Hysteresis voltage	V _{HIS}	• \overline{RST} •Ports 0, 1, 2, 3, 7		4.5 - 5.5		0.1VDD		V
Pin capacitance	CP	All pins	•Every other terminal connected to VSS. •f=1MHz •Ta=25°C	4.5 - 5.5		10		pF

4. Serial Input/Output Characteristics at Ta=0 to +50°C, VSS1=VSS2=VSS3=VSS4=VSS5=VSS6=VSS7=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit				
				VDD[V]	min.	typ.		max.			
Serial clock	Input clock	Cycle	tSCK(1)	SCK0(P32), SCK1(P35)	Refer to figure 5	4.5 - 5.5	2			tCYC	
		Low level pulse width					tSCKL(1)	1			
		High level pulse width					tSCKH(1)	1			
	Output clock	Cycle	tSCK(2)	SCK0(P32), SCK1(P35)	<ul style="list-style-type: none"> •When output is CMOS •Refer to figure 5 	4.5 - 5.5	2			tCYC	
		Low level pulse width					tSCKL(2)		1/2		tSCK
		High level pulse width					tSCKH(2)		1/2		
Serial input	Data set-up time	tsDI	SB0(P31), SB1(P34), SI0, SI1	<ul style="list-style-type: none"> •Data set-up to SI0CLK •Refer to figure 5 	4.5 - 5.5	0.03			µs		
	Data hold time	thDI				0.03					
Serial output	Output delay time	tdD0	SO0(P30), SO1(P33), SB0(P31), SB1(P34)	<ul style="list-style-type: none"> •Data set-up to SI0CLK •When output is CMOS •Refer to figure 5 	4.5 - 5.5			1/3tCYC +0.05			

5. Pulse Input Conditions at Ta=0 to +50°C, VSS1=VSS2=VSS3=VSS4=VSS5=VSS6=VSS7=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD[V]	min.	typ.		max.
High/low level pulse width	tPIH(1)	INT0(P70), INT1(P71), INT2(P72), INT3(P73)	<ul style="list-style-type: none"> •Interrupt acceptable •Events to timer 0 can be input. 	4.5 - 5.5	2			tCYC
	tPIL(1)							
	tPIL(2)	RST	Reset acceptable	4.5 - 5.5	2			

6. AD Converter Characteristics at Ta=0 to +50°C, VSS1=VSS2=VSS3=VSS4=VSS5=VSS6=VSS7=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings			unit
					min.	typ.	max.	
Resolution	N	AN0(P78) - AN7(P7F)		4.5 - 5.5		10		bit
Absolute precision	ET			4.5 - 5.5			±8	LSB
Conversion time	TCAD		AD conversion time =14 × ADTR × tCYC (ADTR=3)	4.5 - 5.5	4.12 (tCYC= 98NS)		4.28 (tCYC= 102NS)	µs
Reference input voltage	AVREF	AVREF		4.5 - 5.5	VSS		VDD	V
Reference input current range	IRIF	AVREF	AVREF=VDD	4.5 - 5.5	75	150	300	µA
Analog input voltage range	VAIN	AN0(P78) - AN7(P7F)		4.5 - 5.5	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5 - 5.5			1	µA
	IAINL		VAIN=VSS	4.5 - 5.5	-1			

7. Current Dissipation Characteristics at Ta=0 to +50°C, VSS1=VSS2=VSS3=VSS4=VSS5=VSS6=VSS7=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings			unit
					min.	typ.	max.	
Current flow during basic operation (Note 2)	IDDOP(1)	VDD1 =VDD2 =VDD3 =VDD4 =AVDD	•FmCF=20MHz for Ceramic resonator oscillation, Crystal oscillation	4.5 - 5.5		60	80	mA

(Note 2) The currents of output transistors and pull-up MOS transistors are ignored.

Table 1. Guaranteed constant ceramic oscillators (main-clock)

Type of oscillator	Producer	Oscillator	C1	C2
20MHz crystal oscillator	Daishinku	TBD		
20MHz Ceramic oscillator	Murata	TBD		
		TBD	Built in	

* Both C1 and C2 must use K rank ($\pm 10\%$) and SL characteristics.

- (Notes)
- Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.
 - If other oscillators are used, we provide no guarantee of performance.

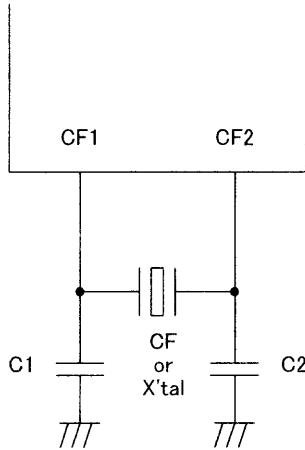


Figure 1 Ceramic oscillation circuit
Crystal oscillation circuit

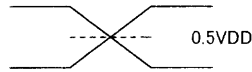


Figure 2 AC timing measurement point

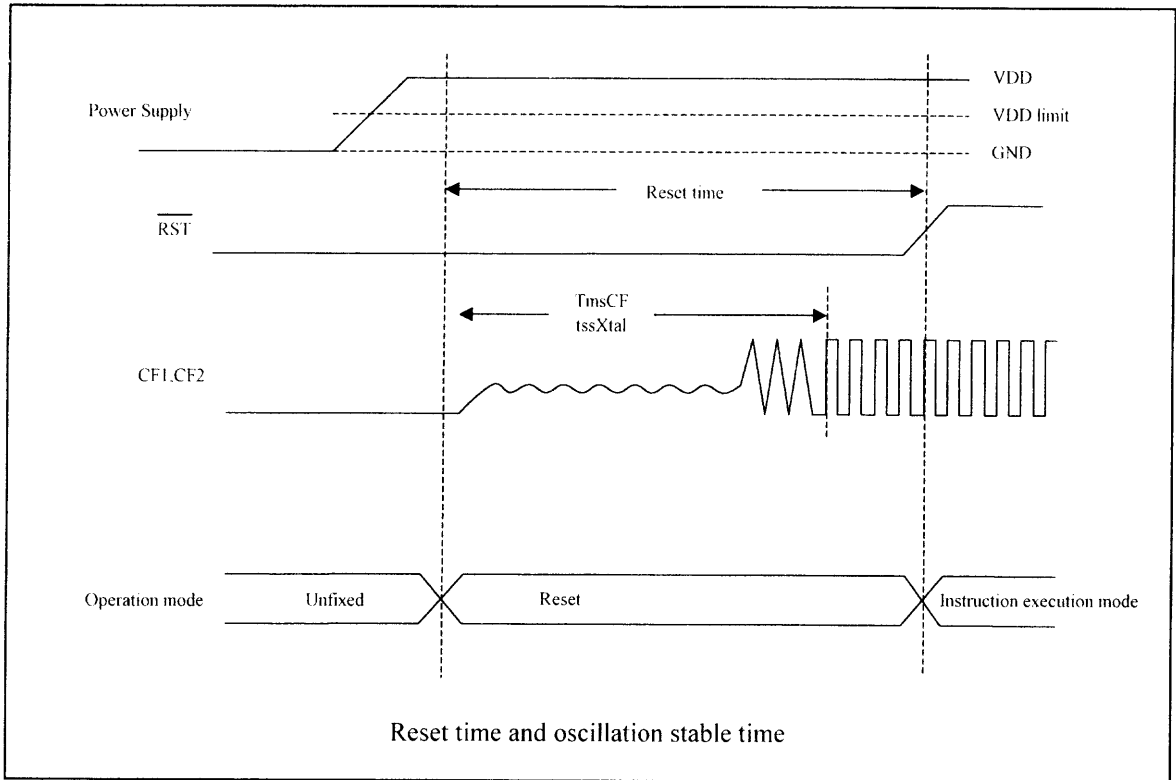


Figure 3 Oscillation stabilizing time

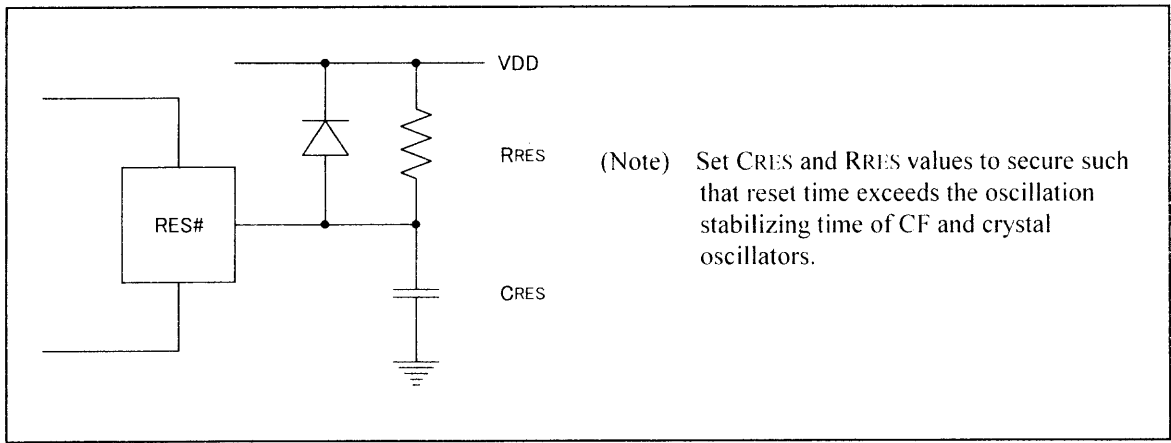


Figure 4 Reset circuit

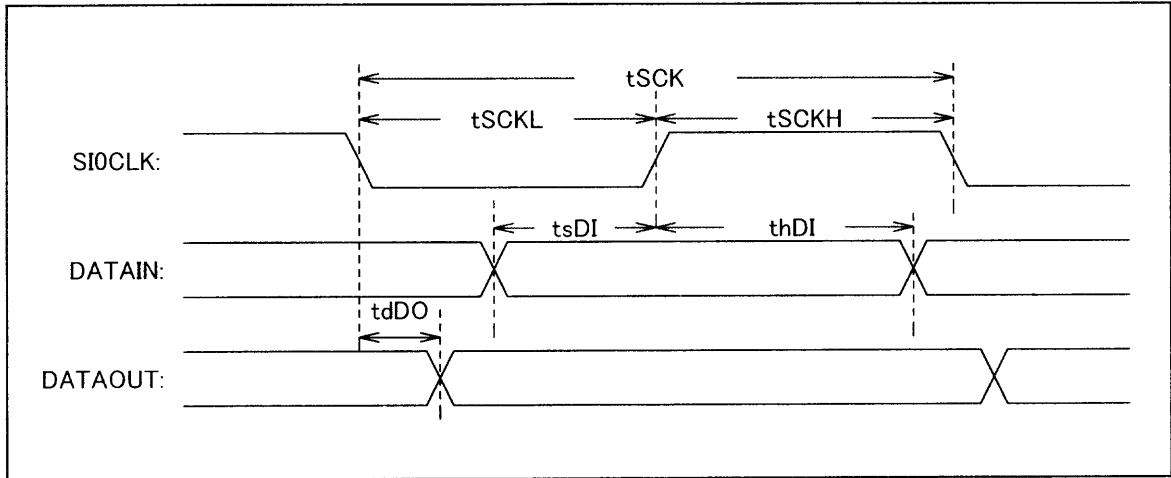


Figure 5 Serial input/output test condition

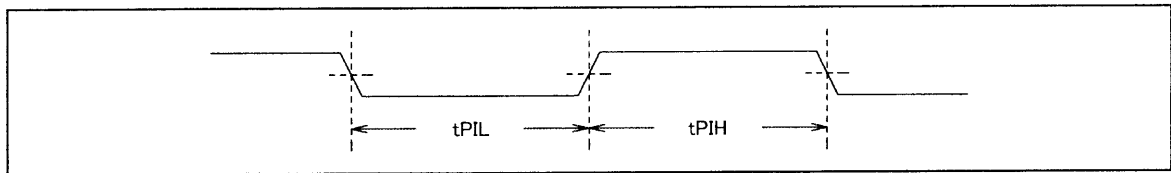


Figure 6 Pulse input timing condition

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